Ordering number : ENN6198A

Monolithic Digital IC

LB1928

Three-Phase Brushless Motor Driver for Office Automation Equipment

Overview

The LB1928 is a 3-phase brushless motor driver well suited for drum and paper feed motors in laser printers, plain-paper copiers and other office automation equipment. Direct PWM drive allows control with low power losses. Peripheral circuitry including speed control circuit and FG amplifier is integrated, thus allows drive circuit to be constructed with a single chip.

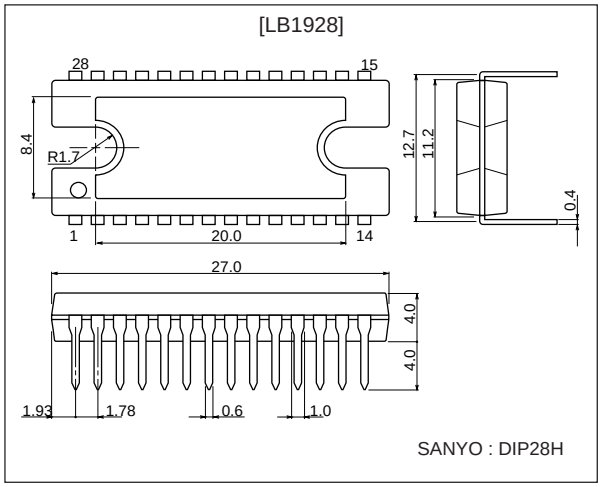
Functions and Features

- Three-phase bipolar drive (30V, 3.1A)
- Direct PWM drive technique
- Built-in diode for absorbing output lower-side kickback
- Speed discriminator and PLL speed control
- Speed lock detection output
- Built-in forward/reverse switching circuit
- Built-in protection circuitry includes current limiter, overheat protection, motor restraint protection, etc.

Package Dimensions

unit: mm

3147B-DIP28H



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	Vcc max		30	V
Maximum output current	I_O max	T ≤ 500 ms	3.1	A
Allowable power dissipation 1	Pd max 1	IC only	3	W
Allowable power dissipation 2	Pd max 2	With an arbitrary large heat sink	20	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage range 1	Vcc		9.5 to 28	V
Regulator voltage output current	I_{REG}		0 to –20	mA
LD output current	I_{LD}		0 to 15	mA

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SANYO Electric Co.,Ltd. Semiconductor Company

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Electrical Characteristics at Ta = 25˚C, Vcc = VM = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current 1	Icc1			23	30	mA
Power supply current 2	Icc2	In STOP mode		3.5	5	mA
[Output block]						
Output saturation voltage 1	Vosat1	Io = 1.0A, Vo(SINK) + Vo(SOURCE)		2.0	2.5	V
Output saturation voltage 2	Vosat2	Io = 2.0A, Vo(SINK) + Vo(SOURCE)		2.6	3.2	V
Output leak current	Ioleak				100	μA
Lower-side diode forward voltage 1	V_D1	I_D = –1.0A		1.2	1.5	V
Lower-side diode forward voltage 2	V_D2	I_D = –2.0A		1.5	2.0	V
[5V regulator voltage output]						
Output voltage	V_{REG}	Io = –5 mA	4.65	5.00	5.35	V
Voltage fluctuation	$\Delta V_{REG}1$	Vcc = 9.5 to 28V		30	100	mV
Load fluctuation	$\Delta V_{REG}2$	Io = –5 to –20 mA		20	100	mV
[Hall amplifier]						
Input bias current	I_{HB}		–2	–0.5		μA
Common mode input voltage range	V_{ICM}		1.5		V_{REG} –1.5	V
Hall input sensitivity			80			mVp-p
Hysteresis width	ΔV_{IN}		15	24	42	mV
Input voltage L -> H	V_{SLH}			12		mV
Input voltage H-> L	V_{SHL}			–12		mV
[PWM oscillator]						
Output High level voltage	$V_{OH(PWM)}$		2.5	2.8	3.1	V
Output Low level voltage	$V_{OL(PWM)}$		1.2	1.5	1.8	V
Oscillator frequency	$f_{(PWM)}$	C = 3900 pF		18		kHz
Amplitude	$V_{(PWM)}$		1.05	1.30	1.55	Vp-p
[CSD circuit]						
Operating voltage	$V_{OH(CSD)}$		3.6	3.9	4.2	V
External capacitance charge current	I_{CHG}		–17	–12	–9	μA
Operating time	$t_{(CSD)}$	C = 10 μF Design target value		3.3		s
[Current limiter operation]						
Limiter	V_{RF}	V_{CC}-VM	0.45	0.5	0.55	V
[Thermal shutdown operation]						
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value (junction temperature)		50		°C
[FG amplifier]						
Input offset voltage	$V_{IO(FG)}$		–10		+10	mA
Input bias current	$I_{B(FG)}$		–1		+1	μA
Output High level voltage	$V_{OH(FG)}$	I_{FGO} = –0.2 mA	V_{REG} –1.2	V_{REG} –0.8		V
Output Low level voltage	$V_{OL(FG)}$	I_{FGO} = 0.2 mA		0.8	1.2	V
FG input sensitivity		Gain 100 times	3			mV
Next-stage Schmitt comparator width		Design target value	100	180	250	mV
Operating frequency range					2	kHz
Open-loop gain		f(FG) = 2 kHz	45	51		dB
[Speed discriminator]						
Output High level voltage	$V_{OH(D)}$	I_{DO} = –0.1 mA	V_{REG} –1.0	V_{REG} –0.7		V
Output Low level voltage	$V_{OL(D)}$	I_{DO} = 0.1 mA		0.8	1.1	V
Count number				512		
[PLL output]						
Output High level voltage	$V_{OH(P)}$	I_{PO} = –0.1 mA	V_{REG} –1.8	V_{REG} –1.5	V_{REG} –1.2	V
Output Low level voltage	$V_{OL(P)}$	I_{PO} = 0.1 mA	1.2	1.5	1.8	V
[Lock detection]						
Output Low level voltage	$V_{OL(LD)}$	I_{LD} = 10 mA		0.15	0.5	V
Lock range				6.25		%

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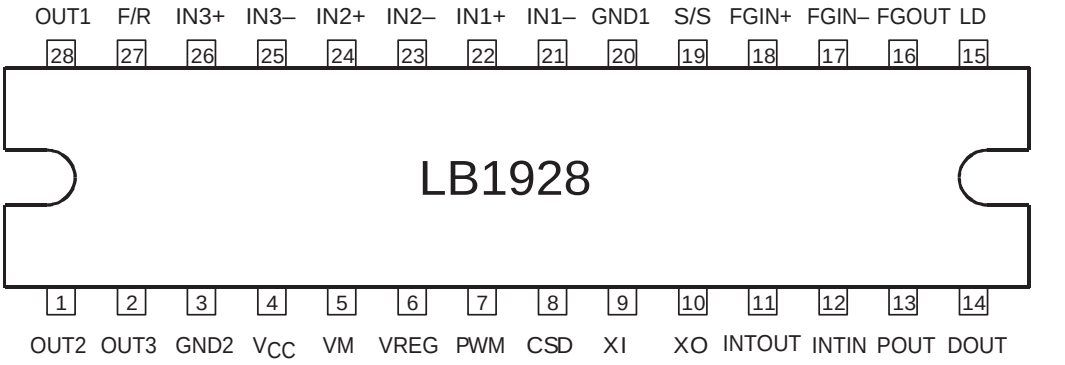
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Integrator]						
Input bias current	$I_{B(INT)}$		–0.4		+0.4	μA
Output High level voltage	$V_{OH(INT)}$	I_{INTO} = –0.2 mA	V_{REG} –1.2	V_{REG} –0.8		V
Output Low level voltage	$V_{OL(INT)}$	I_{INTO} = 0.2 mA		0.8	1.2	V
Open-loop gain		f(INT) = 1 kHz	45	51		dB
Gain bandwidth product		Design target value		450		kHz
Reference voltage		Design target value	–5%	V_{REG}/2	5%	V
[Crystal oscillator]						
Operating frequency range	fOSC		3		10	MHz
Low level pin voltage	V_{OSCL}	I_{OSC} = –0.5 mA		1.65		V
High level pin current	I_{OSCH}	V_{OSC} = V_{OSCL} + 0.3V		0.4		mA
[Start/stop pin]						
High level input voltage range	$V_{IH(S/S)}$		3.5		V_{REG}	V
Low level input voltage range	$V_{IL(S/S)}$		0		1.5	V
Input open voltage	$V_{IO(S/S)}$		V_{REG} –0.5		V_{REG}	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
High level input current	$I_{IH(S/S)}$	$V_{(S/S)}$ = V_{REG}	–10	0	10	μA
Low level input current	$I_{IL(S/S)}$	$V_{(S/S)}$ = 0V	–280	–210		μA
[Forward/reverse pin]						
High level input voltage range	$V_{IH(F/R)}$		3.5		V_{REG}	V
Low level input voltage range	$V_{IL(F/R)}$		0		1.5	V
Input open voltage	$V_{IO(F/R)}$		V_{REG} –0.5		V_{REG}	V
Hysteresis width	ΔV_{IN}		0.35	0.50	0.65	V
High level input current	$I_{IH(F/R)}$	$V_{(F/R)}$ = V_{REG}	–10	0	+10	μA
Low level input current	$I_{IL(F/R)}$	$V_{(F/R)}$ = 0V	–280	–210		μA

Truth Table

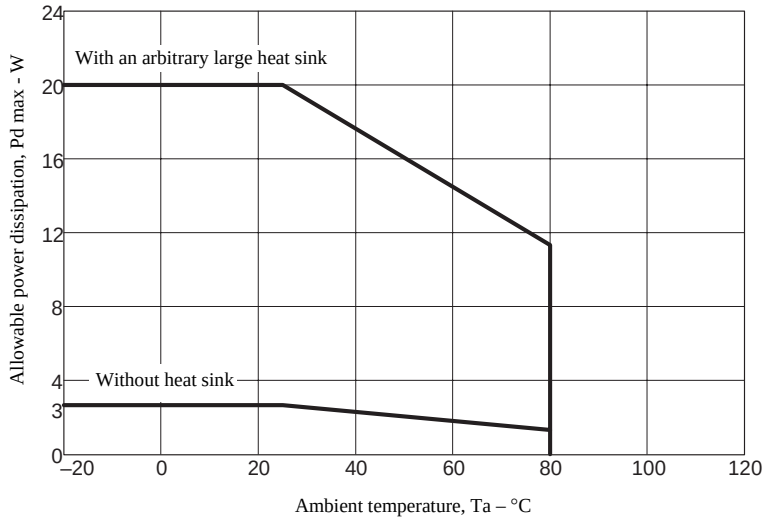
	Source / Sink	F/R = "L"			F/R = "H"		
		IN1	IN2	IN3	IN1	IN2	IN3
1	OUT2 -> OUT1	H	L	H	L	H	L
2	OUT3 -> OUT1	H	L	L	L	H	H
3	OUT3 -> OUT2	H	H	L	L	L	H
4	OUT1 -> OUT2	L	H	L	H	L	H
5	OUT1 -> OUT3	L	H	H	H	L	L
6	OUT2 -> OUT3	L	L	H	H	H	L

Pin Assignment



Top view

Pd max – Ta

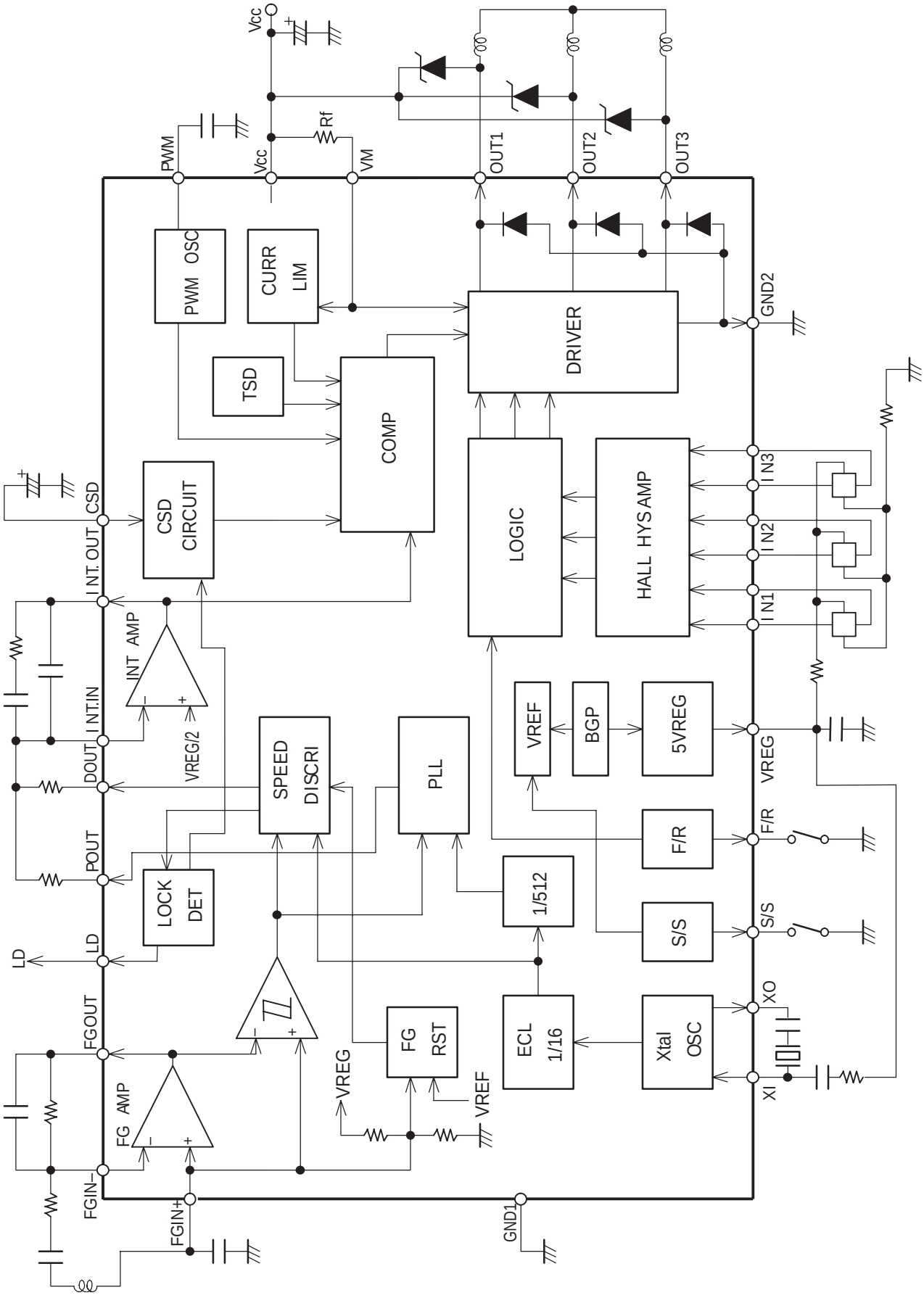


Relationship between crystal oscillator frequency fosc and FG frequency fFG is as follows.

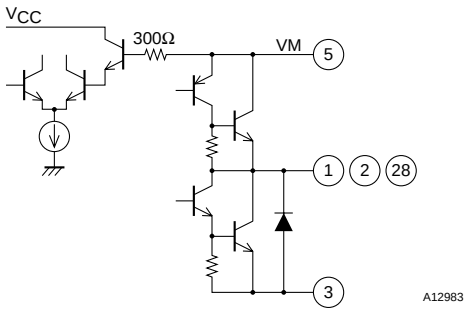
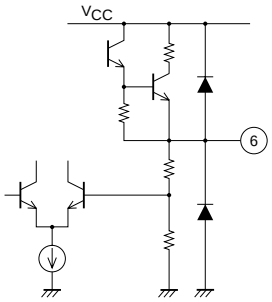
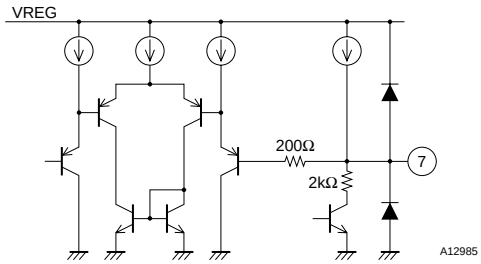
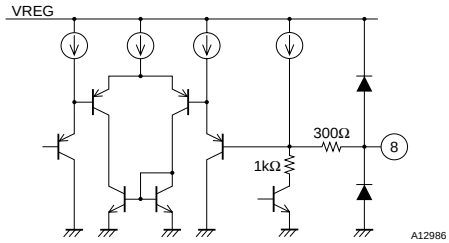
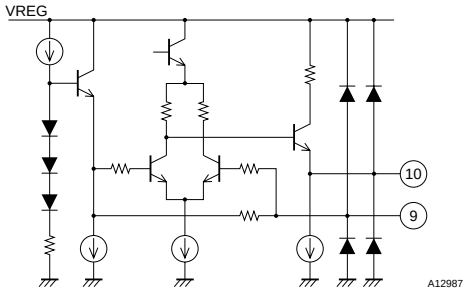
fFG (servo) = fosc/ (ECL divide-by-16 × count number)

= fosc/8192

Equivalent Circuit Block Diagram

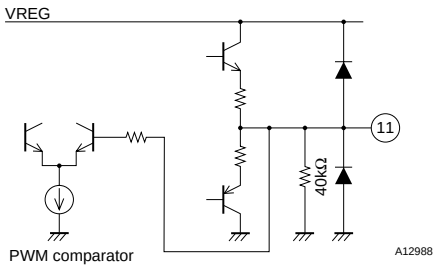
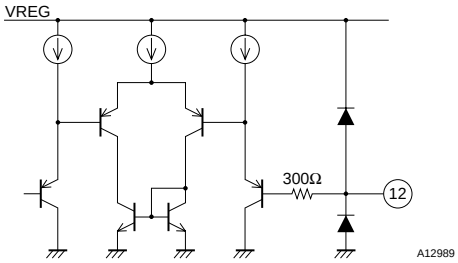
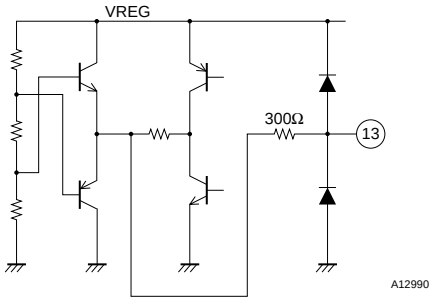
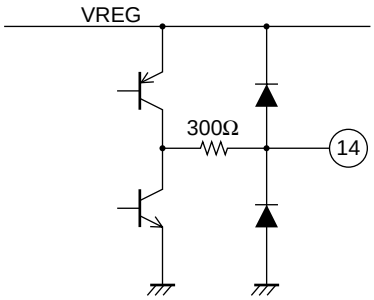
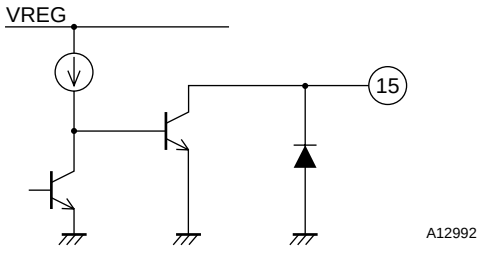


Pin Description

Pin number	Pin name	Equivalent circuit	Pin function
28 1 2	OUT1 OUT2 OUT3		Motor drive output pins. Connect a Schottky diode between these outputs and V_{CC}.
3	GND2		Output ground pin.
5	VM		Output block power supply and output current detection pin. Connect a resistor (Rf) between this pin and V_{CC} to detect the output current as a voltage. The output current is limited according to the equation I_{OUT} = VRF/Rf.
4	V_{CC}		Power supply pin (except for output block)
6	VREG		Regulated power supply output pin (5V output) Connect a capacitor (approx. 0.1 μF) between this pin and ground to stabilize the output.
7	PWM		PWM frequency setting pin. Connect a capacitor between this pin and ground. C = 3900 pC results in a frequency of about 18 kHz.
8	CSD		Lock protection circuit operation time setting pin. Connecting a capacitor of about 10 μF between this pin and ground results in a protection circuit operation time of about 3.3 seconds.
9 10	XI XO		Quartz oscillator pins. Connect to quartz oscillator to generate the reference clock. When an external clock (of several MHz) is used, the clock signal should be input via a resistor of about 5.1 kΩ connected in series with the XI pin. In this case, the XO pin must be left open.

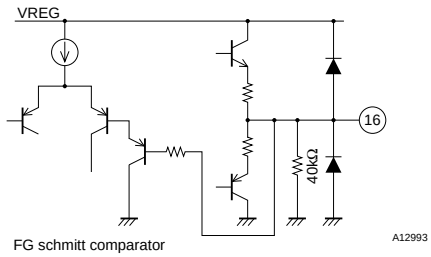
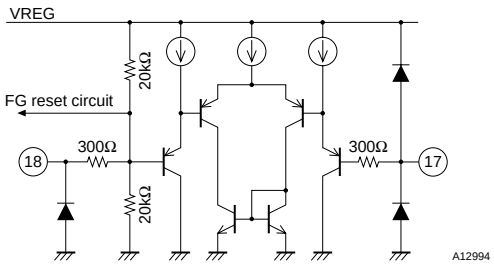
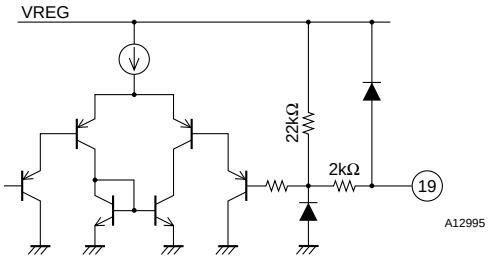
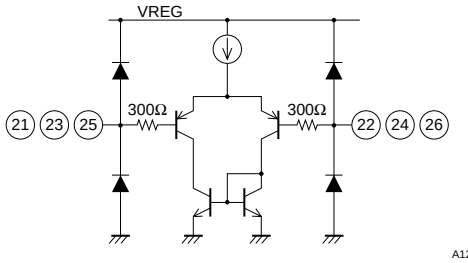
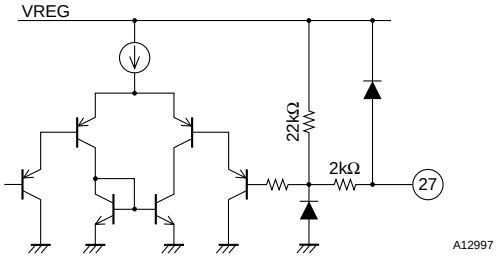
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Pin number	Pin name	Equivalent circuit	Pin function
11	INT OUT		Integrator output pin (speed control pin)
12	INT IN		Integrator input pin.
13	POUT		PLL output pin.
14	DOUT		Speed discriminator output pin. Acceleration: High, Deceleration: Low
15	LD		Speed lock detection pin. When motor rotation is within lock range (±6.25%): Low Withstand voltage: 30V max.

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Pin number	Pin name	Equivalent circuit	Pin function
16	FG OUT		FG amplifier output pin.
17 18	FGIN– FGIN+		FG amplifier input pin. By connecting a capacitor (approx. 0.1 μF) between FGIN+ and ground, the logic circuitry is reset.
19	S/S		Start/stop control pin. Start (Low): 0V to 1.5V Stop (High): 3.5V to VREG High when open. Hysteresis width: approx. 0.5V.
20	GND1		Ground pin (except for output block).
22 21 24 23 26 25	IN1+ IN1– IN2+ IN2– IN3+ IN3–		Hall input pins. High when IN+ > IN–, Low when IN+ < IN–. Hall signal should have an amplitude of at least 100 mVp–p (differential operation). When Hall signal noise is a problem, connect a capacitor between IN+ and IN–.
27	F/R		Forward/reverse control pin. Forward (Low): 0V to 1.5V Reverse (High): 3.5V to VREG High when open. Hysteresis width: approx. 0.5V.

Description of the LB1928

1. Speed control circuit

   The IC performs speed control through combined use of a speed discrimination circuit and PLL circuit. The speed control circuit counts FG cycles and outputs a deviation signal every 2 FG cycles. The PLL circuit outputs a phase deviation signal every FG cycle.

   The FG servo frequency is determined by the following equation. The motor rotation speed is set by the number of FG pulses and the crystal oscillator frequency.

   fFG (servo) = fOSC/8192

   fOSC: Crystal oscillator frequency

2. Output drive circuit

   In order to reduce power loss at the output, the LB1928 uses the PWM drive technique. While ON, the output transistors are always saturated, and motor drive power is adjusted by varying the output ON duty ratio. Because output PWM switching is performed by the lower-side output transistor, a Schottky diode must be connected between OUT and V_{CC}. (If the reverse recovery time of the diode is too long, a feedthrough current will flow at the instant when the lower-side transistor goes ON.) An internal diode is provided between OUT and GND. If large output current causes a problem (waveform distortion during lower-side kickback, etc.), an external rectifying diode or Schottky diode should be connected.

   The output diode is integrated only on the lower side.

3. Current limiting circuit

   The current limiting circuit limits the peak current to the value I = VRF/Rf (VRF = 0.5 V typ., Rf: current detector resistance). Current limiting is achieved by reducing the ON duty ratio of the output, which reduces the current.

4. Power save circuit

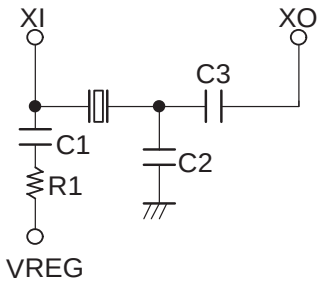
   In order to reduce current drain in the STOP condition, the IC goes into power save mode. In this condition, bias current to most circuits is cut off, but the 5V regulator output remains active.

5. Reference clock

   The reference clock for speed control can be input using one of the following two methods.

   [1] Using a crystal oscillator

   When a crystal is used for oscillation, connect the crystal, capacitors, and a resistor as shown in the figure below.



C1, R1: For stable oscillation

C3: For crystal coupling

C2: For overtone oscillation prevention

(Reference values)

Oscillator frequency (MHz)	C1 (μF)	C2 (pF)	C3 (pF)	R1 (Ω)
3 to 5	0.1	10	47	330k
5 to 8	0.1	None	47	330k
8 to 10	0.1	None	22	330k

The circuit configuration and values are for reference only. The crystal oscillator's characteristics as well as the possibility of floating capacitance and noise due to layout factors must be taken into consideration when designing an actual application.

[Precautions for wiring layout design]

Since the crystal oscillator circuit operates at high frequencies, it is susceptible to the influence of floating capacitance from the circuit board. Wiring should be kept as short as possible and traces should be kept narrow.

When designing the external circuitry, pay special attention to the wiring layout between the oscillator and C3 (C2), to minimize the influence of floating capacitance.

[2] External clock input (equivalent to crystal oscillator, several MHz)

When using an external signal source instead of a crystal oscillator, the clock signal should be input from the XO pin through a resistor of about 5.1 kΩ connected to the pin in series. The XO pin should be left open.

Signal input level

Low : 0 to 0.8V

High : 2.5 to 5.0V

6. Speed lock range

The speed clock range is ±6.25% of the rated speed. When the motor rotation is within the lock range, the LD pin becomes Low (open collector output). When the motor rotation goes out of the lock range, the ON duty ratio of the motor drive output is varied according to the amount of deviation to bring the rotation back into the lock range.

7. PWM frequency

The PWM frequency is determined by the capacitance connected to the PWM pin.

$$f_{PWM} \fallingdotseq 1/(14400 \times C)$$

The PWM frequency should be between 15 and 25 kHz.

8. Hall input signal

The Hall input requires a signal with an amplitude of at least the hysteresis width (42 mV max.). Taking possible noise influences into consideration, an amplitude of at least 100 mV is desirable.

9. Forward/reverse switching

Forward/reverse switching of motor rotation is carried out with the F/R pin. If this is performed while the motor is running, the following points must be observed:

- Feedthrough current during switching is handled by proper circuit design. However, the V_{CC} voltage rise during switching (caused by momentary return of motor current to power supply) must not exceed the rated voltage (30V). If problems occur, the capacitance between V_{CC} and GND must be increased.
- If the motor current after switching exceeds the current limiter value, the lower-side transistors go OFF but the upper-side transistors go into the short brake state, which causes a current flow. The magnitude of the current is determined by the motor counterelectromotive voltage and the coil resistance. This current may not exceed the rated current (3.1A). (Forward/reverse switching at high speed therefore is not safe.)

10. Motor restraint protection circuit

To protect the IC and the motor itself when rotation is inhibited, a restraint protection circuit is provided. If the LD output is High (unlocked) for a certain interval in the start condition, the lower-side transistors are turned off. The length of the interval is determined by the capacitance at the CSD pin. A capacitance of 10 μF results in a set interval of about 3.3 seconds. (Tolerance approx. ±30%)

Set interval (s) ≒ 0.33 × C (μF)

If the capacitor arrangement is subject to leak current, possible adverse effects such as setting time tolerances must be taken into consideration.

When the restraint protection circuit has been activated, the condition can only be canceled by setting the system to the stop condition or by turning the power off and on again (in the stop condition). When wishing not to use the restraint protection circuit, connect the CSD pin to ground.

If the stop time when releasing the restraint protection is short, the capacitor charge will not be fully dissipated. This in turn will cause a shorter restraint protection activation time after the motor has been restarted. The stop time should therefore be designed to be sufficiently long, using the equation shown below (also when restarting in the motor start transient state).

Stop time (ms) ≥ 15 × C (μF)

11. Power supply regulation

Because this IC has a high output current, power supply line fluctuations can occur easily. Therefore a capacitor of sufficient capacitance must be connected between the V_{CC} pin and ground to assure stable operation. If a diode is used in the power line for reverse-connection protection, the likelihood of power line fluctuations increases further, which will require more capacitance.

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