Dual-Channel Ultralow Noise Amplifier with Selectable Gain and Input Impedance

Data Sheet **AD8432**

FEATURES

- **Low noise**
  - **Input voltage noise: 0.85 nV/√Hz**
  - **Current noise: 2.0 pA/√Hz**
- **High speed**
  - **200 MHz bandwidth (G = 12.04 dB)**
  - **295 V/µs slew rate**
- **Selectable gain**
  - **G = 12.04 dB (×4)**
  - **G = 18.06 dB (×8)**
  - **G = 21.58 dB (×12)**
  - **G = 24.08 dB (×16)**
- **Active input impedance matching**
- **Integrated input clamp diodes**
- **Single-ended input, differential output**
- **Supply range: 4.5 V to 5.5 V**
- **Low power: 60 mW/channel**

APPLICATIONS

- **CW Doppler ultrasound front ends**
- **Low noise preamplification**
- **Predriver for I/Q demodulators and phase shifters**
- **Wideband analog-to-digital drivers**

FUNCTIONAL BLOCK DIAGRAM

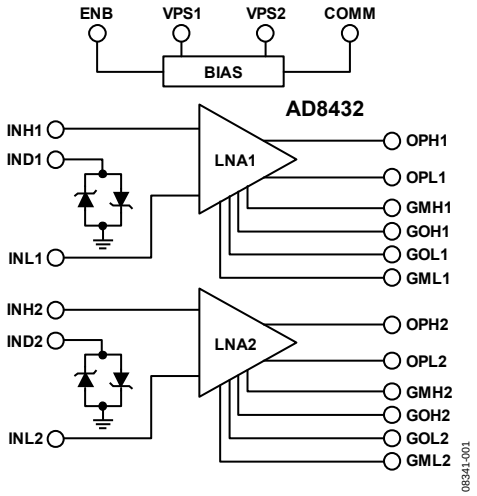


Figure 1.

GENERAL DESCRIPTION

The AD8432 is a dual-channel, low power, ultralow noise amplifier with selectable gain and active impedance matching. Each channel has a single-ended input, differential output, and integrated input clamps. By pin strapping the gain setting pins, four accurate gains of G = 12.04 dB, 18.06 dB, 21.58 dB, and 24.08 dB (×4, ×8, ×12, and ×16, respectively) are possible. A bandwidth of 200 MHz at G = 12.04 dB makes this amplifier well suited for many high speed applications.

The exceptional noise performance of the AD8432 is made possible by the active impedance matching. Using a feedback network, the input impedance of the amplifiers can be adjusted to match the signal source impedance without compromising the noise performance. Impedance matching and low noise in the AD8432 allow designers to create wider dynamic range systems that are able to detect even very low level signals.

The AD8432 achieves 0.85 nV/√Hz input-referred voltage noise for a gain of 12.04 dB. The AD8432's ultralow noise, low distortion, gain accuracy, and channel-to-channel matching are ideal for high performance ultrasound systems and for processing I/Q demodulator signals.

The AD8432 operates on a single supply of 5 V at 24 mA. It is available in a 4 mm × 4 mm, 24-lead LFSCP. The LFCSP features an exposed paddle that provides a low thermal resistance path to the PCB, which enables more efficient heat transfer and increases reliability. The operating temperature range is −40°C to +85°C.

Rev. D **Document Feedback**
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REVISION HISTORY

3/2017—Rev. C to Rev. D

Changed CP-24-7 to CP-24-15 ... Throughout
Changes to Outline Dimensions ... 29
Changes to Ordering Guide ... 29

7/2012—Rev. B to Rev. C

Changes to Figure 1 ... 1
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Deleted Gain Settings Section and Table 8 ... 25
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3/2011—Rev. A to Rev. B

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2/2010—Rev. 0 to Rev. A

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Added Figure 27, Figure 29, and Figure 31, Renumbered Sequentially ... 11
Added Figure 33 and Figure 35 ... 12
Changes to Figure 58 ... 16

10/2009—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, R_S = R_{IN} = 50 Ω, R_{FB} =150 Ω, C_{SH} = 47 pF, R_{SH} = 15 Ω, R_L = 500 Ω (per SE output), C_L = 5 pF (per SE output), G = 12.04 dB (single-ended input to differential output), f = 1 MHz, unless otherwise specified.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Gain Range	Input to differential output (selectable gain)	12.04		24.08	dB
	Input to single output (selectable gain)	6.02		18.06	dB
Gain Error			0.1	1	dB
−3 dB Small Signal Bandwidth	R_{IN} unterminated, R_{FB} = ∞, C_{SH} = 0 pF, R_{SH} = 0 Ω				
	G = 12.04 dB		200		MHz
	G = 18.06 dB		90		MHz
	G = 21.58 dB		50		MHz
	G = 24.08 dB		32		MHz
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p		42		MHz
Slew Rate (Rising Edge)	V_{OUT} = 2 V p-p, f = 10 MHz		295		V/µs
Slew Rate (Falling Edge)	V_{OUT} = 2 V p-p, f = 10 MHz		170		V/µs
Overdrive Recovery Time			10		ns
DISTORTION/NOISE PERFORMANCE					
Input Voltage Noise	R_{FB} = ∞		0.85		nV/√Hz
Input Current Noise	R_{FB} = ∞		2.0		pA/√Hz
Noise Figure					
Unterminated	R_S = 50 Ω, R_{FB} = ∞		2.8		dB
Active Termination	R_S = R_{IN} = 50 Ω, R_{FB} = 150 Ω		4.8		dB
	R_S = 50 Ω, R_{FB} = 226 Ω, R_{IN} = 75 Ω		4.2		dB
	R_S = 50 Ω, R_{FB} = 301 Ω, R_{IN} = 100 Ω		3.2		dB
	R_S = 50 Ω, R_{FB} = 619 Ω, R_{IN} = 200 Ω		2.1		dB
	R_S = 50 Ω, R_{FB} = 3.57 kΩ, R_{IN} = 1 kΩ		2.3		dB
Output Referred Noise	G = 12.04 dB, R_{FB} = ∞		3.4		nV/√Hz
	G = 18.06 dB, R_{FB} = ∞		6.8		nV/√Hz
	G = 21.58 dB, R_{FB} = ∞		10.2		nV/√Hz
	G = 24.08 dB, R_{FB} = ∞		13.6		nV/√Hz
Harmonic Distortion					
1 MHz (V_{OUT} = 1 V p-p)	HD2		−67		dBc
	HD2, R_S = 50 Ω, R_{IN} unterminated		−74		dBc
	HD3		−103		dBc
	HD3, R_S = 50 Ω, R_{IN} unterminated		−106		dBc
1 MHz (V_{OUT} = 2 V p-p)	HD2		−65		dBc
	HD2, R_S = 50 Ω, R_{IN} unterminated		−72		dBc
	HD3		−103		dBc
	HD3, R_S = 50 Ω, R_{IN} unterminated		−92		dBc
10 MHz (V_{OUT} = 1 V p-p)	HD2		−66		dBc
	HD2, R_S = 50 Ω, R_{IN} unterminated		−62		dBc
	HD3		−78		dBc
	HD3, R_S = 50 Ω, R_{IN} unterminated		−73		dBc
10 MHz (V_{OUT} = 2 V p-p)	HD2		−60		dBc
	HD2, R_S = 50 Ω, R_{IN} unterminated		−56		dBc
	HD3		−72		dBc
	HD3, R_S = 50 Ω, R_{IN} unterminated		−65		dBc

Parameter	Conditions	Min	Typ	Max	Unit
Two-Tone IMD3 Distortion	R_S = 50 Ω, R_{IN} unterminated				
10 MHz	V_{OUT} = 1 V p-p, f1 = 9.5 MHz, f2 = 10.5 MHz		−89.1		dBc
	V_{OUT} = 2 V p-p, f1 = 9.5 MHz, f2 = 10.5 MHz		−66.0		dBc
1 MHz	V_{OUT} = 1 V p-p, f1 = 0.9 MHz, f2 = 1.1 MHz		−88.9		dBc
	V_{OUT} = 2 V p-p, f1 = 0.9 MHz, f2 = 1.1 MHz		−73.7		dBc
Input 1dB Compression Point	f = 1 MHz		7.5		dBm
	f = 10 MHz		7.7		dBm
Output Third-Order Intercept					
1 MHz	V_{OUT} = 1 V p-p of composite tones		29.7		dBV rms
	V_{OUT} = 2 V p-p of composite tones		28.2		dBV rms
10 MHz	V_{OUT} = 1 V p-p of composite tones		23.2		dBV rms
	V_{OUT} = 2 V p-p of composite tones		24.2		dBV rms
1 MHz	V_{OUT} = 1 V p-p of composite tones, reference to 50 Ω		42.7		dBm
	V_{OUT} = 2 V p-p of composite tones, reference to 50 Ω		41.2		dBm
10 MHz	V_{OUT} = 1 V p-p of composite tones, reference to 50 Ω		36.2		dBm
	V_{OUT} = 2 V p-p of composite tones, reference to 50 Ω		37.2		dBm
Crosstalk	V_{OUT} = 1 V p-p, f = 1 MHz		102		dB
DC PERFORMANCE					
Input Offset Voltage		−6.25	+1	+6.25	mV
Input Offset Voltage Drift			300		µV/°C
INPUT CHARACTERISTICS					
Input Voltage Range	AC-coupled		1.2		V p-p
Input Resistance	R_{FB} = 150 Ω		50		Ω
	R_{FB} = 226 Ω		75		Ω
	R_{FB} = 301 Ω		100		Ω
	R_{FB} = 619 Ω		200		Ω
	R_{FB} = 3.57 kΩ		1		kΩ
	R_{FB} = ∞, f = 100 kHz		6.2		kΩ
Input Capacitance			6		pF
Input Common-Mode Voltage			3.25		V
OUTPUT CHARACTERISTCS					
Output Common-Mode Voltage			2.5		V
Output Offset Voltage		−25	+4	+25	mV
Output Voltage Swing			4.8		V p-p
Output Resistance	Single-ended, either output		<0.1		Ω
Output Resistance in Shutdown Mode	Single-ended, either output		2.5		kΩ
Output Short-Circuit Current	R_L = 10 Ω differential		77		mA
Enable Response Time	ENB_{ON} (enable high to output on)		200		µs
	ENB_{OFF} (enable low to output off)		200		µs
POWER SUPPLY					
Supply Voltage		4.5	5	5.5	V
Quiescent Current	ENB = 5 V		24		mA
Over Temperature	T_A = −40°C		21		mA
	T_A = +85°C		27		mA
Supply Current in Shutdown Mode	ENB = GND		50	100	µA
Power Dissipation			120		mW
PSRR	G = 24.08 dB, f = 100 kHz, no bypass capacitors		−82		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltage	
Supply Voltage	5.5 V
Input Voltage	0 V to VPS
Power Dissipation	120 mW
Temperature	
Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Package Glass Transition Temperature (T_G)	150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} value in Table 3 assumes a 4-layer JEDEC standard board with zero airflow.

Table 3. Thermal Resistance[1]

Parameter	θ_{JA}	θ_{JC}	θ_{JB}	Ψ_{JT}	Unit
40-Lead LFCSP	57.9	11.2	35.9	1.1	°C/W

[1] 4-layer JEDEC board (2S2P).

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8432 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 150°C for an extended period can cause changes in silicon devices, potentially resulting in a loss of functionality.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

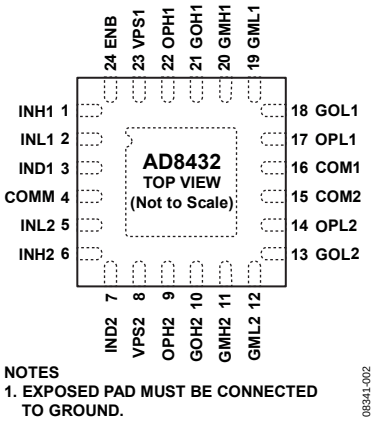


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INH1	LNA1 Noninverting Input.
2	INL1	LNA1 Inverting Input (AC-Coupled to Ground).
3, 7	IND1, IND2	Integrated Input Clamping Back-to-Back Diodes.
4	COMM	Input Ground.
5	INL2	LNA2 Inverting Input (AC-Coupled to Ground).
6	INH2	LNA2 Noninverting Input.
8	VPS2	5 V Supply.
9	OPH2	Noninverting Output of LNA2.
10	GOH2	Gain Setting Pin for LNA2.
11	GMH2	Gain Setting Pin for LNA2.
12	GML2	Gain Setting Pin for LNA2.
13	GOL2	Gain Setting Pin for LNA2.
14	OPL2	Inverting Output of LNA2.
15	COM2	LNA2 Output Ground.
16	COM1	LNA1 Output Ground.
17	OPL1	Inverting Output of LNA1.
18	GOL1	Gain Setting Pin for LNA1.
19	GML1	Gain Setting Pin for LNA1.
20	GMH1	Gain Setting Pin for LNA1.
21	GOH1	Gain Setting Pin for LNA1.
22	OPH1	Noninverting Output of LNA1.
23	VPS1	5 V Supply.
24	ENB	Enable.
	EPAD	Exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, R_S = R_{IN} = 50 Ω, R_{FB} =150 Ω, C_{SH} = 47 pF, R_{SH} = 15 Ω, R_L =500 Ω (per SE output), C_L = 5 pF (per SE output), G = 12.04 dB (single-ended input to differential output), f = 1 MHz, unless otherwise specified.

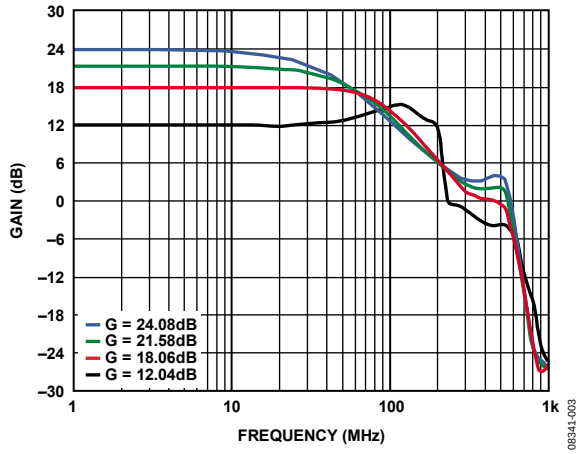


Figure 3. Small Signal Differential Gain vs. Frequency, R_{IN} Unterminated

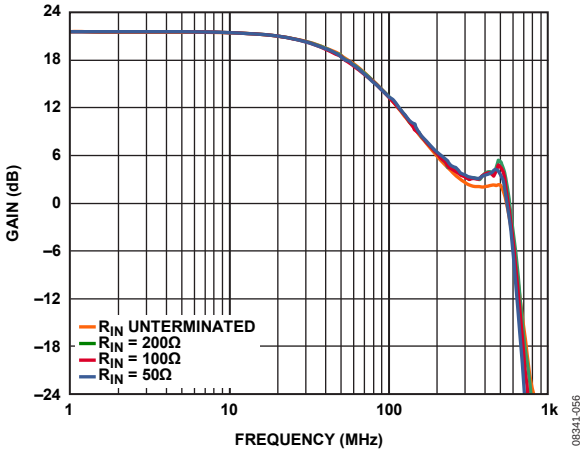


Figure 6. Small Signal Frequency Response vs. R_{IN}, G = 21.58 dB

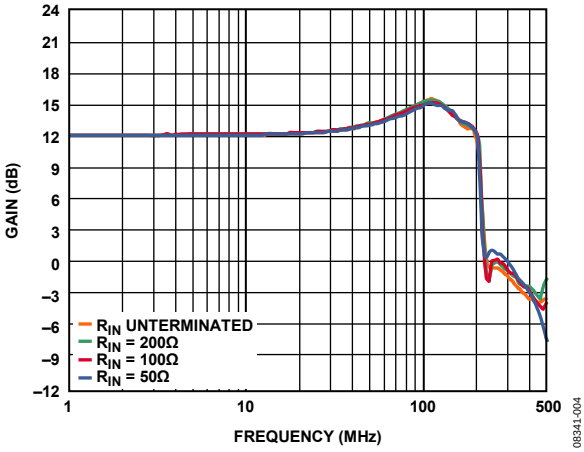


Figure 4. Small Signal Frequency Response vs. R_{IN}, G = 12.04 dB

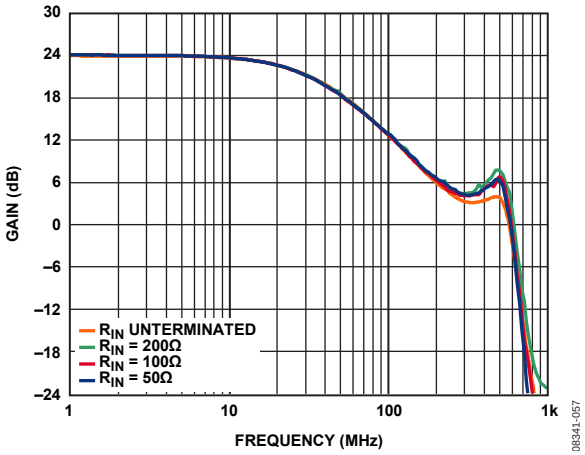


Figure 7. Small Signal Frequency Response vs. R_{IN}, G = 24.08 dB

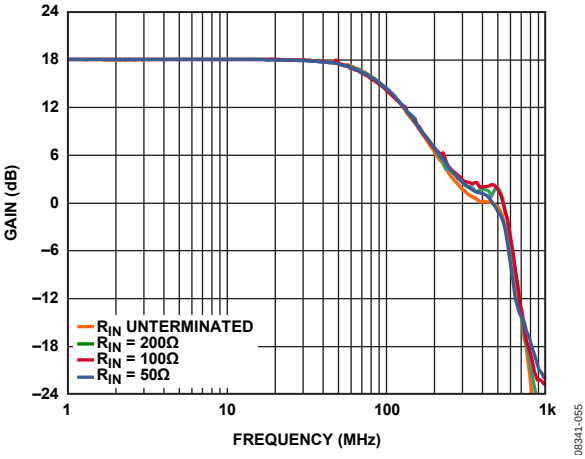


Figure 5. Small Signal Frequency Response vs. R_{IN}, G = 18.06 dB

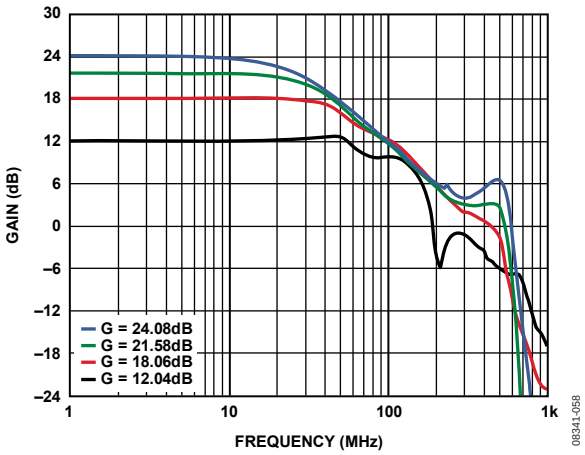


Figure 8. Differential Gain vs. Frequency, V_{OUT} = 1 V p-p, R_{IN} = 50 Ω

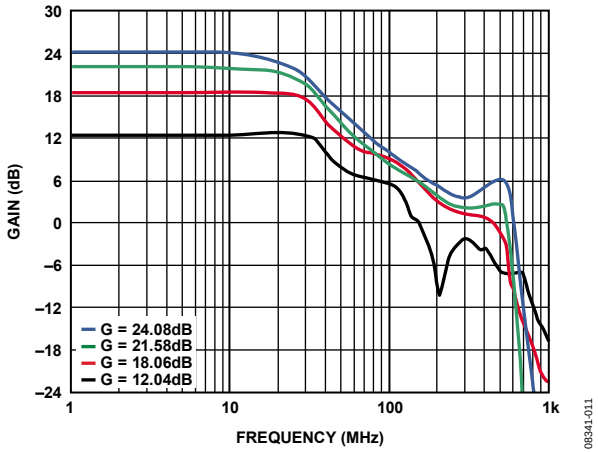


Figure 9. Differential Gain vs. Frequency, V_{OUT} = 2 V p-p, R_{IN} = 50 Ω

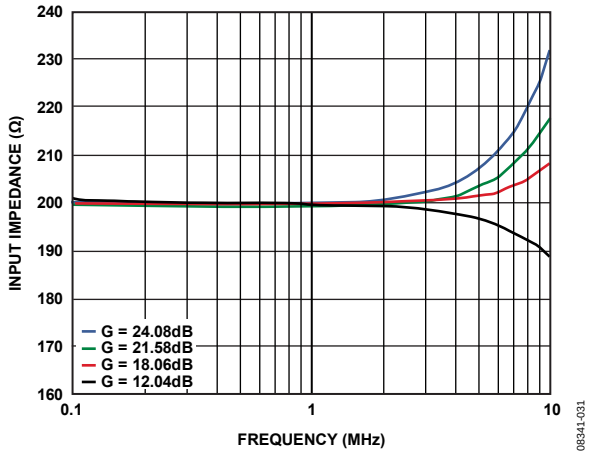


Figure 12. Input Impedance R_{IN} vs. Frequency, 200 Ω Active Termination

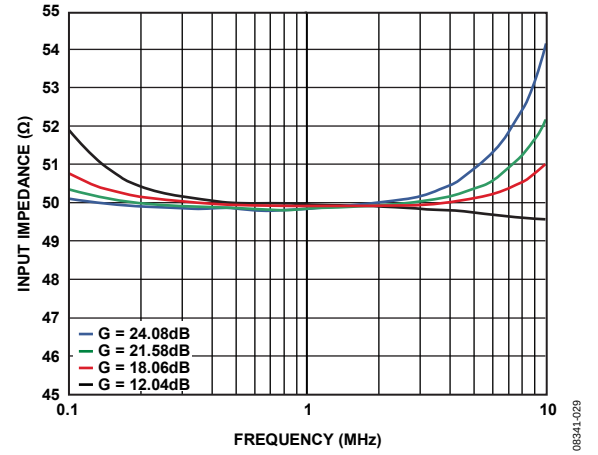


Figure 10. Input Impedance R_{IN} vs. Frequency, 50 Ω Active Termination

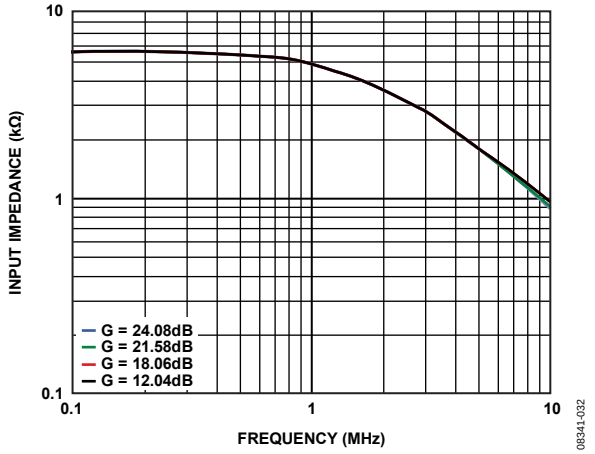


Figure 13. Input Impedance R_{IN} vs. Frequency, Unterminated

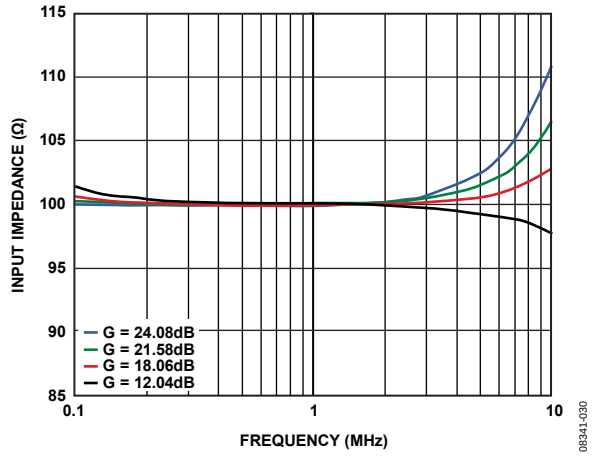


Figure 11. Input Impedance R_{IN} vs. Frequency, 100 Ω Active Termination

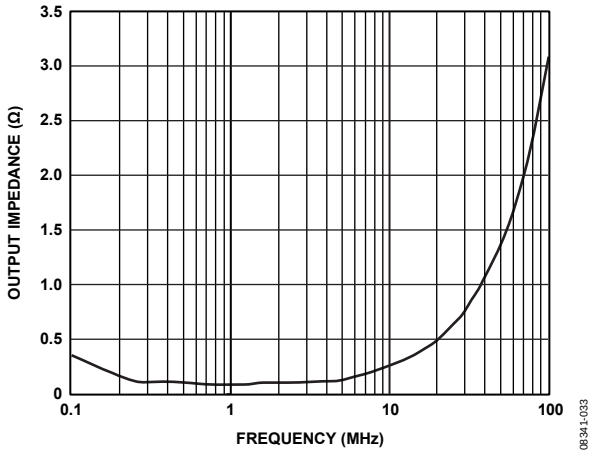


Figure 14. Output Impedance vs. Frequency

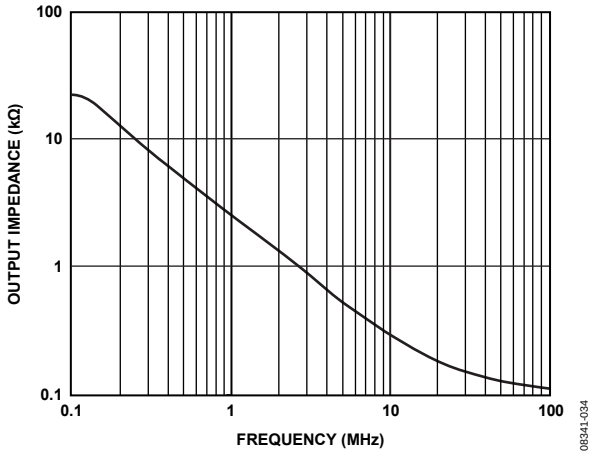


Figure 15. Output Impedance vs. Frequency in Disable Mode

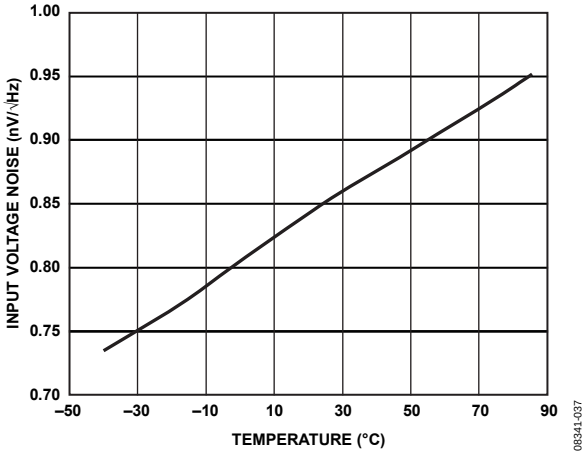


Figure 18. Input Voltage Noise vs. Temperature

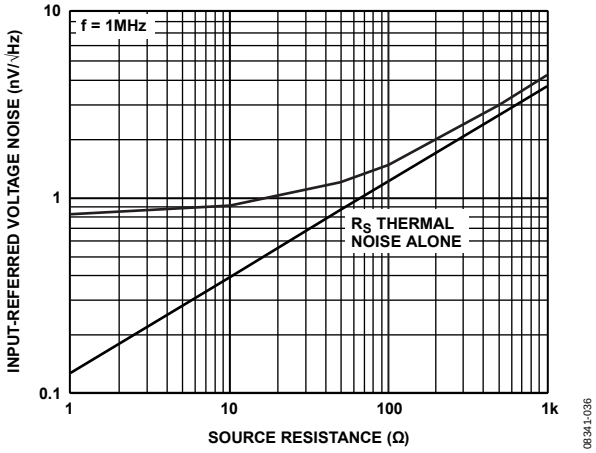


Figure 16. Input-Referred Voltage Noise vs. Source Resistance (R_S)

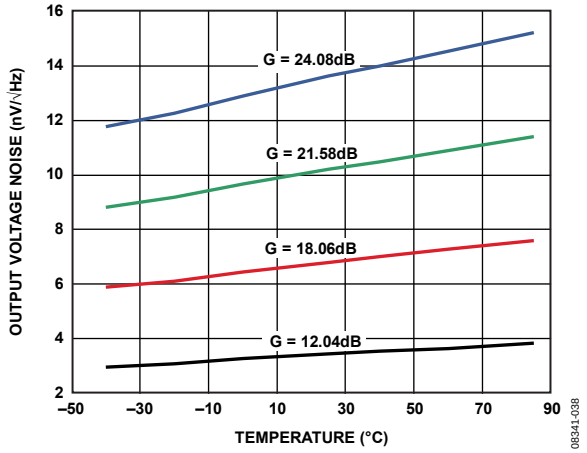


Figure 19. Output Voltage Noise vs. Temperature

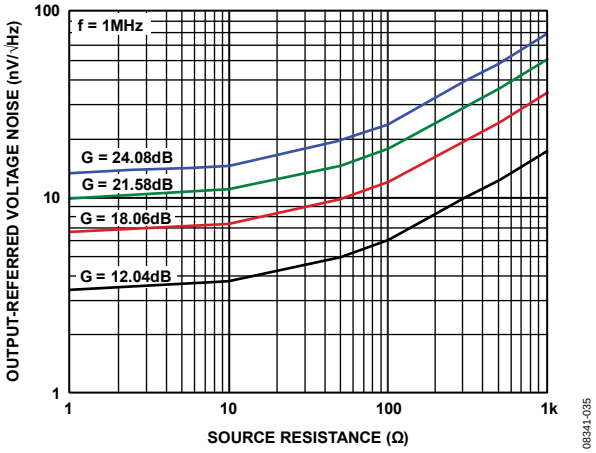


Figure 17. Output-Referred Voltage Noise vs. Source Resistance (R_S)

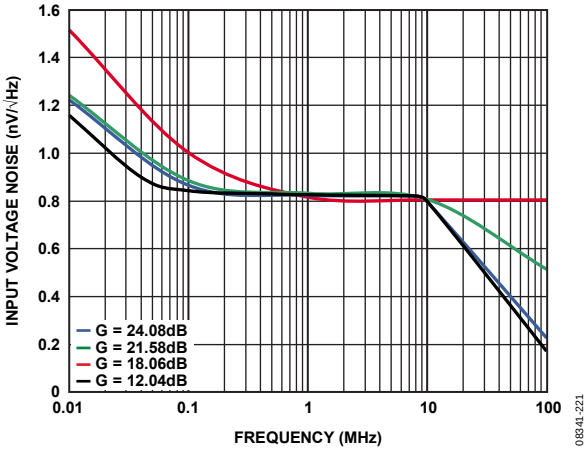


Figure 20. Input Voltage Noise vs. Frequency

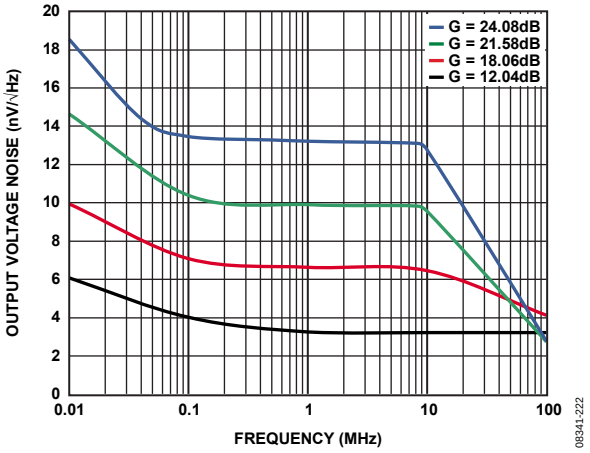


Figure 21. Output Voltage Noise vs. Frequency

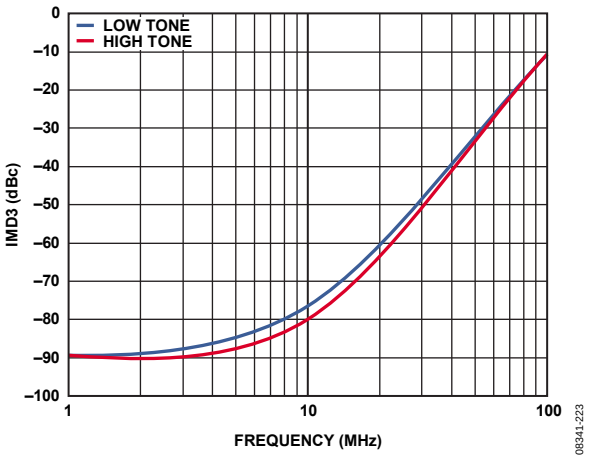


Figure 22. IMD3 vs. Frequency

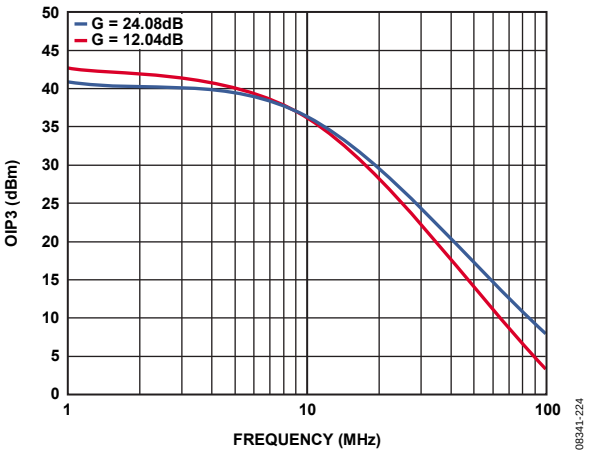


Figure 23. Output Third-Order Intercept vs. Frequency

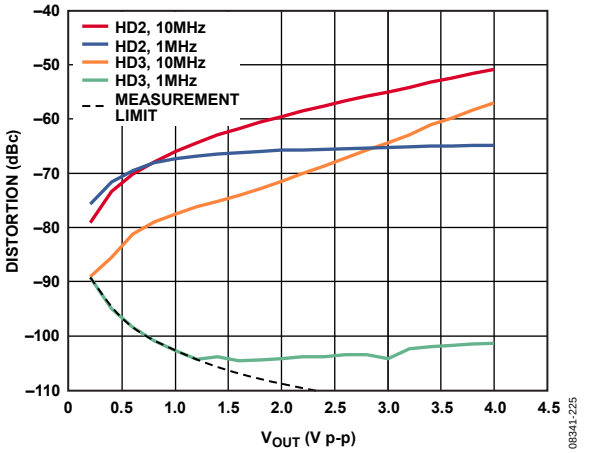


Figure 24. Harmonic Distortion vs. Differential Output Voltage, G = 12.04 dB

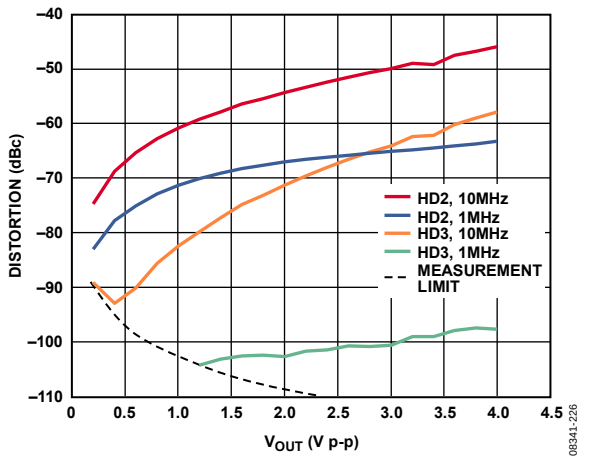


Figure 25. Harmonic Distortion vs. Differential Output Voltage, G = 24.08 dB

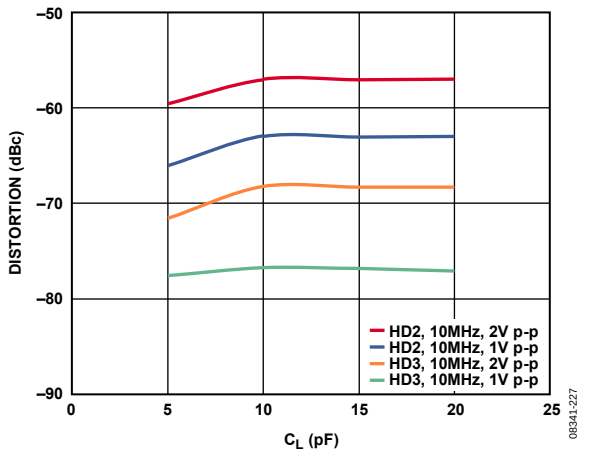


Figure 26. Harmonic Distortion at 10 MHz vs. Capacitive Load (C_L), G = 12.04 dB

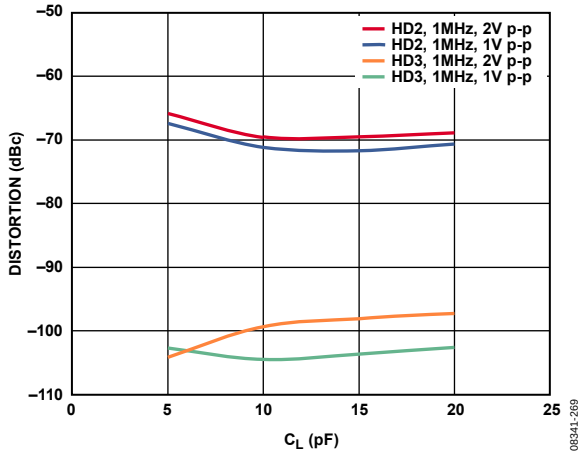


Figure 27. Harmonic Distortion at 1 MHz vs. Capacitive Load (C_L), G = 12.04 dB

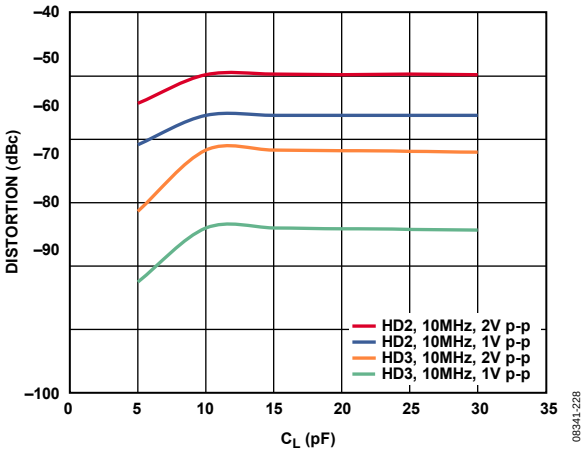


Figure 28. Harmonic Distortion at 10 MHz vs. Capacitive Load (C_L), G = 24.08 dB

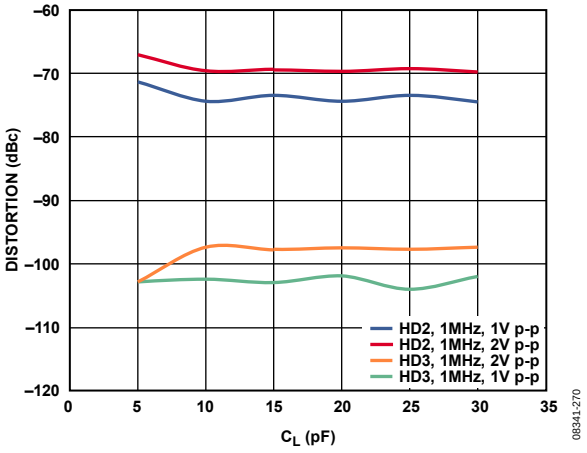


Figure 29. Harmonic Distortion at 1 MHz vs. Capacitive Load (C_L), G = 24.08 dB

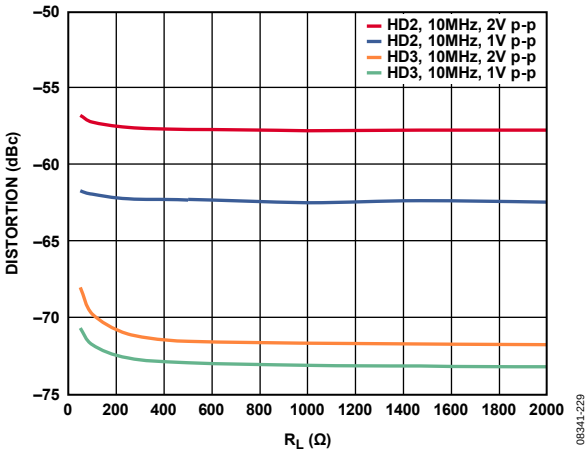


Figure 30. Harmonic Distortion at 10 MHz vs. Resistive Load (R_L), G = 12.04 dB

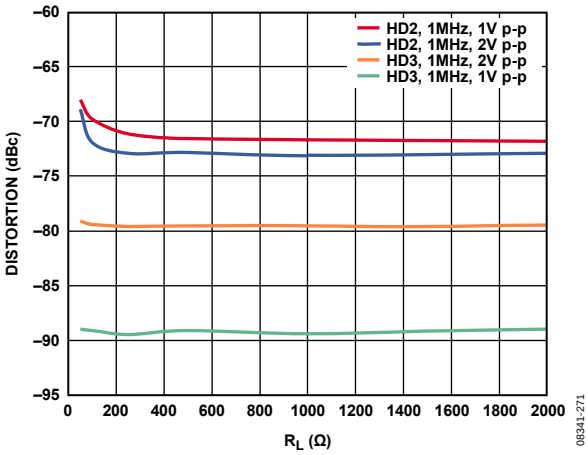


Figure 31. Harmonic Distortion at 1 MHz vs. Resistive Load (R_L), G = 12.04 dB

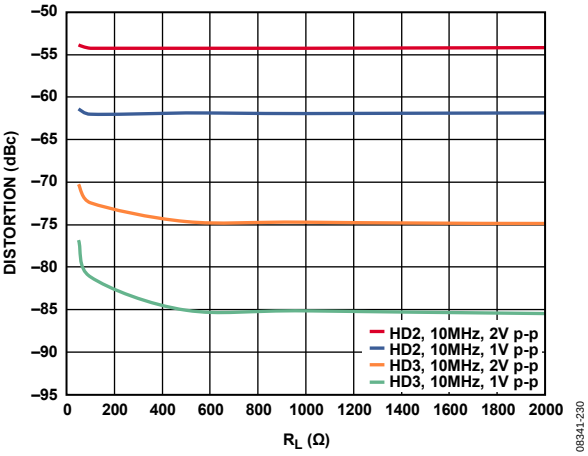


Figure 32. Harmonic Distortion at 10 MHz vs. Resistive Load (R_L), G = 24.08 dB

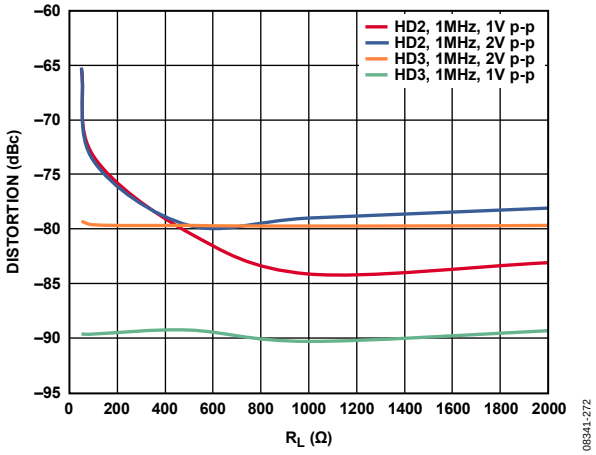


Figure 33. Harmonic Distortion at 1 MHz vs. Resistive Load (R_L), G = 24.08 dB

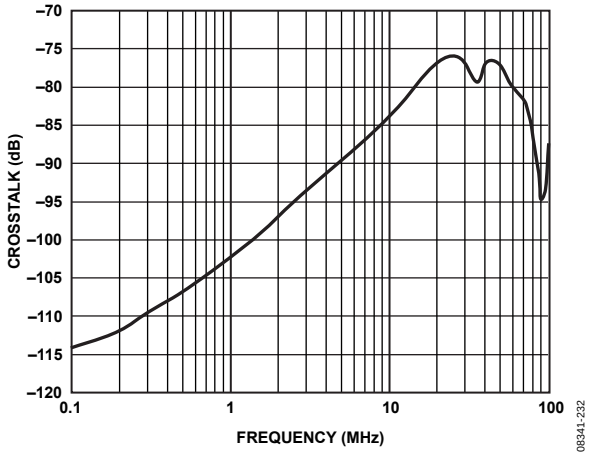


Figure 36. Channel Crosstalk vs. Frequency

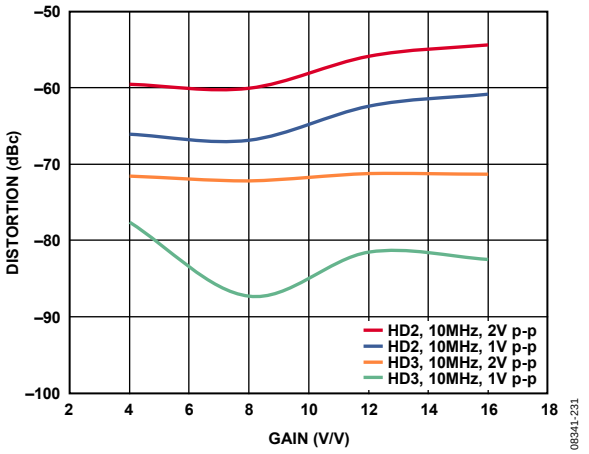


Figure 34. Harmonic Distortion at 10 MHz vs. Gain

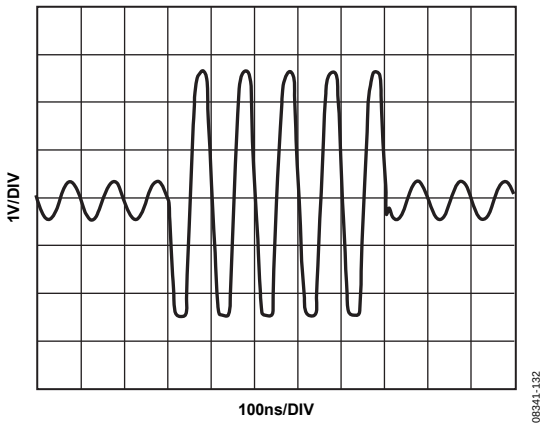


Figure 37. Overdrive Recovery, G = 12.04 dB

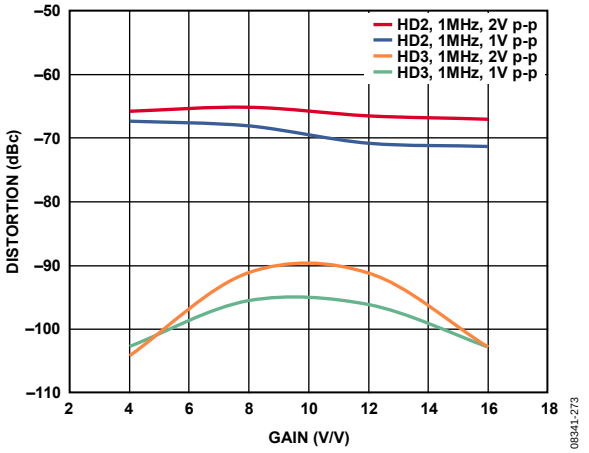


Figure 35. Harmonic Distortion at 1 MHz vs. Gain

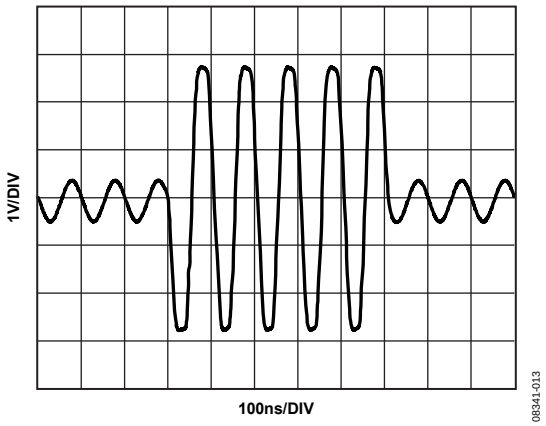


Figure 38. Overdrive Recovery, G = 24.08 dB

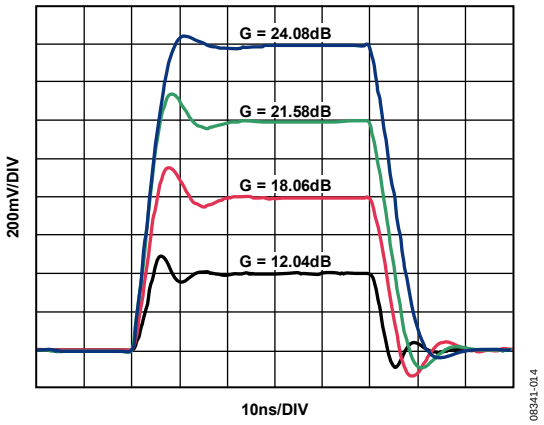


Figure 39. Small Signal Transient Response vs. Gain, V_{IN} = 100 mV p-p

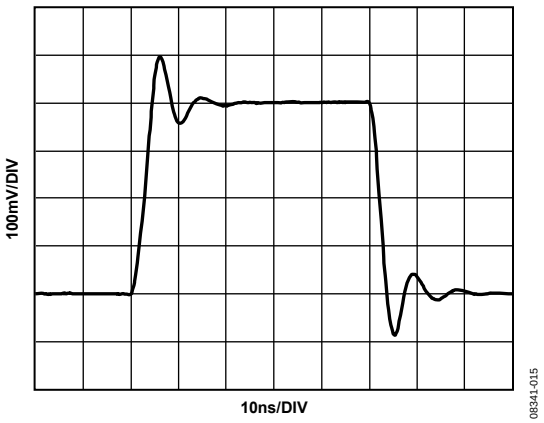


Figure 40. Small Signal Transient Response, G = 12.04 dB

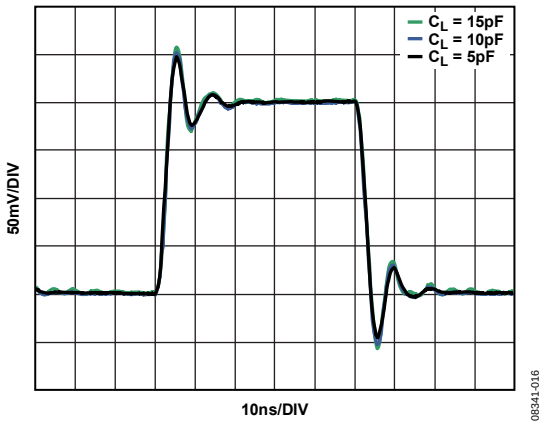


Figure 41. Small Signal Transient Response vs. Capacitive Load (C_L), G = 12.04 dB

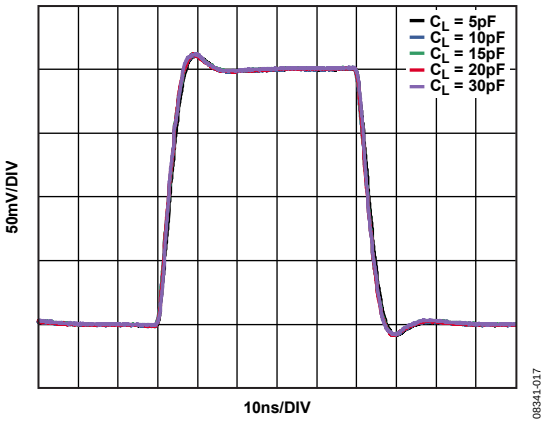


Figure 42. Small Signal Transient Response vs. Capacitive Load (C_L), G = 24.08 dB

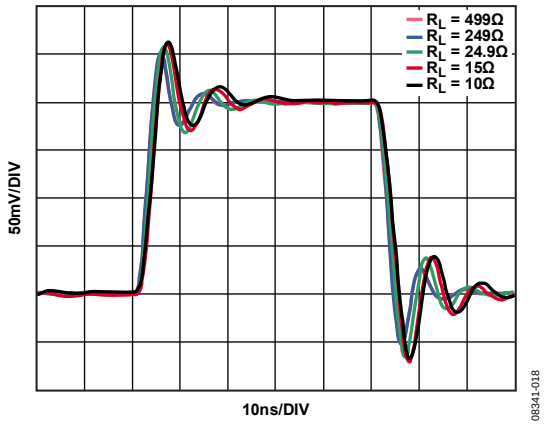


Figure 43. Small Signal Transient Response vs. Resistive Load (R_L), G = 12.04 dB

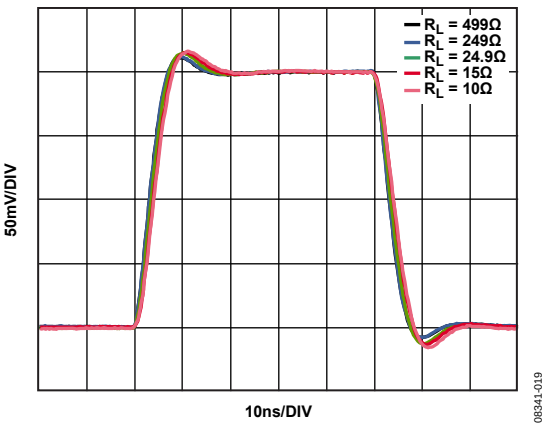


Figure 44. Small Signal Transient Response vs. Resistive Load (R_L), G = 24.08 dB

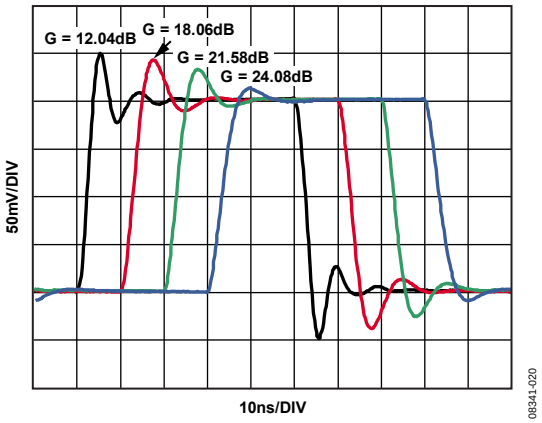


Figure 45. Small Signal Transient Response vs. Gain, V_{OUT} = 200 mV p-p

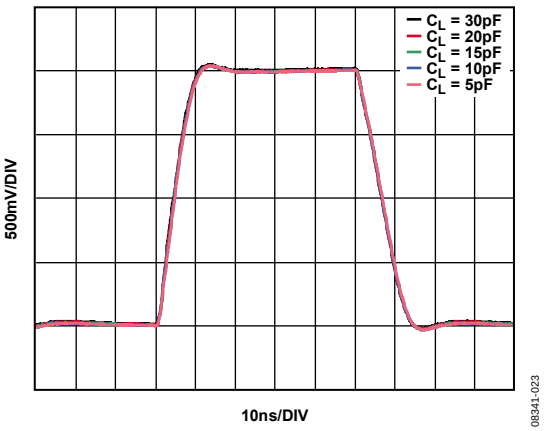


Figure 48. Large Signal Transient Response vs. Capacitive Load (C_L), G = 24.08 dB

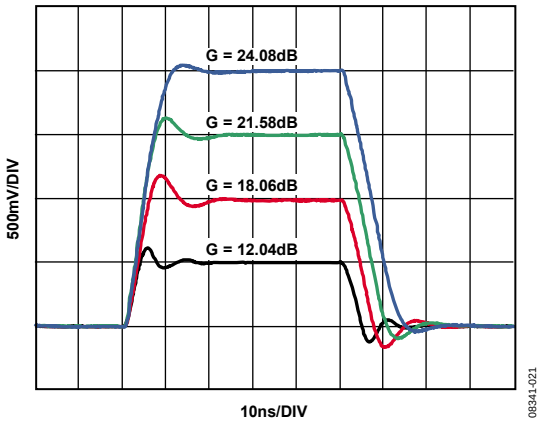


Figure 46. Large Signal Transient Response vs. Gain, V_{IN} = 125 mV p-p

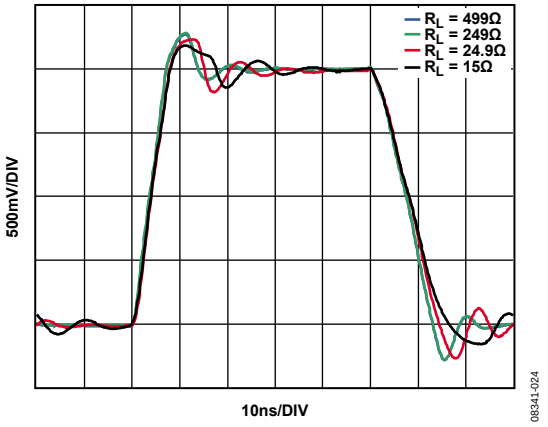


Figure 49. Large Signal Transient Response vs. Resistive Load (R_L), G = 12.04 dB

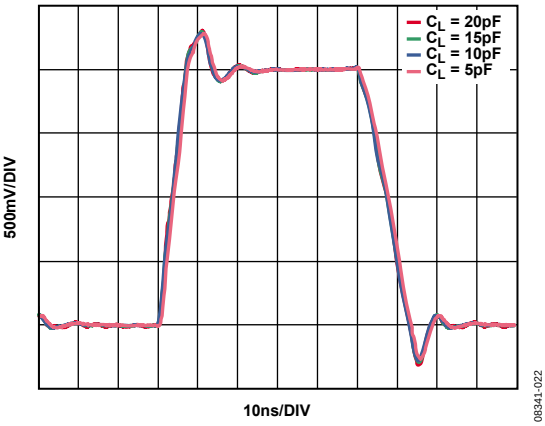


Figure 47. Large Signal Transient Response vs. Capacitive Load (C_L), G = 12.04 dB

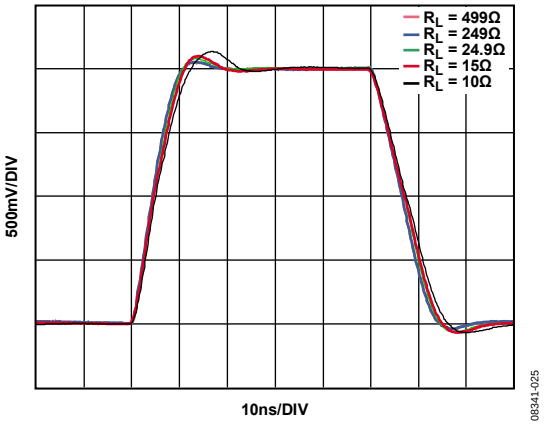


Figure 50. Large Signal Transient Response vs. Resistive Load (R_L), G = 24.08 dB

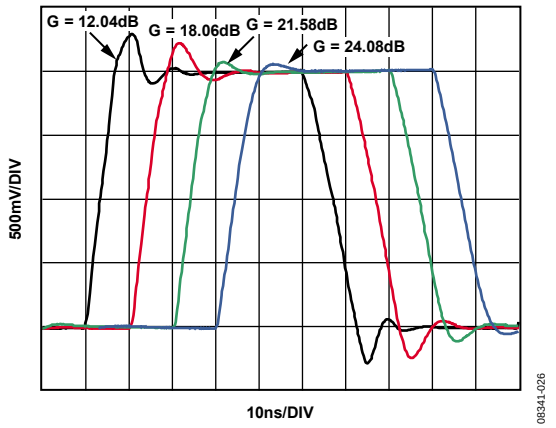


Figure 51. Large Signal Transient Response vs. Gain, V_{OUT} = 2 V p-p

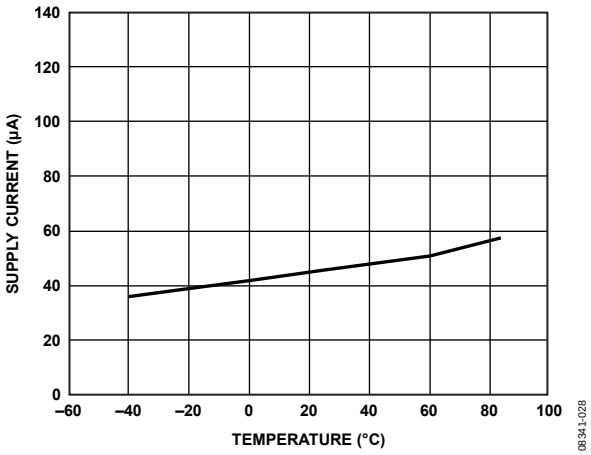


Figure 54. Supply Current vs. Temperature in Disable Mode

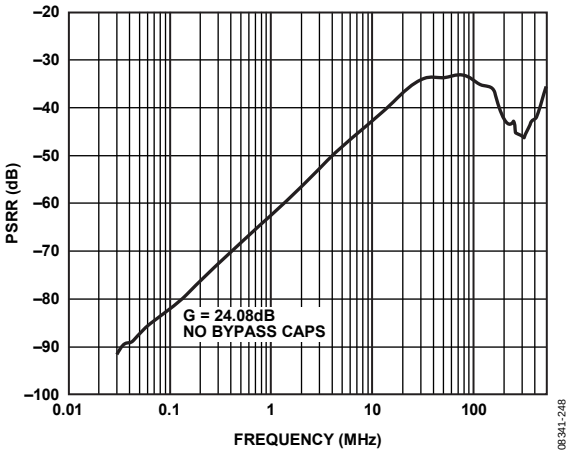


Figure 52. PSRR vs. Frequency

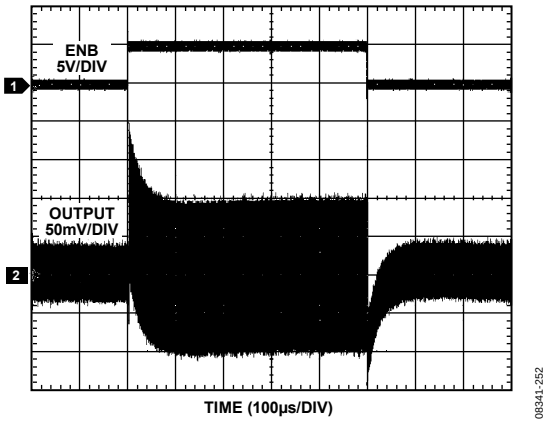


Figure 55. Small Signal Enable Response

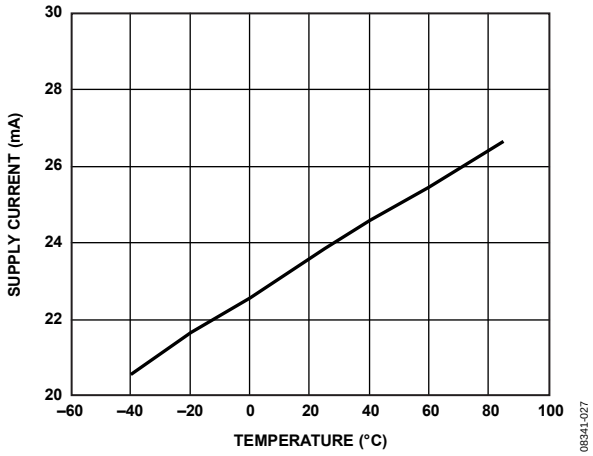


Figure 53. Supply Current vs. Temperature

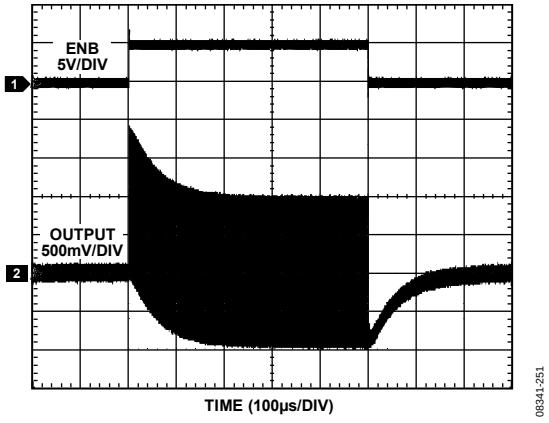


Figure 56. Large Signal Enable Response

TEST CIRCUITS

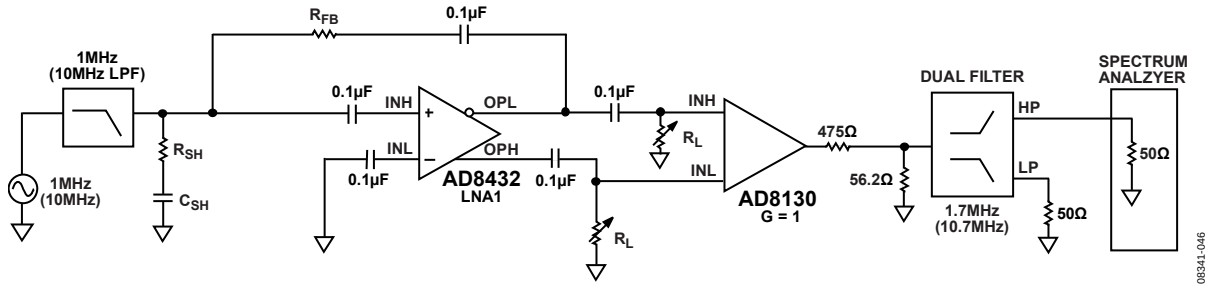


Figure 57. Harmonic Distortion vs. Resistive Load (R_L) Measurements

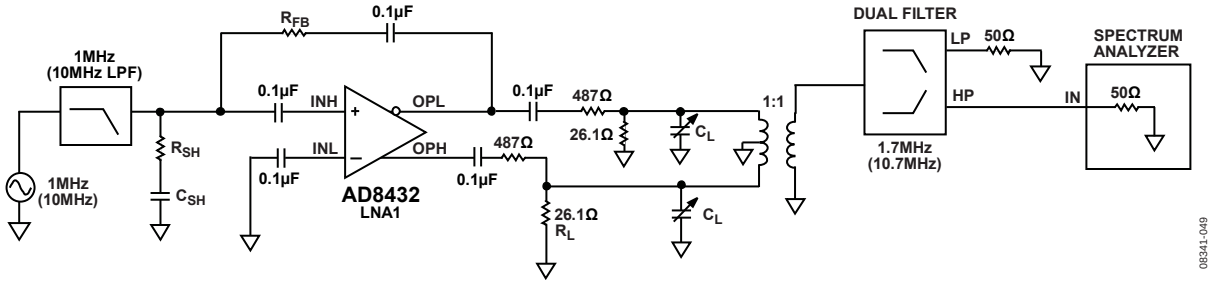


Figure 58. Harmonic Distortion vs. Capacitive Load (C_L) Measurements

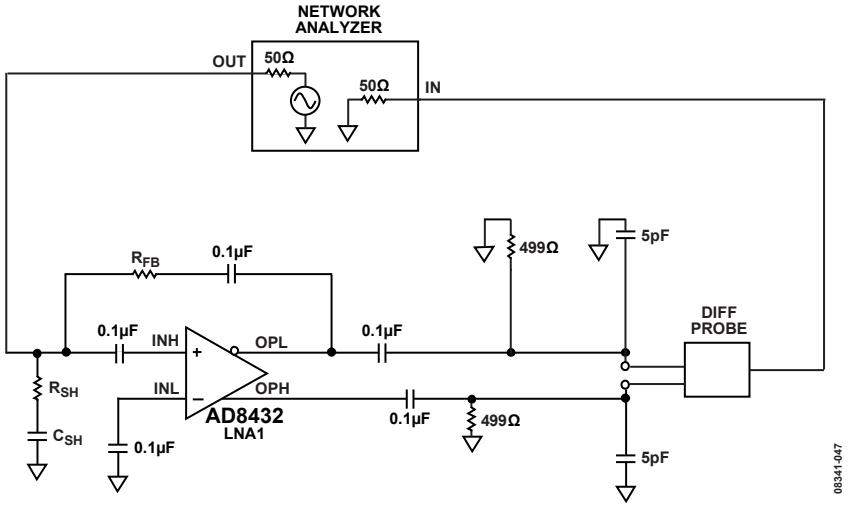


Figure 59. Frequency Response Measurements

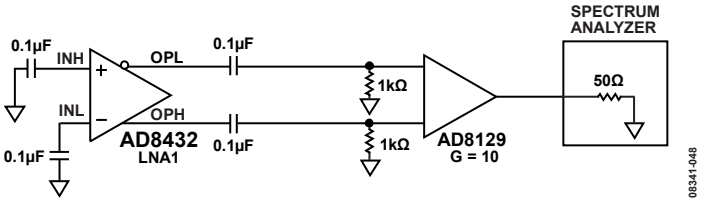


Figure 60. Voltage Noise Measurements

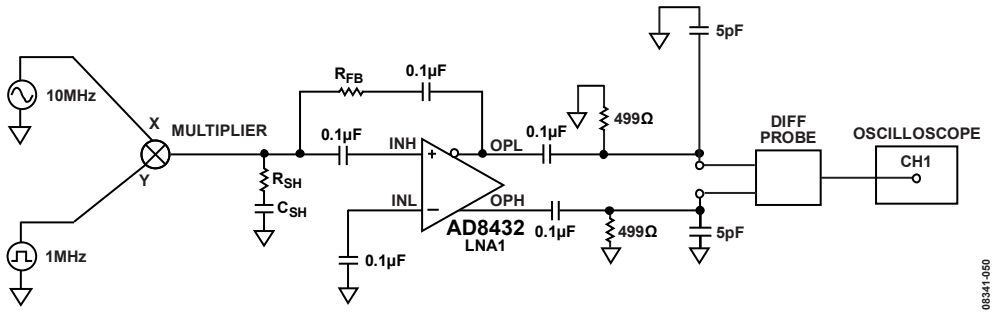


Figure 61. Overdrive Recovery Measurements

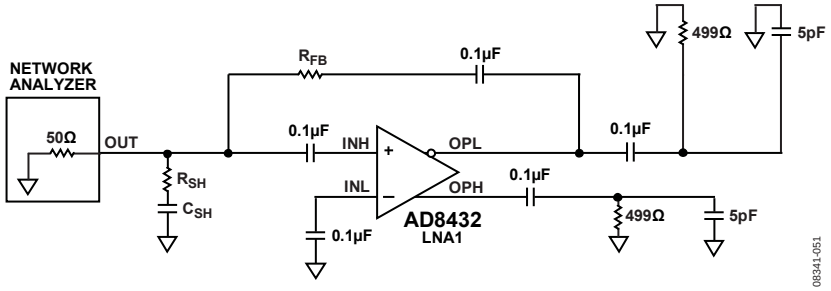


Figure 62. Input Impedance vs. Frequency Measurements

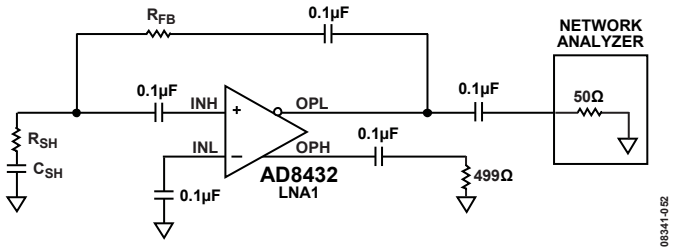


Figure 63. Output Impedance vs. Frequency Measurements

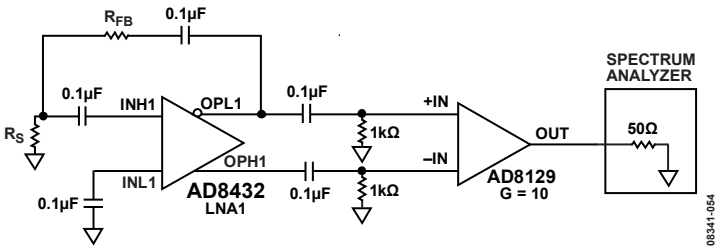


Figure 64. Noise Figure Measurements

THEORY OF OPERATION

LOW NOISE AMPLIFIER (LNA)

The AD8432 is a dual-channel, ultralow noise amplifier with integrated pin-strappable, gain-setting resistors. The resistors can be externally connected to achieve differential gains of 12.04 dB, 18.06 dB, 21.58 dB, and 24.08 dB (×4, ×8, ×12, and ×16, respectively). A simplified schematic of an LNA is shown in Figure 65.

The LNA is driven with a single-ended input and measured differentially at the output. The inverting input INL must be ac-coupled to ground through a capacitor for proper operation. The LNA cannot be driven differentially due to the asymmetry of the internal gain setting resistors. The gain from the inverting input INL to the single-ended output (OPH or OPL) does not match the gain from the noninverting input INH to the single-ended output.

The AD8432 inputs have a dc bias voltage of 3.25 V, which is generated internally. The inputs must be ac-coupled through a series capacitor to maintain the dc bias level of the inputs. Likewise, the AD8432 outputs have a dc bias voltage of 2.5 V. An ac coupling capacitor in series with each single-ended output is recommended to prevent improper loading of the outputs. The AD8432 inputs have a dc bias voltage of 3.25 V, which is generated internally. The inputs must be ac-coupled through a series capacitor to maintain the dc bias level of the inputs (see CINL and CINH in Figure 65).

The AD8432 supports a differential output voltage of 4.8 V p-p for the common-mode output voltage of 2.5 V. Therefore, for a differential gain of G = 12.04 dB, the maximum input voltage allowed is 1.2 V p-p.

Clamping the inputs ensures quick recovery from large input voltages. The input back-to-back diodes, which are integrated inside the die (IND1 and IND2), should be used for the lowest gain configuration (12.04 dB) to protect the input from overdriving. They should be connected after the source resistance or before the INH coupling capacitor.

The use of a fully differential topology and negative feedback minimizes distortion. A differential signal enables smaller swings at each output, which results in reduction of third-order distortion.

The AD8432 is a voltage feedback amplifier. Due to gain bandwidth product (GBW), a decrease in bandwidth should be expected as the gain increases. Table 5 displays the values of the −3 dB bandwidth for each gain with unterminated input impedance.

GAIN SETTING TECHNIQUE

Pin strapping is used to set the gain of the amplifier. Gain setting resistors are integrated in the LNA and are accessible externally through the GOH, GMH, GML, and GOL pins. By externally shorting these pins, and thereby shorting or connecting the internal resistors, the AD8432 can be configured for four different gains. Table 5 shows which pins must be connected to achieve the desired gain.

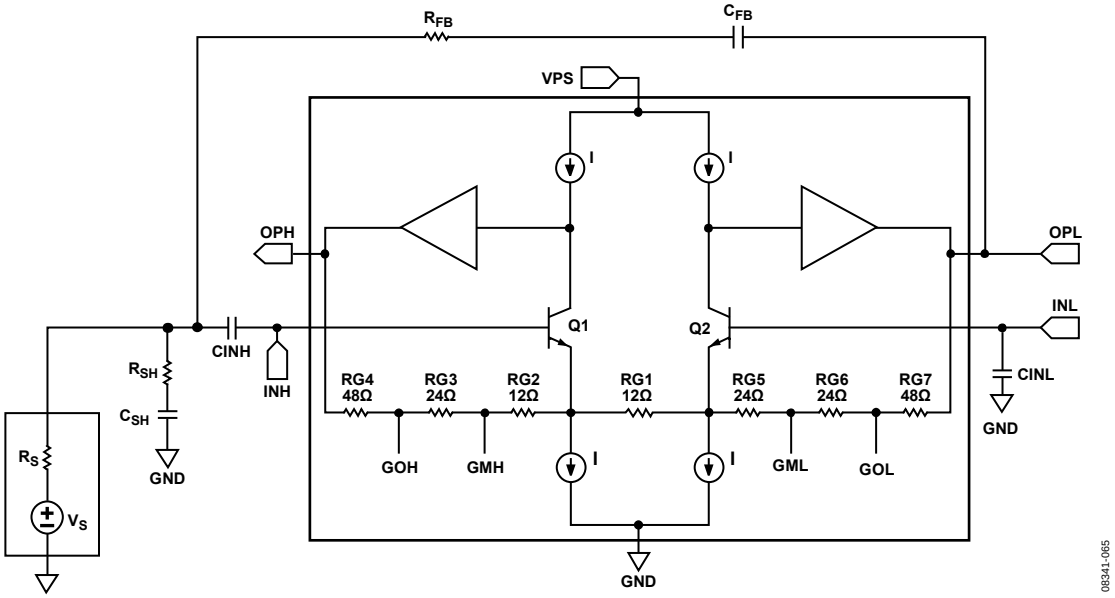


Figure 65. Simplified Schematic of a Single LNA Channel, Including External Shunt and Feedback Components

Table 5. Gain Setting Using a Pin-Strapping Technique and −3 dB Bandwidth for Each Gain Configuration

Differential Gain (dB)	Single Gain (dB)	−3 dB BW (MHz)	RG1 (Ω)	RG2 (Ω)	RG3 (Ω)	RG4 (Ω)	RG5 (Ω)	RG6 (Ω)	RG7 (Ω)
12.04	6.02	200	12	12	Connect GMH to GOH	Connect GOH to OPH	24	Connect GML to GOL	Connect GOL to OPL
18.06	12.04	90	12	12	24	Connect GOH to OPH	24	24	Connect GOL to OPL
21.58	15.56	50	12	12	Connect GMH to GOH	48	24	Connect GML to GOL	48
24.08	18.06	32	12	12	24	48	24	24	48

The single-ended gain from INH to OPH (see Figure 65) is defined as

$$G_{OPH-INH} = \frac{R_{G1} + R_{G2} + R_{G3} + R_{G4}}{R_{G1}}$$

The single-ended gain from INH to OPL is defined as

$$G_{OPL-INH} = -\frac{R_{G5} + R_{G6} + R_{G7}}{R_{G1}}$$

The values of the seven gain resistors were chosen so that both single-ended gains are equal. For example, to set a gain of 12.04 dB (G = ×4) differentially, the gain from INH to each output (OPH, OPL) should be 6.02 dB (G = ×2).

INH to OPH: For $R_{G1} = R_{G2} = R_G$, then

$$G_{OPH-INH} = \frac{R_{G1} + R_{G2}}{R_{G1}} = \frac{2 \times R_G}{R_G} = 2$$

INH to OPL: For $R_{G1} = R_G$ and $R_{G5} = 2 \times R_G$, then

$$G_{OPL-INH} = -\frac{R_{G5}}{R_{G1}} = -\frac{2 \times R_G}{R_G} = -2$$

ACTIVE INPUT RESISTANCE MATCHING

The AD8432 reduces noise and optimizes signal power transfer by using active input termination to perform signal source resistance matching.

The primary purpose of input impedance matching is to optimize the input signal power transfer. With resistive termination, the input noise increases due to the thermal noise of the terminating resistor and the increased contribution of the input voltage noise generator of the LNA. With active impedance matching, however, the contributions of both are smaller than they are for resistive termination by a factor of 1/(1 + ½ LNA) gain. The noise figure (NF) for the three terminating schemes is shown in Figure 67.

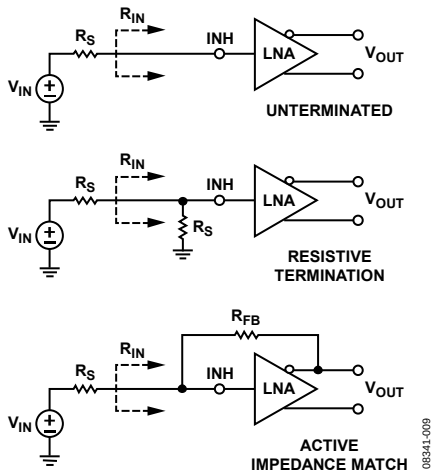


Figure 66. Input Resistance Matching

To achieve this active impedance match, connect a feedback resistor, R_{FB}, between the INH and OPL (see Figure 66). R_{IN} is given in Equation 1, where G/2 is the single-ended gain.

$$R_{IN} = \frac{R_{FB}}{1 + \frac{G}{2}} \quad (1)$$

In addition, to further reduce the input resistance, there is an internal resistance of 6.2 kΩ in parallel with the source resistance, such that

$$R_{IN} = \frac{R_{FB}}{1 + \frac{G}{2}} \| R_{INTERNAL} \quad (2)$$

Equation 3 should be used to calculate R_{FB} accurately for a desired input resistance and single-ended gain. Refer to Table 6 for calculated results for R_{FB} for several input resistance and gain combinations.

$$\Rightarrow R_{FB} = \frac{R_{IN}\left(1 + \frac{G}{2}\right)}{1 - \frac{R_{IN}}{R_{INTERNAL}}},\ R_{INTERNAL} = 6.2\ \text{k}\Omega \quad (3)$$

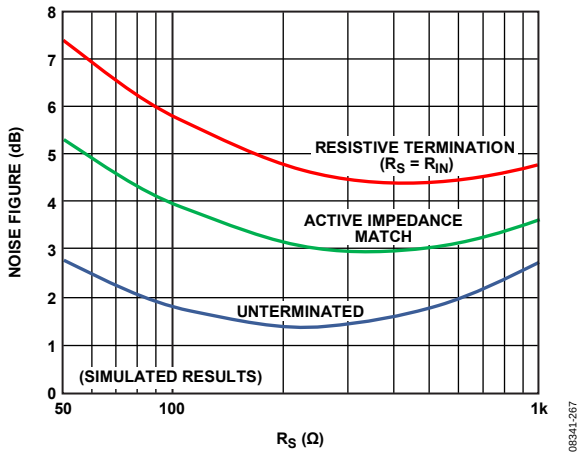


Figure 67. Noise Figure vs. R_S for Resistive, Active Match, and Unterminated Inputs

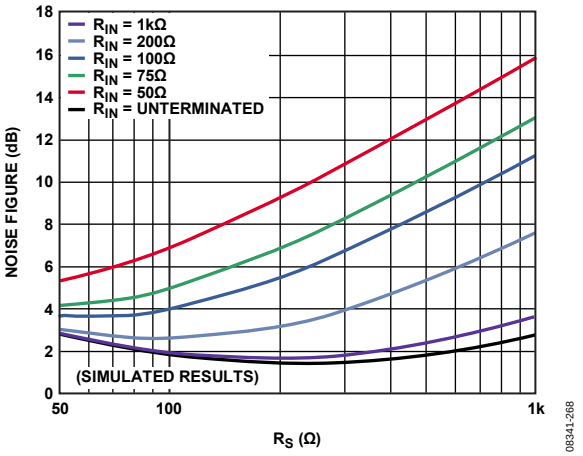


Figure 68. Noise Figure vs. R_S for Various Values of R_{IN}, Actively Matched

The user must determine the level of matching accuracy desired and adjust R_{FB} accordingly. The R_{FB} and C_{FB} network presents a load to OPL that OPH does not see. The user can add an identical load on OPH to improve slightly the distortion caused by this imbalance.

There is a feedback capacitor (C_{FB}) in series with R_{FB} (see Figure 65) because the dc levels of the positive output and the positive input are different. At higher frequencies, the value of the feedback capacitor must be considered.

The unterminated bandwidth ($R_{FB} = \infty$) is 200 MHz. The AD8432 has a low input-referred voltage noise of 0.85 nV/√Hz at the lowest gain, 12.04 dB (unterminated configuration). To achieve such low noise, the dual amplifier consumes 24 mA, resulting in a power consumption of 120 mW.

Table 6. Feedback Resistance for Several R_{IN} and Gain Combinations

Desired R_{IN} (Ω)	Differential Gain (V/V)	Single-Ended Gain, G/2 (V/V)	Exact R_{FB} (Ω), Equation 2	R_{FB} (Ω), 1% Standard Value	Actual R_{IN} (Ω), Equation 2
50	4	2	151.2	150	49.6
75	4	2	227.8	226	74.4
100	4	2	304.9	301	98.7
200	4	2	620	619	199.7
1 k	4	2	3.58 k	3.57 k	998.4
50	8	4	252	250	49.6
100	8	4	508.2	511	100.5
50	12	6	352.9	357	50.6
100	12	6	711.5	715	100.5
50	16	8	453.7	453	49.9
100	16	8	914.8	909	99.4

APPLICATIONS INFORMATION

The AD8432 LNA provides precision gain and ultralow noise performance with minimal external components. Because it is a high performance part, care must be taken to ensure that it is configured optimally to attain the best performance and dynamic range for the system.

TYPICAL SETUP

The internal bias circuitry of the AD8432 sets the input bias voltage at 3.25 V and the output bias voltage at 2.5 V. It is important to ac couple the inputs through a capacitor to maintain the internal dc bias levels. When active input termination is used (R_{FB}), a decoupling capacitor (C_{FB}) is required to isolate the input and output bias voltages of the LNA. A typical value for C_{FB} is 0.1 µF, but a smaller value capacitor is more appropriate at higher frequencies.

The unterminated input impedance of the AD8432 is 6.2 kΩ. Any input resistance between 50 Ω and 6.2 kΩ can be synthesized using active impedance matching.

At the lowest gain (12.04 dB), the gain response exhibits some peaking at higher frequencies. A resistor-capacitor shunt network (RC) at the input (see RSHx and CSHx in Figure 69) is recommended to reduce gain peaking and enhance stability at higher frequencies.

Table 7 shows the recommended values of R_{FB}, C_{SH}, and R_{SH} for all four gains and several input impedance combinations. The values for the C_{SH} and R_{SH} network are determined empirically and can be customized as needed to optimize performance. As R_{IN} increases, the value of C_{SH} diminishes, and for higher input impedance values, no capacitor may be required.

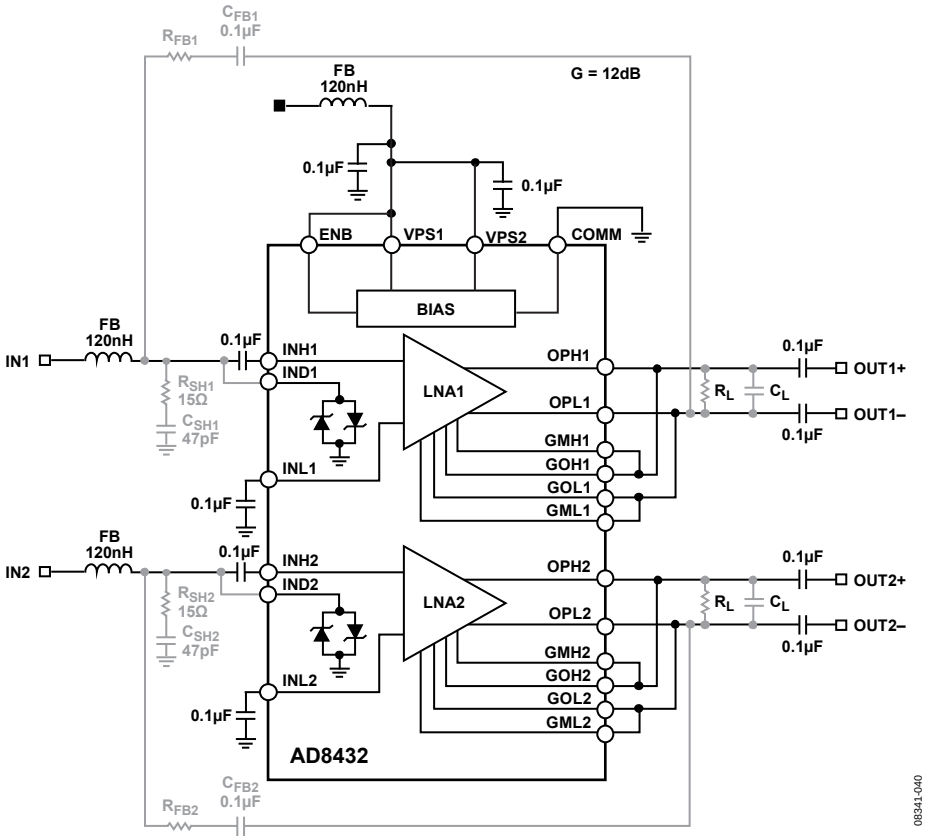


Figure 69. Typical AD8432 Setup, G = 12.04 dB

Table 7. External Component Selections for Common Input Impedance

R_{IN} (Ω)	Gain (dB)	$R_{FB1, 2}$ (Ω)	$C_{SH1, 2}$ (pF)	$R_{SH1, 2}$ (Ω)	−3 dB BW (MHz)
50	12	150	47	15	176
	18	249	30	15	116
	21	357	None	None	117
	24	453	None	None	87
75	12	226	36	15	167
	18	383	None	None	144
	21	536	None	None	100
	24	681	None	None	72
100	12	301	30	15	164
	18	511	None	None	134
	21	715	None	None	90
	24	909	None	None	63
200	12	619	18	15	164
	18	1.02 k	None	None	116
	21	1.43 k	None	None	74
	24	1.87 k	None	None	51
1 k	12	3.57 k	10	10	160
	18	5.9 k	None	None	99
	21	8.25 k	None	None	61
	24	10.7 k	None	None	43
Unterminated, R_S = 50 Ω	12	∞	None	None	178
	18	∞	None	None	95
	21	∞	None	None	59
	24	∞	None	None	40
Unterminated, R_S = 0 Ω	12	∞	None	None	210
	18	∞	None	None	96
	21	∞	None	None	55
	24	∞	None	None	38

I/Q DEMODULATION FRONT END

The AD8432 low noise amplifiers can be used to drive the differential RF inputs of the dual AD8333 or the quad AD8339 I/Q demodulators. The primary application for the AD8339 is phased array beamforming in medical ultrasound, specifically in CW Doppler processing. Other applications include phased array radar and smart antennas for mobile communications.

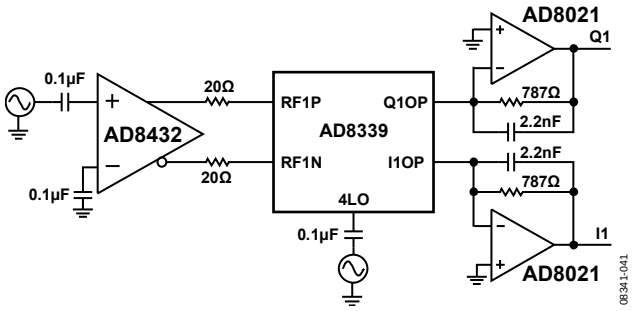


Figure 70. Block Diagram of AD8432 and AD8339 Application for Ultrasound Beamforming

Because of its low output noise and low distortion, the AD8432 ensures minimal degradation in dynamic range while amplifying the RF input signal. At the lowest gain of 12.04 dB, the AD8432 contributes only 3.4 nV/√Hz output voltage noise.

Figure 70 shows a simplified block diagram of one channel of the AD8432 driving the AD8339. The AD8432 outputs can be connected directly to the AD8339 RF inputs through 20 Ω resistors. A differential clock signal, 4LO, which is applied to the 4LOP and 4LON pins of the AD8339, has a frequency 4× that of the RF inputs. The AD8339 downconverts the RF signals, generates quadrature, and phase-shifts the resultant I and Q signals.

The I and Q outputs of the AD8339 are current outputs. A transimpedance amplifier, such as the AD8021, processes the outputs and performs several functions, including the following:

- Current-to-voltage conversion
- Summation amplifier for multiple channels
- Active low-pass filter

In beamforming applications, the I and Q outputs of a number of receiver channels are summed, which increases the system dynamic range by 10 $\log_{10}$ (N), where N is the number of channels being summed. The external RC feedback network of the AD8021 is a 100 kHz low-pass filter as shown in Figure 70. See the AD8333 and AD8339 datasheets for more details on implementing I/Q demodulators.

Evaluation boards are available for the AD8432 and the AD8339 to facilitate system level design and testing. A detailed reference schematic of the setup is shown in Figure 71. The AD8432 is shown in this configuration with a gain of 12.04 dB, with unterminated inputs. If active termination is preferred, use an R_{FB} and C_{FB} network as discussed in the Theory of Operation section. The IND1/IND2 clamping diodes can be connected to IN1/IN2 to protect the LNA input from being overdriven.

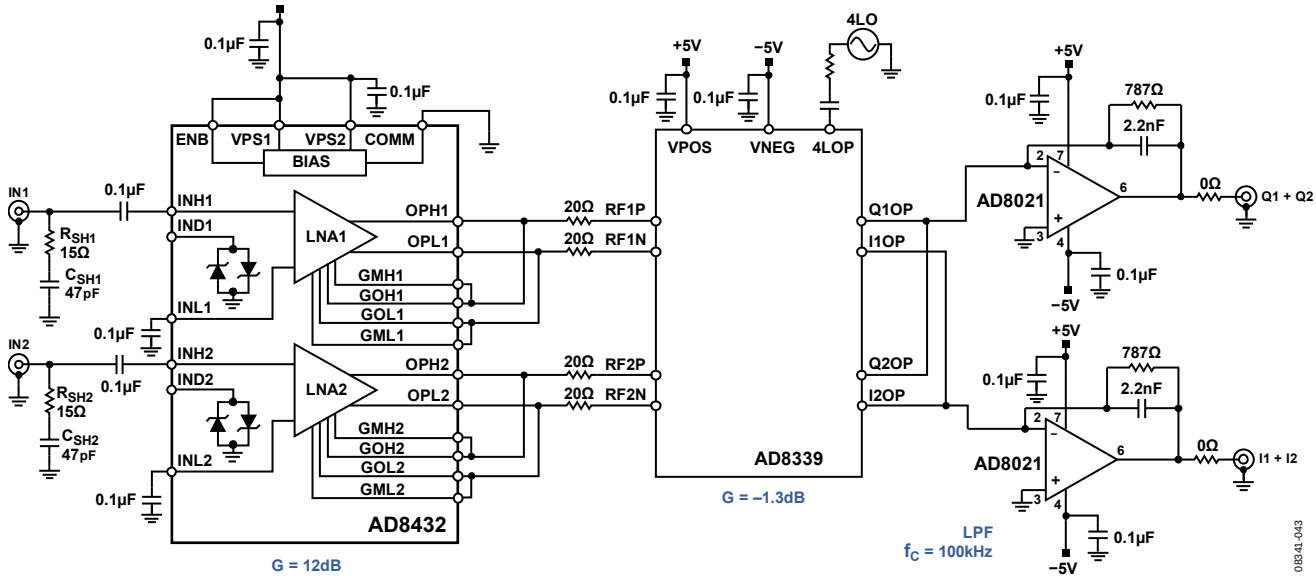


Figure 71. Schematic of the AD8432 (G = 12.04 dB) and AD8339 Application for Ultrasound Beamforming

DIFFERENTIAL-TO-SINGLE-ENDED CONVERSION

Some applications require the low noise and high dynamic range of the AD8432; however, they may also require a single-ended output, rather than a differential output. The AD8129 or AD8130 differential receiver amplifier can be used for the differential-to-single-ended conversion of the AD8432 output, as shown in Figure 72.

The AD8129 is a low noise, high gain (10 or greater) amplifier intended for applications over very long cables, where signal attenuation is significant. The AD8130 is stable at a gain of 1 and can be used for applications where lower gains are required. The AD8129 and AD8130 have user-adjustable gain, set by the ratio of two resistors, to help compensate for losses in the transmission line.

A transformer or balun can also be used to convert the differential output of the AD8432 to a single-ended output. Transformers have lower distortion; however, care must be taken to properly match the impedance of the transformer. The test circuit for distortion measurements in Figure 58 uses an ADTT1-1 transformer to perform differential-to-single-ended conversion.

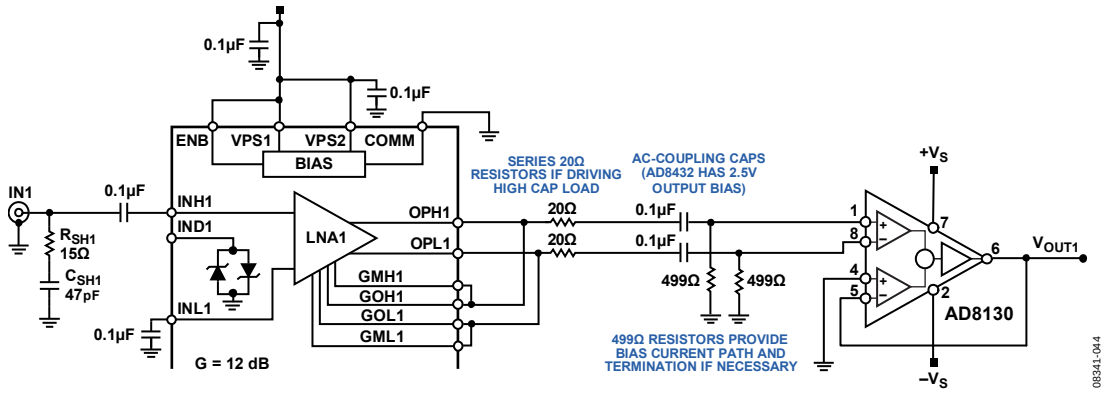


Figure 72. AD8432 Differential-to-Single-Ended Conversion Using the AD8129/AD8130 with Unity Gain

EVALUATION BOARD

Figure 73 is a photo of the AD8432 evaluation board. Completely assembled and pretested, the board provides convenient and fast verification of system design and to assess the performance of the AD8432 under user-specific operating conditions. The remainder of this section describes the operation and construction of the board.

Figure 74 through Figure 79 are various artwork and assembly views and Figure 80 shows the schematic diagram. The board provides access to the inputs, the outputs, and the gain settings. As shipped, the board is configured for a gain of 21 dB and 50 Ω input termination. Multiple combinations of gain and impedance matching are available to the user.

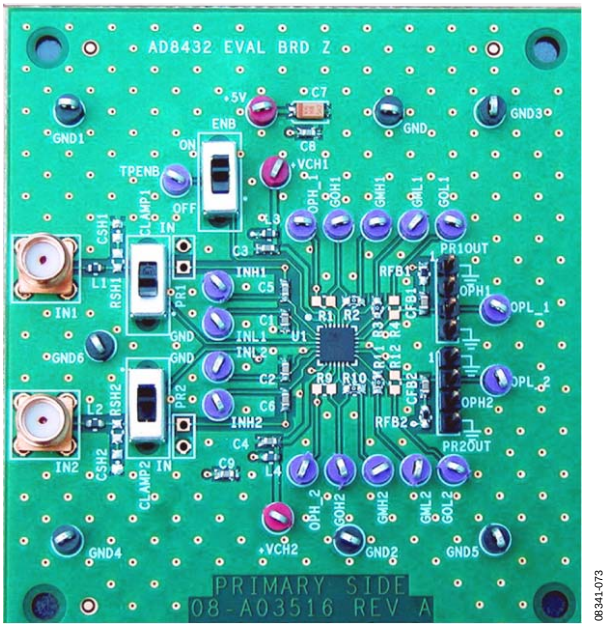


Figure 73. Evaluation Board

CONNECTION AND OPERATION

Power Supply

The AD8432 requires only a single 5 V supply connected to the +5V red test loop and black test loop GND next to it. Separate power pins are provided for the two LNA channels, but the two amplifier sections are wired together and rf-decoupled by small inductors as a precaution. The remaining red test loops are for pin probing as necessary. Should the need for amplifier isolation arise, simply un-power the unneeded amplifier by removing L3 or L4. (Refer to Figure 74 and Figure 80.

Input Termination

The AD8432 features active input termination and boards are shipped for 50 Ω. The input impedance is determined by the LNA gain, and the feedback resistors R_{FB1} and R_{FB2} (see the schematic in Figure 80) and source impedance (refer to the Theory of Operation section and Table 7). C_{FB} provides the necessary ac coupling between the input and output when using active termination; a 0.1 µF capacitor is recommended. The R_{FB} and C_{FB} network presents a load to the OPL; if needed, an equivalent load at OPH balances the differential output.

Switches CLAMP1 and CLAMP2 connect the input clamping diodes (IND1 and IND2) across the signal path. The diodes provide input overvoltage protection in applications where fast transient pulses exceeding 5.5 V or less than –0.6 V are present. Clamping diodes enable faster overdrive recovery times, especially at the lowest gain (12.04 dB). Fast transients are usually not fatal to the device, which features ESD protection in any event.

Setting the Amplifier Gain

The violet test loops OPnn, GOnn and GMnn and Resistors R1–R4 and Resistors R9–R12 are provided for gain adjustment. Install 0 Ω resistors to reduce gain, leaving the positions open to increase gain. As shipped, the evaluation board is configured for G = 21 dB (12×). Table 8 lists the configuration for the four available LNA gain values.

Table 8. Gain Setting Configuration

LNA1	LNA2	GAIN dB(×)			
		8(4)	18(8)	21(12)	24(16)
R1	R9	Y[1]	Y[1]	open	open
R2	R10	Y[1]	open	Y[1]	open
R3	R11	Y[1]	open	Y[1]	open
R4	R12	Y[1]	Y[1]	open	open

[1] Y = Install 0 Ω.

Output

The 4-pin headers PR1OUT and PR2OUT are placed close to the AD8432, and provide a way for monitoring the differential output or the single-ended output using a high impedance differential probe. The two inner pins of the headers are connected to OPL/OPH, and the two outer pins of the headers are connected to ground.

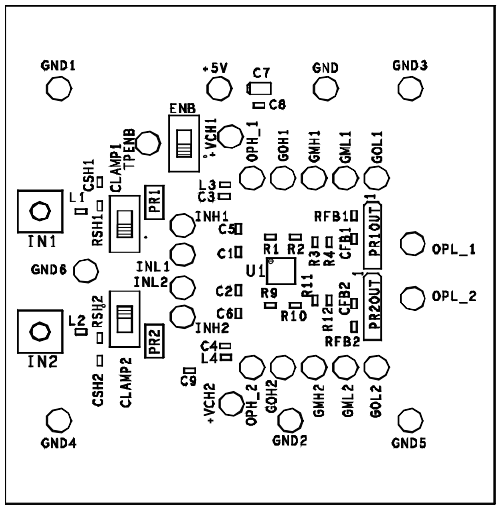


Figure 74. Evaluation Board Assembly

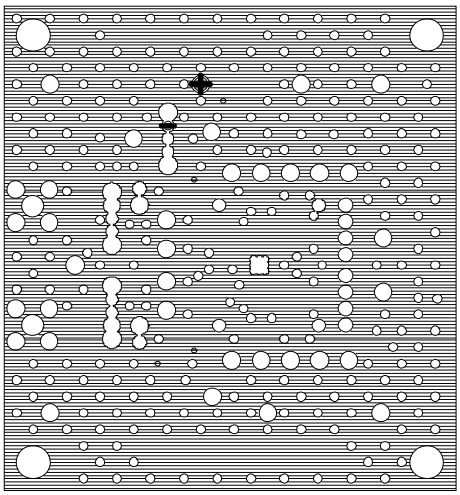


Figure 77. AD8432-EVALZ Power Plane Copper

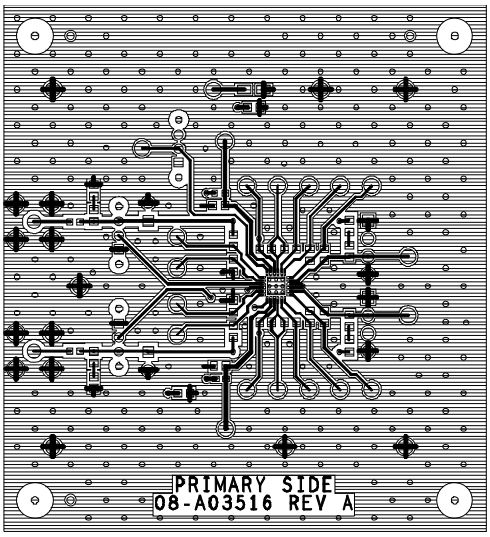


Figure 75. AD8432 Primary Side Copper

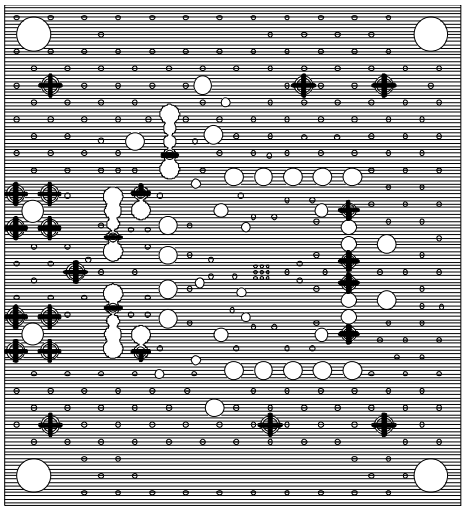


Figure 78. AD8432-EVALZ Ground Plane Copper

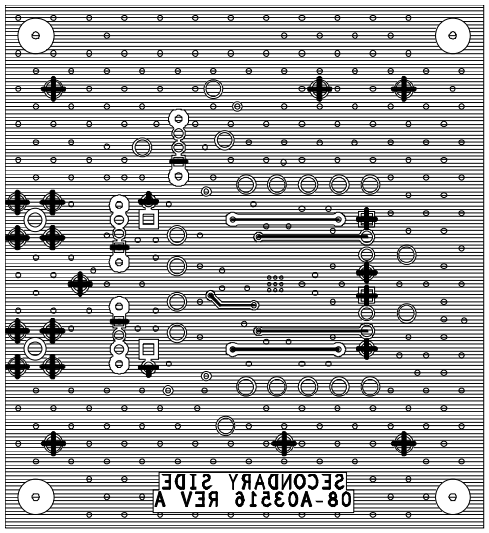


Figure 76. AD8432-EVALZ Secondary Side Copper

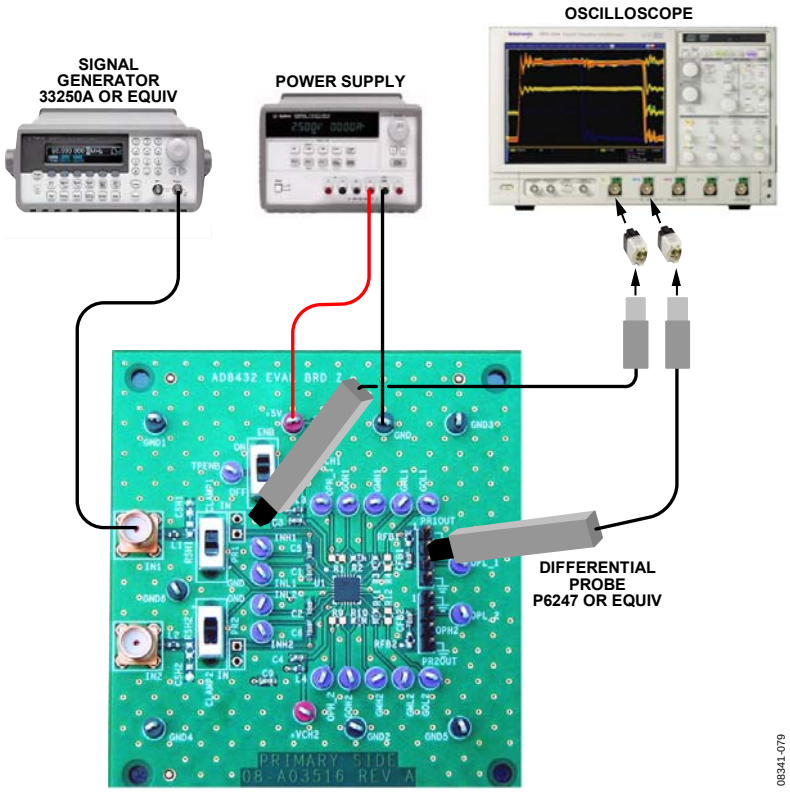


Figure 79. Bench Setup for Testing the AD8432-EVALZ

SCHEMATIC

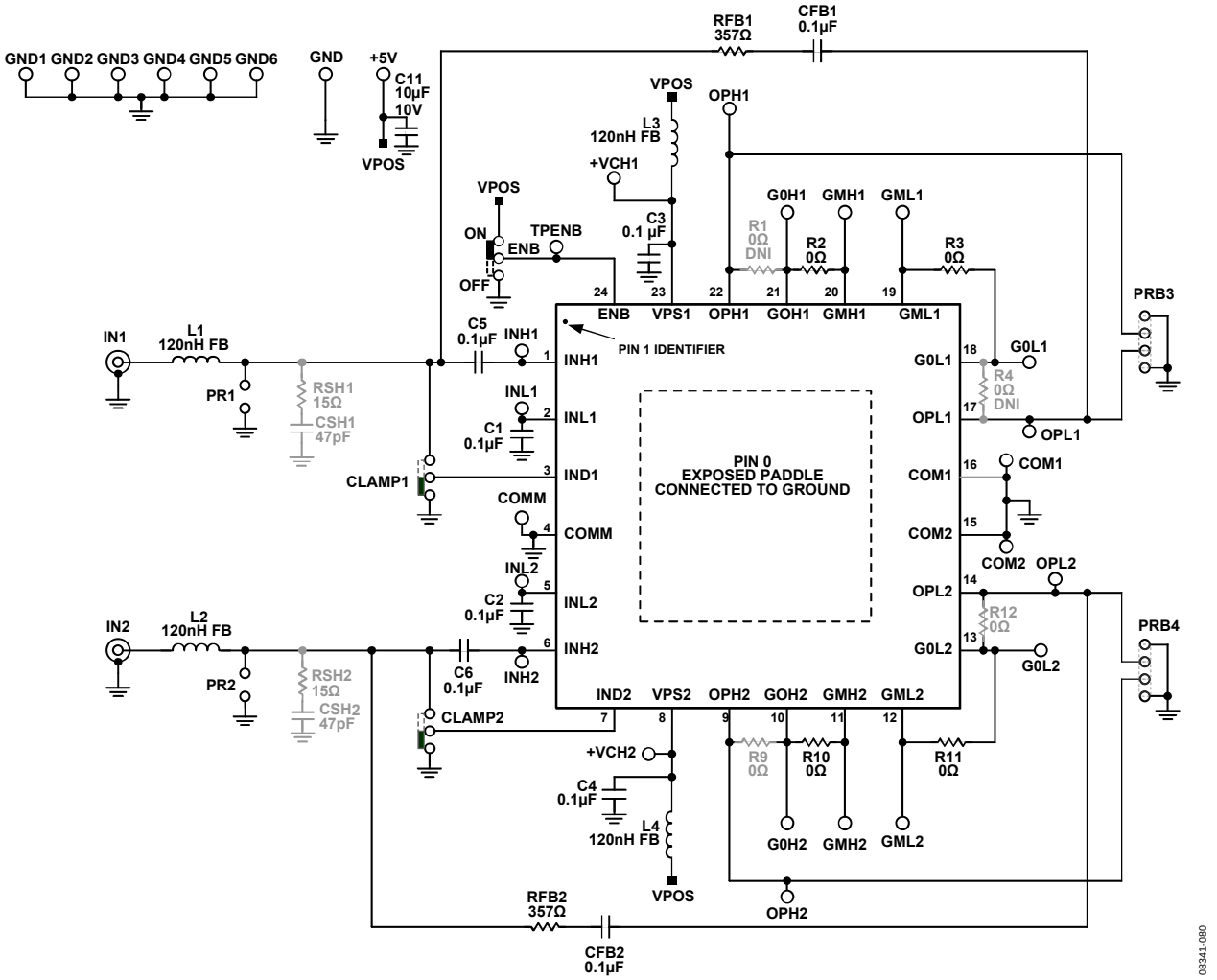


Figure 80. AD8436-EVALZ Schematic

OUTLINE DIMENSIONS

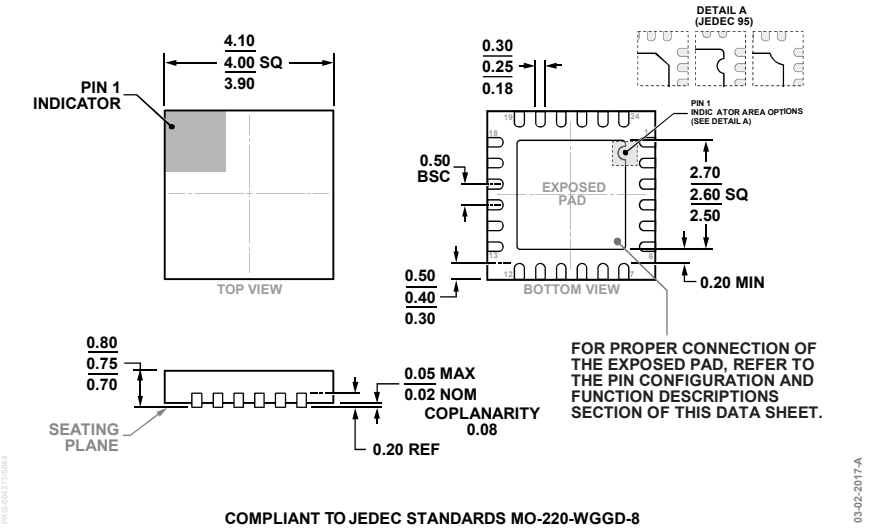


Figure 81. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mmand 0.75 mm Package Height
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8432ACPZ-R7	−40°C to +85°C	24-Lead LFCSP, 7″ Tape and Reel	CP-24-15
AD8432ACPZ-RL	−40°C to +85°C	24-Lead LFCSP, 13″ Tape and Reel	CP-24-15
AD8432ACPZ-WP	−40°C to +85°C	24-Lead LFCSP, Waffle Pack	CP-24-15
AD8432-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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