

TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT DYNAMIC RAM MODULES

SMMS675A – MARCH 1997 – REVISED APRIL 1997

- **Organization**
 - TM497BBK32H/I: 4194304 x 32
 - TM893CBK32H/I: 8388608 x 32
- **Single 5-V Power Supply ($\pm 10\%$ Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497BBK32H/I – Uses Eight 16M-Bit Dynamic Random-Access Memory (DRAM) Devices in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893CBK32H/I – Uses Sixteen 16M-Bit DRAMs in Plastic SOJ Packages**
- **Long Refresh Period**
32 ms (2 048 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page Mode Operation With $\overline{\text{CAS}}$ -Before-RAS (CBR), RAS-Only, and Hidden Refresh**

- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC}	ACCESS TIME t_{AA}	ACCESS TIME t_{CAC}	READ OR WRITE CYCLE (MIN)
	(MAX)	(MAX)	(MAX)	(MIN)
'497BBK32H/I-50	50 ns	25 ns	13 ns	90 ns
'497BBK32H/I-60	60 ns	30 ns	15 ns	110 ns
'497BBK32H/I-70	70 ns	35 ns	18 ns	130 ns
'893CBK32H/I-50	50 ns	25 ns	13 ns	90 ns
'893CBK32H/I-60	60 ns	30 ns	15 ns	110 ns
'893CBK32H/I-70	70 ns	35 ns	18 ns	130 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
0°C to 70°C
- **Gold-Tabbed Version Available:[†]**
TM497BBK32H, TM893CBK32H
- **Tin-Lead (Solder-) Tabbed Version**
Available: TM497BBK32I, TM893CBK32I

description

The TM497BBK32H/I is a 16M-byte dynamic random-access memory (DRAM) device organized as $4 \times 4194304 \times 8$ bits in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417400ADJ, 4194304×4 -bit DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417400ADJ is described in the TMS417400A data sheet (literature number SMKS889).

The TM497BBK32H/I SIMM is available in the single-sided BK leadless module for use with sockets. The TM497BBK32H/I features RAS access times of 50, 60, and 70 ns. This device is characterized for operation from 0°C to 70°C.

The TM893CBK32H/I is a 32M-byte DRAM organized as $4 \times 8388608 \times 8$ bits in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS417400ADJ, 4194304×4 -bit DRAMs.

The TM893CBK32H/I SIMM is available in the double-sided BK leadless module for use with sockets. The TM893CBK32H/I features RAS access times of 50, 60, and 70 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497BBK32H/I operates as eight TMS417400ADJs connected as shown in the functional block diagram and in Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1997, Texas Instruments Incorporated

TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT DYNAMIC RAM MODULES

SMMS675A – MARCH 1997 – REVISED APRIL 1997

operation (continued)

The TM893CBK32H/I operates as sixteen TMS417400ADJs connected as shown in the functional block diagram and in Table 2. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

Table 1 and Table 2 show TM497BBK32H/I and TM389CBK32H/I data block configurations in reference to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ interfacing.

Table 1. TM497BBK32H/I Connection Table

DATA BLOCK	$\overline{\text{RASx}}$	$\overline{\text{CASx}}$
DQ0–DQ7	$\overline{\text{RAS0}}$	$\overline{\text{CAS0}}$
DQ8–DQ15	$\overline{\text{RAS0}}$	$\overline{\text{CAS1}}$
DQ16–DQ23	$\overline{\text{RAS2}}$	$\overline{\text{CAS2}}$
DQ24–DQ31	$\overline{\text{RAS2}}$	$\overline{\text{CAS3}}$

Table 2. TM893CBK32H/I Connection Table

DATA BLOCK	$\overline{\text{RASx}}$		$\overline{\text{CASx}}$
	Side 1	Side 2	
DQ0–DQ7	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS0}}$
DQ8–DQ15	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS1}}$
DQ16–DQ23	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS2}}$
DQ24–DQ31	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS3}}$

single-in-line memory module and components

PC substrate: 1.27 ± 0.1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage

Bypass capacitors: Multilayer ceramic

Contact area for TM497BBK32H and TM893CBK32H: Nickel plate and gold plate over copper

Contact area for TM497BBK32I and TM893CBK32I: Nickel plate and tin-lead over copper

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2 048 rows must be strobed with $\overline{\text{RAS}}$ to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

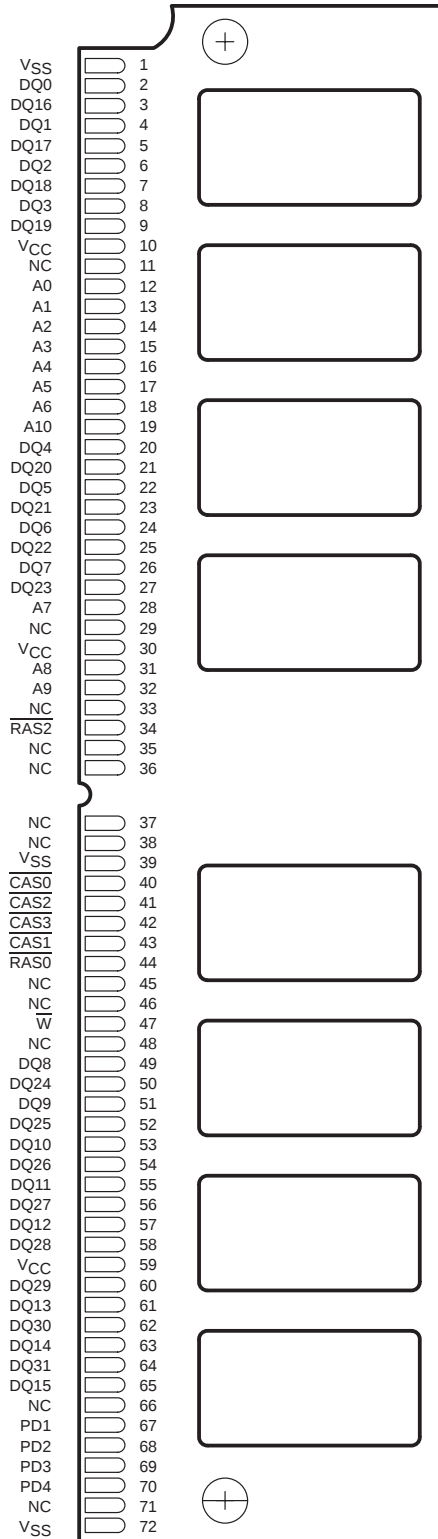
power up

To achieve proper operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{\text{RAS}}$ -only or CBR) cycle.

TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
DYNAMIC RAM MODULES

SMMS675A – MARCH 1997 – REVISED APRIL 1997

**BK SINGLE-IN-LINE PACKAGE
(TOP VIEW)**



**TM497BBK32H/I
(SIDE VIEW)**



**TM893CBK32H/I
(SIDE VIEW)**



PIN NOMENCLATURE

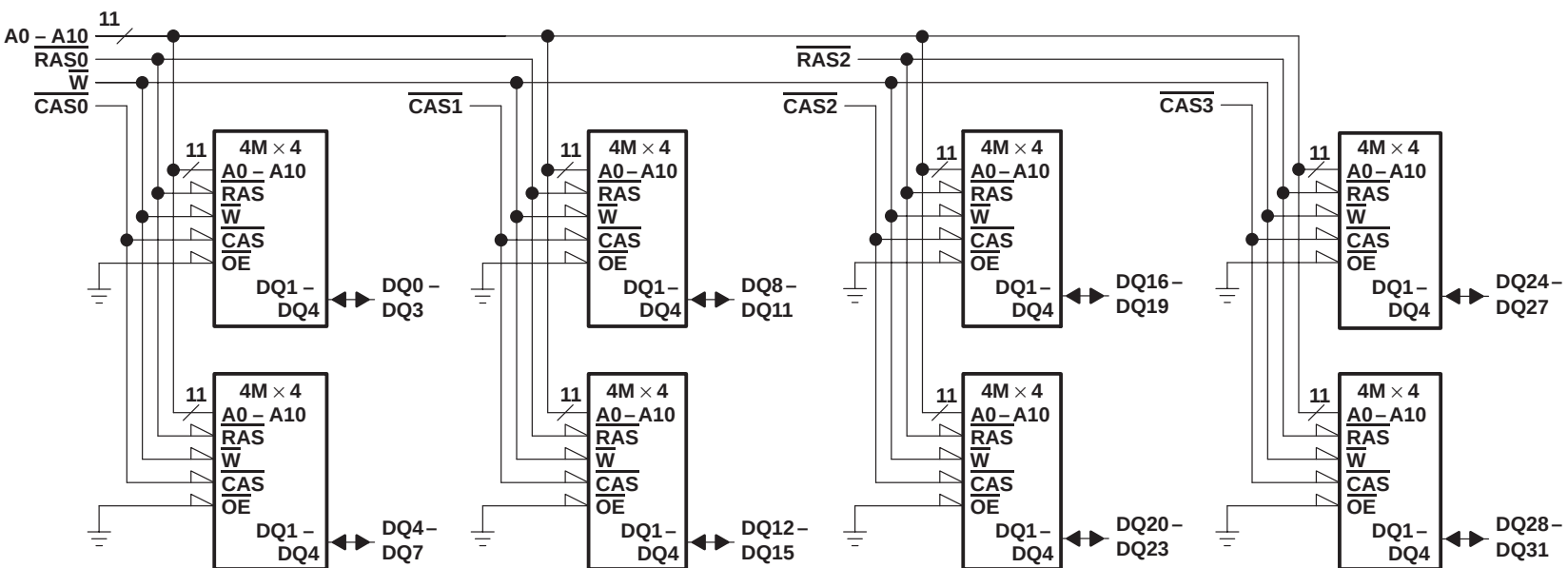
A0–A10	Address Inputs
CAS0–CAS3	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
RAS0–RAS3	Row-Address Strobe
V _{CC}	5-V Supply
V _{SS}	Ground
W	Write Enable

PRESENCE DETECT

SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497BBK32H/I	50 ns	V _{SS}	NC	V _{SS}	V _{SS}
	60 ns	V _{SS}	NC	NC	NC
	70 ns	V _{SS}	NC	V _{SS}	NC
TM893CBK32H/I	50 ns	NC	V _{SS}	V _{SS}	V _{SS}
	60 ns	NC	V _{SS}	NC	NC
	70 ns	NC	V _{SS}	V _{SS}	NC

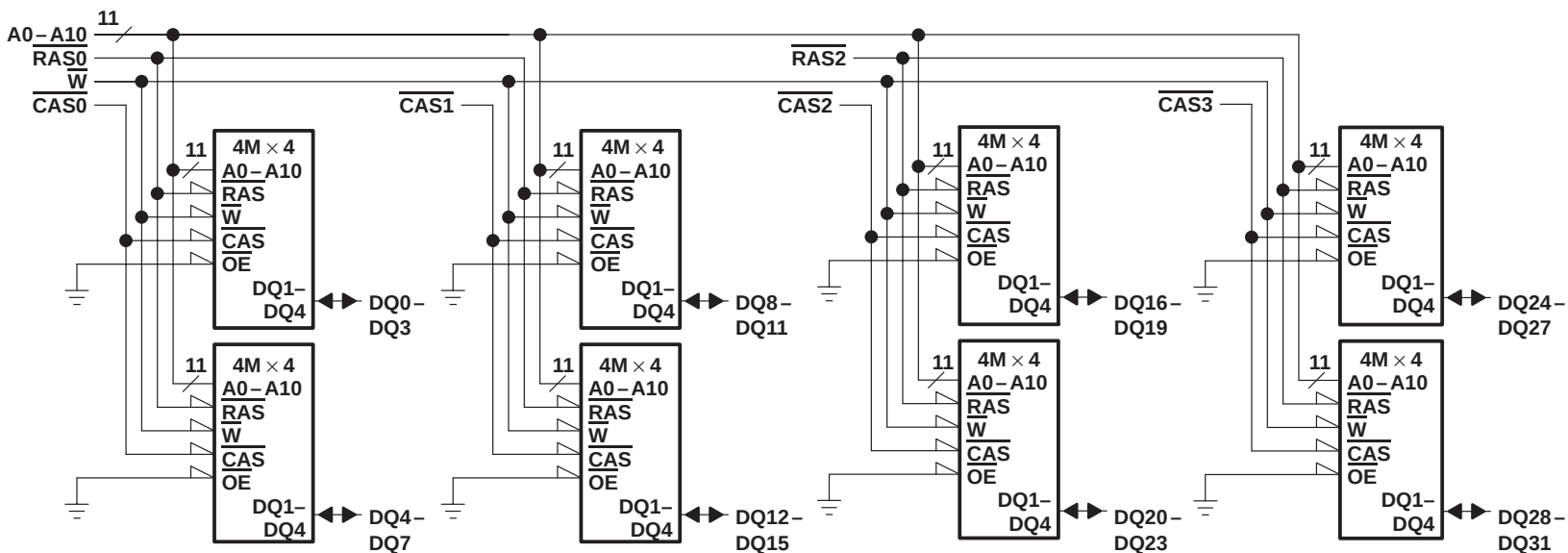
**TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
DYNAMIC RAM MODULES**
SMMS675A - MARCH 1997 - REVISED APRIL 1997

functional block diagram of TM497BBK32H/I

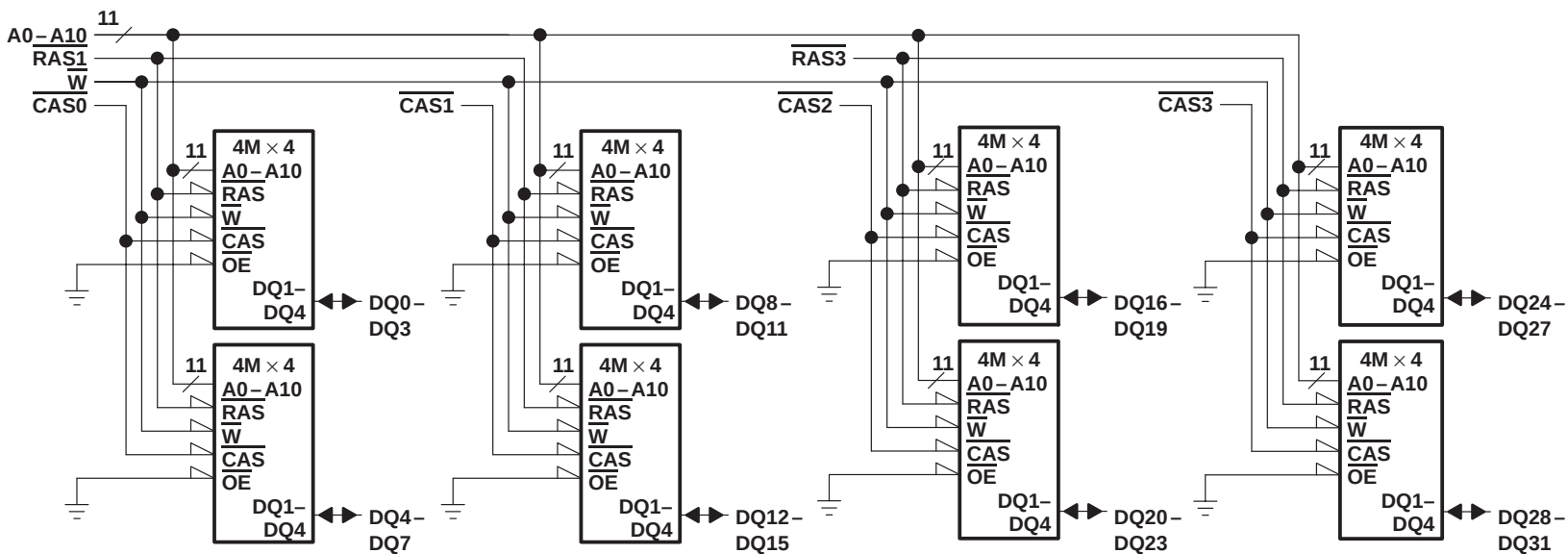


functional block diagram of TM893CBK32H/I

side 1



side 2



TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
DYNAMIC RAM MODULES

SMMS675A – MARCH 1997 – REVISED APRIL 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	– 1 V to 7 V
Voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	16 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2.4		6.5	V
V_{IL} Low-level input voltage (see Note 2)	– 1		0.8	V
T_A Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS [‡]	'497BBK32H/I-50		'497BBK32H/I-60		'497BBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH} High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
V_{OL} Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
I_I Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC} , CAS high		± 10		± 10		± 10	µA
I_{CC1} Read- or write-cycle current (see Note 3)	$V_{CC} = 5.5$ V, Minimum cycle		1040		880		800	mA
I_{CC2} Standby current	$V_{IH} = 2.4$ V (TTL), After one memory cycle, RAS and CAS high		16		16		16	mA
	$V_{IH} = V_{CC} - 0.2$ V (CMOS), After one memory cycle, RAS and CAS high		8		8		8	mA
I_{CC3} Average refresh current (RAS only or CBR) (see Note 3)	$V_{CC} = 5.5$ V, RAS cycling, (RAS only); Minimum cycle, CAS high RAS low after CAS low (CBR)		1040		880		800	mA
I_{CC4} Average page current (see Note 4)	$V_{CC} = 5.5$ V, RAS low, $t_{PC} = \text{MIN}$, CAS cycling		720		560		480	mA

[‡] For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}} = V_{IL}$

4. Measured with a maximum of one address change while $\overline{\text{CAS}} = V_{IH}$



**TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
DYNAMIC RAM MODULES**

SMMS675A – MARCH 1997 – REVISED APRIL 1997

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'893CBK32H/I-50		'893CBK32H/I-60		'893CBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 5 mA	2.4		2.4		2.4		V
V _{OL} Low-level output voltage	I _{OL} = 4.2 mA		0.4		0.4		0.4	V
I _I Input current (leakage)	V _{CC} = 5.5 V, V _I = 0 V to 6.5 V, All others = 0 V to V _{CC}		± 20		± 20		± 20	µA
I _O Output current (leakage)	V _{CC} = 5.5 V, V _O = 0 V to V _{CC} , CASx high		± 20		± 20		± 20	µA
I _{CC1} Read- or write-cycle current (see Note 3)	V _{CC} = 5.5 V, Minimum cycle		1048		888		808	mA
I _{CC2} Standby current	V _{IH} = 2.4 V (TTL), After one memory cycle, RASx and CASx high		32		32		32	mA
	V _{IH} = V _{CC} – 0.2 V (CMOS), After one memory cycle, RASx and CASx high		16		16		16	mA
I _{CC3} Average refresh current (RAS only or CBR) (see Note 3)	V _{CC} = 5.5 V, RASx cycling, (RASx only); Minimum cycle CASx low (CBR) CASx high RASx low after		2080		1760		1600	mA
I _{CC4} Average page current (see Note 4)	V _{CC} = 5.5 V, RASx low, t _{PC} = MIN, CASx cycling		1440		1120		960	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}} = V_{IL}$

4. Measured with a maximum of one address change while CAS = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		TM497BBK32H/I		TM893CBK32H/I		UNIT
		MIN	MAX	MIN	MAX	
C _{i(A)}	Input capacitance, address inputs		50		80	pF
C _{i(R)}	Input capacitance, $\overline{\text{RAS}}$ inputs		33		28	pF
C _{i(C)}	Input capacitance, $\overline{\text{CAS}}$ inputs		17		28	pF
C _{i(W)}	Input capacitance, write-enable input		66		112	pF
C _{o(DQ)}	Output capacitance on DQ pins		9		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.



TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
DYNAMIC RAM MODULES

SMMS675A – MARCH 1997 – REVISED APRIL 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	'497BBK32H/I-50 '893CBK32H/I-50		'497BBK32H/I-60 '893CBK32H/I-60		'497BBK32H/I-70 '893CBK32H/I-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AA} Access time from column address		25		30		35	ns
t _{CAC} Access time from $\overline{\text{CAS}}$ low		13		15		18	ns
t _{CPA} Access time from column precharge		30		35		40	ns
t _{RAC} Access time from $\overline{\text{RAS}}$ low		50		60		70	ns
t _{CLZ} $\overline{\text{CAS}}$ to output in low-impedance state	0		0		0		ns
t _{OH} Output disable time from start of $\overline{\text{CAS}}$ high	3		3		3		ns
t _{OFF} Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0	13	0	15	0	18	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.



**TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
DYNAMIC RAM MODULES**

SMMS675A – MARCH 1997 – REVISED APRIL 1997

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'497BBK32H/I-50 '893CBK32H/I-50		'497BBK32H/I-60 '893CBK32H/I-60		'497BBK32H/I-70 '893CBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC}	Cycle time, random read or write (see Note 7)	90		110		130		ns
t _{PC}	Cycle time, page-mode read or write (see Notes 7 and 8)	35		40		45		ns
t _{RASP}	Pulse duration, page-mode, $\overline{\text{RAS}}$ low	50	100 000	60	100 000	70	100 000	ns
t _{RAS}	Pulse duration, non-page-mode, $\overline{\text{RAS}}$ low	50	10 000	60	10 000	70	10 000	ns
t _{CAS}	Pulse duration, $\overline{\text{CAS}}$ low	13	10 000	15	10 000	18	10 000	ns
t _{CP}	Pulse duration, $\overline{\text{CAS}}$ high	8		10		10		ns
t _{RP}	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	30		40		50		ns
t _{WP}	Pulse duration, $\overline{\text{W}}$ low	10		10		10		ns
t _{ASC}	Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{ASR}	Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t _{DS}	Setup time, data before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{RCS}	Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{CWL}	Setup time, $\overline{\text{W}}$ -low before $\overline{\text{CAS}}$ high	13		15		18		ns
t _{RWL}	Setup time, $\overline{\text{W}}$ -low before $\overline{\text{RAS}}$ high	13		15		18		ns
t _{WCS}	Setup time, $\overline{\text{W}}$ -low before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{WRP}	Setup time, $\overline{\text{W}}$ -high before $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t _{CAH}	Hold time, column address after $\overline{\text{CAS}}$ low	10		10		15		ns
t _{RHCP}	Hold time, $\overline{\text{RAS}}$ high after $\overline{\text{CAS}}$ precharge	30		35		40		ns
t _{DH}	Hold time, data after $\overline{\text{CAS}}$ low	10		10		15		ns
t _{RAH}	Hold time, row address after $\overline{\text{RAS}}$ low	8		10		10		ns
t _{RCH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 9)	0		0		0		ns
t _{RRH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 9)	0		0		0		ns
t _{WCH}	Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low	10		10		15		ns
t _{WRH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t _{CHR}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	10		10		10		ns
t _{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	5		5		5		ns
t _{CSH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	50		60		70		ns
t _{CSR}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	5		5		5		ns
t _{RAD}	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 10)	13	25	15	30	15	35	ns
t _{RAL}	Delay time, column address to $\overline{\text{RAS}}$ high	25		30		35		ns
t _{CAL}	Delay time, column address to $\overline{\text{CAS}}$ high	25		30		35		ns
t _{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 10)	18	37	20	45	20	52	ns
t _{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR only)	5		5		5		ns
t _{RSH}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	13		15		18		ns
t _{REF}	Refresh time interval		32		32		32	ms
t _T	Transition time	2	30	2	30	2	30	ns

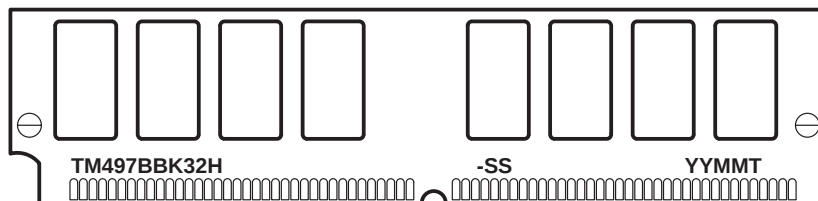
- NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to ensure access time.



**TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
DYNAMIC RAM MODULES**

SMMS675A – MARCH 1997 – REVISED APRIL 1997

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: The location of the part number may vary.

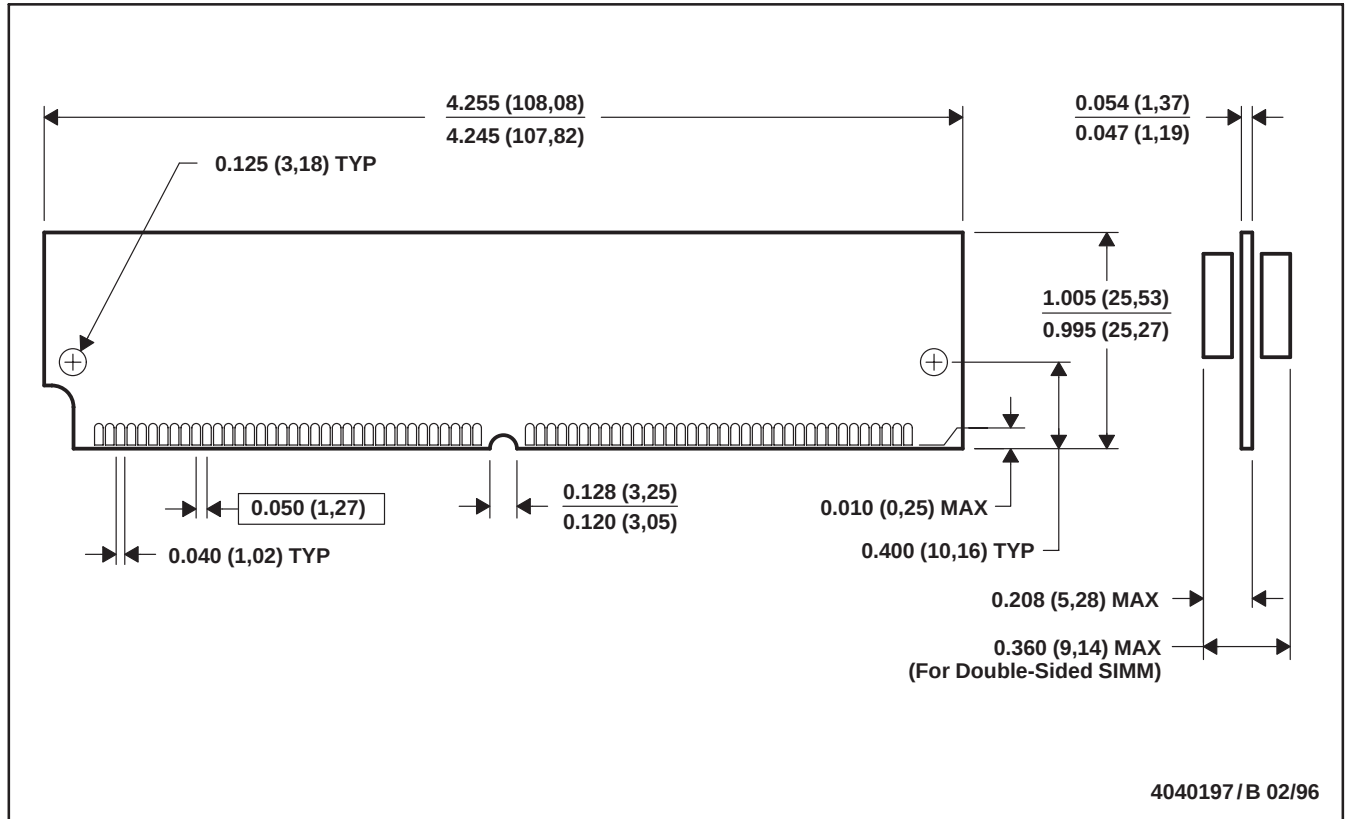
TM497BBK32H, TM497BBK32I 4194304 BY 32-BIT
 TM893CBK32H, TM893CBK32I 8388608 BY 32-BIT
 DYNAMIC RAM MODULES

SMMS675A – MARCH 1997 – REVISED APRIL 1997

MECHANICAL DATA

BK (R-PSIM-N72)

SINGLE-IN-LINE MEMORY MODULE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.