

ISO772x High-Speed, Robust EMC, Reinforced Dual-Channel Digital Isolators

1 Features

- 100 Mbps Data Rate
- Robust Isolation Barrier:
 - >100-Year Projected Lifetime at 1.5 kV_{RMS} Working Voltage
 - Up to 5000 V_{RMS} Isolation Rating
 - Up to 12.8 kV Surge Capability
 - ±100 kV/μs Typical CMTI
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V Level Translation
- Default Output *High* (ISO772x) and *Low* (ISO772xF) Options
- Wide Temperature Range: –55°C to +125°C
- Low Power Consumption, Typical 1.7 mA per Channel at 1 Mbps
- Low Propagation Delay: 11 ns Typical
- Robust Electromagnetic Compatibility (EMC)
 - System-Level ESD, EFT, and Surge Immunity
 - ±8 kV IEC 61000-4-2 Contact Discharge Protection across Isolation Barrier
 - Low Emissions
- Wide-SOIC (DW-16, DWV-8) and Narrow-SOIC (D-8) Package Options
- Automotive Version Available: [ISO772x-Q1](#)
- Safety-Related Certifications:
 - VDE Reinforced Insulation according to DIN V VDE V 0884-11:2017-01
 - 5000 V_{RMS} (DW-16, DWV-8) and 3000 V_{RMS} (D-8) Isolation Rating per UL 1577
 - CSA Certification per IEC 60950-1, IEC 62368-1 and IEC 60601-1 End Equipment Standards
 - CQC Certification per GB4943.1-2011
 - TUV Certification according to EN 60950-1 and EN 61010-1

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment

3 Description

The ISO772x devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW and DWV packages) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO₂) insulation barrier. The ISO7720 device has both channels in the same direction while the ISO7721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See the [Device Functional Modes](#) section for further details.

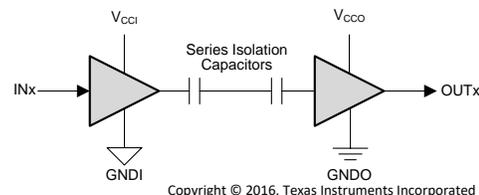
Used in conjunction with isolated power supplies, these devices help prevent noise currents on data buses, such as RS-485, RS-232, and CAN, from damaging sensitive circuitry. Through innovative chip design and layout techniques, the electromagnetic compatibility of the ISO772x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO772x family of devices is available in 16-pin SOIC wide-body (DW), 8-pin SOIC wide-body (DWV), and 8-pin SOIC narrow-body (D) packages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7720, ISO7721 ISO7721F, ISO7721F	D (8)	4.90 mm × 3.91 mm
	DWV (8)	5.85 mm × 7.50 mm
	DW (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2018) to Revision D	Page
• Made editorial and cosmetic changes throughout the document	1
• Changed From: "Isolation Barrier Life: >40 Years" To: ">100-Year Projected Lifetime at 1.5 kV _{RMS} Working Voltage" in Features	1
• Added "Up to 5000 V _{RMS} Isolation Rating" in Features	1
• Added "Up to 12.8 kV Surge Capability" in Features	1
• Added "±8 kV IEC 61000-4-2 Contact Discharge Protection across Isolation Barrier" in Features	1
• Added "Automotive Version Available: ISO772x-Q1" in Features	1
• Deleted "Certification Planned" statement throughout the document	1
• Updated Applications list	1
• Updated Simplified Schematic to show two isolation capacitors in series per channel instead of a single isolation capacitor	1
• Added "Contact discharge per IEC 61000-4-2" specification of ±8000 V in ESD Ratings table	5
• Changed 'Signaling' rate to 'Data' rate and added table note to <i>Data rate</i> specification in Recommended Operating Conditions table	5
• Changed V _{IO_{RM}} Value for DW-16 and DWV-8 packages From: "1414 V _{PK} " To: "2121 V _{PK} " in Insulation Specifications table	7
• Changed V _{IO_{WM}} Values for DW-16 and DWV-8 packages From: "1000 V _{RMS} " and "1414 V _{DC} " To: "1500 V _{RMS} " and "2121 V _{DC} " in Insulation Specifications table	7
• Added 'see Figure 26 ' to TEST CONDITIONS of V _{IO_{WM}} specification	7
• Changed V _{IO_{TM}} TEST CONDITIONS for 100% production test From: "V _{TEST} = V _{IO_{TM}} " To: "V _{TEST} = 1.2 x V _{IO_{TM}} " in Insulation Specifications table	7

Revision History (continued)

• Changed V_{IOSM} TEST CONDITIONS From: "Test method per IEC 60065" To: "Test method per IEC 62368-1" in Insulation Specifications table	7
• Changed q_{pd} TEST CONDITIONS for method b1 test From: " $V_{ini} = V_{IOTM}$ " To: " $V_{ini} = 1.2 \times V_{IOTM}$ " in Insulation Specifications table	7
• Updated certification information in Safety-Related Certifications table.....	8
• Added Insulation Lifetime sub-section under Application Curve section.....	24
• Added 'How to use isolation to improve ESD, EFT and Surge immunity in industrial systems' application report to Documentation Support section	27

Changes from Revision B (March 2017) to Revision C
Page

• Added the 8-pin SOIC package (DWV) to the data sheet	1
• Updated the VDE and CSA certification description throughout the document	1
• Changed the climatic category for the D package from 5/125/21 to 55/125/21	7
• Changed the maximum working voltages for DW-16 and D-8 from 400 to 700 V_{RMS} and 250 to 400 V_{RMS} (respectively) in the Safety-Related Certifications table.....	8
• Switched the line colors for V_{CC} at 2.5 V and V_{CC} at 3.3 V in the Low-Level Output Voltage vs Low-Level Output Current graph.....	15
• Deleted EN from the Common-Mode Transient Immunity Test Circuit figure	17
• Added the Device Support section	27

Changes from Revision A (December 2016) to Revision B
Page

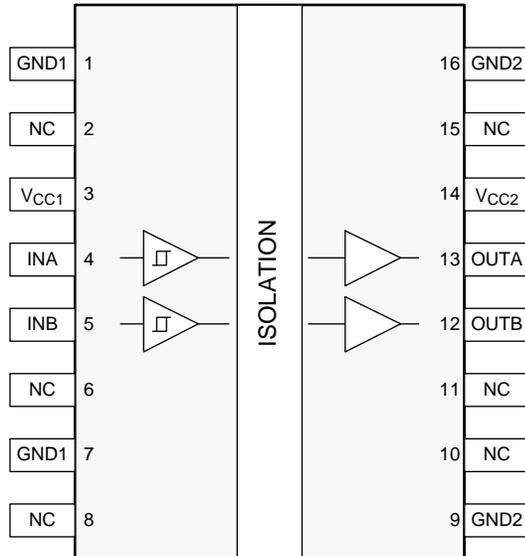
• Added D-8 values for TUV in the Safety-Related Certifications table	8
• Changed the minimum CMTI value from 40 kV/ μ s to 85 kV/ μ s in all Electrical Characteristics tables.....	10
• Added the Receiving Notification of Documentation Updates section	27
• Changed the Electrostatic Discharge Caution statement	27

Changes from Original (November 2016) to Revision A
Page

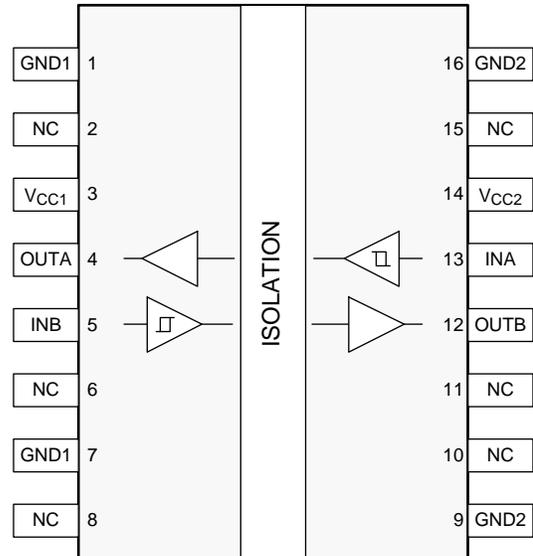
• Changed Feature From: IEC 60950-1, IEC 60601-1 and IEC 61010-1 End Equipment Standards To: IEC 60950-1 and IEC 60601-1 End Equipment Standards	1
• Added Climatic category to the Insulation Specifications	7
• Changed the CSA column of Regulatory Information	8
• Changed DW package) To: (DW-16) in the TUV column of Regulatory Information	8
• Changed t_{ie} TYP value From: 1.5 To 1 in Switching Characteristics—5-V Supply	13
• Changed t_{ie} TYP value From: 1.5 To 1 in Switching Characteristics—3.3-V Supply	13
• Changed t_{ie} TYP value From: 1.5 To 1 in Switching Characteristics—2.5-V Supply	13

5 Pin Configuration and Functions

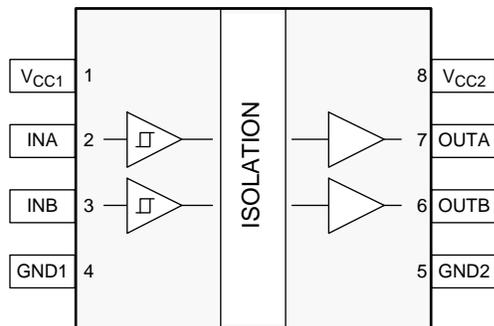
**ISO7720 DW Package
16-Pin SOIC
Top View**



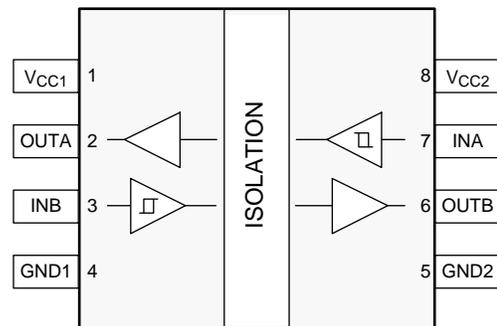
**ISO7721 DW Package
16-Pin SOIC
Top View**



**ISO7720 D and DWV Package
8-Pin SOIC
Top View**



**ISO7721 D and DWV Package
8-Pin SOIC
Top View**



Pin Functions

NAME	PIN		I/O	DESCRIPTION		
	DW PACKAGE	D, DWV PACKAGE				
	ISO7720	ISO7721	ISO7720	ISO7721		
GND1	1, 7	1, 7	4	4	—	Ground connection for V_{CC1}
GND2	9	9	5	5	—	Ground connection for V_{CC2}
	16	16				
INA	4	13	2	7	I	Input, channel A
INB	5	5	3	3	I	Input, channel B
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	—	—	—	Not connected
OUTA	13	4	7	2	O	Output, channel A
OUTB	12	12	6	6	O	Output, channel B
V_{CC1}	3	3	1	1	—	Power supply, V_{CC1}
V_{CC2}	14	14	8	8	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

See ⁽¹⁾.

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage ⁽²⁾	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	$V_{CC} + 0.5^{(3)}$	V
I_O	Output current	-15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±6000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	
	Contact discharge per IEC 61000-4-2; Isolation barrier withstand test ⁽³⁾⁽⁴⁾	±8000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- (4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising		2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling	1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis	100	200		mV
I_{OH}	High-level output current	$V_{CCO}^{(1)} = 5\text{ V}$		-4	mA
		$V_{CCO} = 3.3\text{ V}$		-2	
		$V_{CCO} = 2.5\text{ V}$		-1	
I_{OL}	Low-level output current	$V_{CCO} = 5\text{ V}$		4	mA
		$V_{CCO} = 3.3\text{ V}$		2	
		$V_{CCO} = 2.5\text{ V}$		1	
V_{IH}	High-level input voltage	$0.7 \times V_{CCI}^{(1)}$		V_{CCI}	V
V_{IL}	Low-level input voltage	0		$0.3 \times V_{CCI}$	V
DR ⁽²⁾	Data rate	0		100	Mbps
T_A	Ambient temperature	-55	25	125	°C

- (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .
- (2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO772x			UNIT
		DW (SOIC)	DWV (SOIC)	D (SOIC)	
		16 PINS	16 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.5	84.3	137.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.6	36.3	54.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	47.0	71.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.3	7.4	7.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.2	45.1	70.7	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7720						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			100	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			20	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			80	mW
ISO7721						
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			100	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			50	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $C_L = 15\text{ pF}$, input a 50 MHz 50% duty cycle square wave			50	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE			UNIT
			DW	DWV	D	
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	8	8.5	4	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	8	8.5	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	>600	V
	Material group	According to IEC 60664-1	I	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V _{RMS}	I-IV	I-IV	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-IV	I-IV	I-III	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	I-IV	n/a	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	I-III	n/a	
DIN V VDE V 0884-11:2017-01 ⁽²⁾						
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2121	637	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) test; see Figure 26	1500	1500	450	V _{RMS}
		DC voltage	2121	2121	637	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	8000	7071	4242	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 62368-1, 1.2/50 µs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	8000	8000	5000	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a, After Input/Output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test), V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤5	≤5	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 × sin(2πft), f = 1 MHz	~0.5	~0.5	~0.5	pF
R _{IO}	Isolation resistance ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	>10 ¹²	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	>10 ¹¹	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	>10 ⁹	>10 ⁹	
	Pollution degree		2	2	2	
	Climatic category		55/125/21	55/125/21	55/125/21	
UL 1577						
V _{ISO}	Withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	5000	5000	3000	V _{RMS}

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
Reinforced Insulation; Maximum transient isolation voltage, 8000 V _{PK} (DW-16), 7071 V _{PK} (DWV-8) and 4242 V _{PK} (D-8); Maximum repetitive peak isolation voltage, 2121 V _{PK} (DW-16, DWV-8) and 637 V _{PK} (D-8); Maximum surge isolation voltage, 8000 V _{PK} (DW-16, DWV-8) and 5000 V _{PK} (D-8)	800 V _{RMS} (DW-16) and 850 V _{RMS} (DWV-8) reinforced insulation and 400 V _{RMS} (D-8) basic insulation working voltage per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1:2014, (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V _{RMS} (DW-16, DWV-8) max working voltage	DW-16, DWV-8: Single protection, 5000 V _{RMS} ; D-8: Single protection, 3000 V _{RMS}	DW-16, DWV-8: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage; D-8: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V _{RMS} maximum working voltage	5000 V _{RMS} (DW-16, DWV-8) and 3000 V _{RMS} (D-8) Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V _{RMS} (DW-16, DWV-8) and 300 V _{RMS} (D-8) 5000 V _{RMS} (DW-16, DWV-8) and 3000 V _{RMS} (D-8) Reinforced insulation per EN 60950-1:2006/A2:2013 up to working voltage of 800 V _{RMS} (DW-16, DWV-8) and 400 V _{RMS} (D-8)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate numbers: CQC15001121716 (DW-16) CQC18001199096 (DWV-8) CQC15001121656 (D-8)	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I _S	Safety input, output, or supply current ⁽¹⁾	R _{θJA} = 86.5 °C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 1			263	mA
		R _{θJA} = 86.5 °C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 1			401	
		R _{θJA} = 86.5 °C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 1			525	
P _S	Safety input, output, or total power ⁽¹⁾	R _{θJA} = 86.5 °C/W, T _J = 150°C, T _A = 25°C, see Figure 2			1445	mW
T _S	Maximum safety temperature ⁽¹⁾				150	°C
DWV-8 PACKAGE						
I _S	Safety input, output, or supply current ⁽¹⁾	R _{θJA} = 84.3 °C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 3			270	mA
		R _{θJA} = 84.3 °C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 3			412	
		R _{θJA} = 84.3 °C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 3			539	
P _S	Safety input, output, or total power ⁽¹⁾	R _{θJA} = 84.3 °C/W, T _J = 150°C, T _A = 25°C, see Figure 4			1483	mW
T _S	Maximum safety temperature ⁽¹⁾				150	°C
D-8 PACKAGE						
I _S	Safety input, output, or supply current ⁽¹⁾	R _{θJA} = 137.7 °C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 5			165	mA
		R _{θJA} = 137.7 °C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 5			252	
		R _{θJA} = 137.7 °C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 5			330	
P _S	Safety input, output, or total power ⁽¹⁾	R _{θJA} = 137.7 °C/W, T _J = 150°C, T _A = 25°C, see Figure 6			908	mW
T _S	Maximum safety temperature ⁽¹⁾				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{θJA}, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$$T_J = T_A + R_{\theta JA} \times P, \text{ where } P \text{ is the power dissipated in the device.}$$

$$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S, \text{ where } T_{J(max)} \text{ is the maximum allowed junction temperature.}$$

$$P_S = I_S \times V_I, \text{ where } V_I \text{ is the maximum input voltage.}$$

6.9 Electrical Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -4\text{ mA}$; see Figure 15	$V_{CCO}^{(1)} - 0.4$	4.8		V
V_{OL}	Low-level output voltage $I_{OL} = 4\text{ mA}$; see Figure 15		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input threshold voltage	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common-mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 17	85	100		$\text{kV}/\mu\text{s}$
C_I	Input Capacitance ⁽²⁾ $V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$		2		pF

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7720							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720), $V_I = 0\text{ V}$ (ISO7720 with F suffix)	I_{CC1}		0.8	1.1	mA	
		I_{CC2}		1.1	1.7		
	$V_I = 0\text{ V}$ (ISO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)	I_{CC1}		2.9	4.2		
		I_{CC2}		1.2	1.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		1.8		2.7
			I_{CC2}		1.3		1.9
		10 Mbps	I_{CC1}		1.9		2.7
			I_{CC2}		2.2		3
		100 Mbps	I_{CC1}		2.5	3.2	
			I_{CC2}		11.6	14	
ISO7721							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721), $V_I = 0\text{ V}$ (ISO7721 with F suffix)	I_{CC1}, I_{CC2}		1	1.6	mA	
		I_{CC1}, I_{CC2}		2.2	3.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		1.7		2.4
			I_{CC1}, I_{CC2}		2.2		3
		10 Mbps	I_{CC1}, I_{CC2}		2.2		3
			I_{CC1}, I_{CC2}		7.3		9

6.11 Electrical Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -2\text{ mA}$; see Figure 15	$V_{CCO}^{(1)} - 0.3$	3.2		V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$; see Figure 15		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold		$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 17	85	100		$\text{kV}/\mu\text{s}$

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.12 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7720							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720), $V_I = 0\text{ V}$ (ISO7720 with F suffix)	I_{CC1}		0.8	1.1	mA	
		I_{CC2}		1.1	1.7		
	$V_I = 0\text{ V}$ (ISO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)	I_{CC1}		2.9	4.2		
		I_{CC2}		1.2	1.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		1.8		2.7
			I_{CC2}		1.2		1.9
		10 Mbps	I_{CC1}		1.9		2.7
			I_{CC2}		1.9		2.6
		100 Mbps	I_{CC1}		2.2	3.1	
			I_{CC2}		8.6	11	
ISO7721							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721), $V_I = 0\text{ V}$ (ISO7721 with F suffix)	I_{CC1}, I_{CC2}		1	1.6	mA	
		I_{CC1}, I_{CC2}		2.2	3.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		1.6		2.4
			I_{CC1}, I_{CC2}		2		2.8
		10 Mbps	I_{CC1}, I_{CC2}		5.6		7
			I_{CC1}, I_{CC2}				

6.13 Electrical Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage $I_{OH} = -1\text{ mA}$; see Figure 15	$V_{CCO}^{(1)} - 0.2$	2.45		V
V_{OL}	Low-level output voltage $I_{OL} = 1\text{ mA}$; see Figure 15		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold		$0.6 \times V_{CCI}$	$0.7 \times V_{CCI}$	V
$V_{IT-(IN)}$	Falling input voltage threshold	$0.3 \times V_{CCI}$	$0.4 \times V_{CCI}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis	$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I_{IH}	High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
I_{IL}	Low-level input current $V_{IL} = 0\text{ V}$ at INx	-10			μA
CMTI	Common-mode transient immunity $V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$; see Figure 17	85	100		$\text{kV}/\mu\text{s}$

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.14 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
ISO7720							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7720), $V_I = 0\text{ V}$ (ISO7720 with F suffix)	I_{CC1}		0.8	1.1	mA	
		I_{CC2}		1.1	1.7		
	$V_I = 0\text{ V}$ (ISO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)	I_{CC1}		2.9	4.2		
		I_{CC2}		1.2	1.9		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}		1.8		2.7
			I_{CC2}		1.3		1.9
		10 Mbps	I_{CC1}		1.9		2.7
			I_{CC2}		1.7		2.4
		100 Mbps	I_{CC1}		2.2	3	
			I_{CC2}		6.8	9	
ISO7721							
Supply current - DC signal	$V_I = V_{CCI}$ (ISO7721), $V_I = 0\text{ V}$ (ISO7721 with F suffix)	I_{CC1}, I_{CC2}		1	1.6	mA	
	$V_I = 0\text{ V}$ (ISO7721), $V_I = V_{CCI}$ (ISO7721 with F suffix)	I_{CC1}, I_{CC2}		2.2	3.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	I_{CC1}, I_{CC2}		1.6		2.4
		10 Mbps	I_{CC1}, I_{CC2}		1.9		2.7
		100 Mbps	I_{CC1}, I_{CC2}		4.6		6

6.15 Switching Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL} Propagation delay time	See Figure 15	6	11	16	ns
PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $			0.5	4.9	ns
$t_{sk(o)}$ Channel-to-channel output skew time ⁽²⁾	Same direction channels			4	ns
$t_{sk(pp)}$ Part-to-part skew time ⁽³⁾				4.5	ns
t_r Output signal rise time	See Figure 15		1.8	3.9	ns
t_f Output signal fall time				1.9	3.9
t_{DO} Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 16		0.1	0.3	μ s
t_{ie} Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL} Propagation delay time	See Figure 15	6	11	16	ns
PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				0.5	5
$t_{sk(o)}$ Channel-to-channel output skew time ⁽²⁾	Same direction channels			4.1	ns
$t_{sk(pp)}$ Part-to-part skew time ⁽³⁾				4.5	ns
t_r Output signal rise time	See Figure 15		0.7	3	ns
t_f Output signal fall time				0.7	3
t_{DO} Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 16		0.1	0.3	μ s
t_{ie} Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} , t_{PHL} Propagation delay time	See Figure 15	7.5	12	18.5	ns
PWD Pulse width distortion ⁽¹⁾ $ t_{PHL} - t_{PLH} $				0.5	5.1
$t_{sk(o)}$ Channel-to-channel output skew time ⁽²⁾	Same direction channels			4.1	ns
$t_{sk(pp)}$ Part-to-part skew time ⁽³⁾				4.6	ns
t_r Output signal rise time	See Figure 15		1	3.5	ns
t_f Output signal fall time				1	3.5
t_{DO} Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 16		0.1	0.3	μ s
t_{ie} Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

- (1) Also known as pulse skew.
- (2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

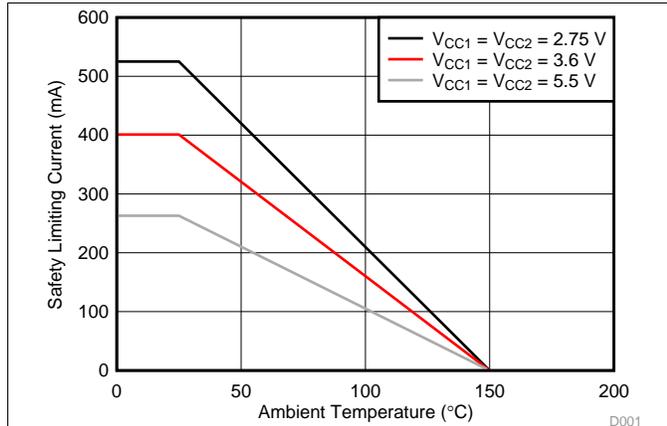


Figure 1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

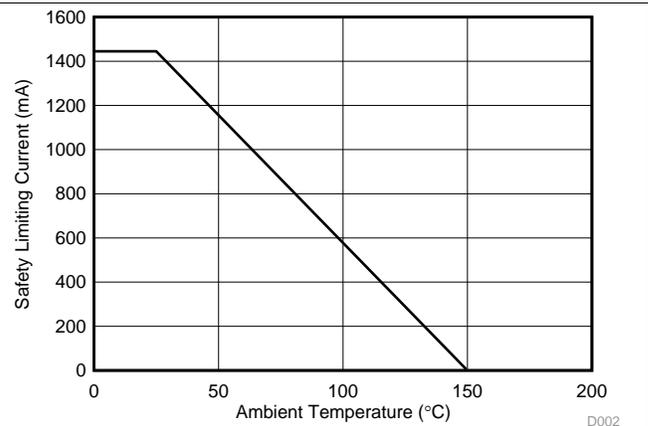


Figure 2. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

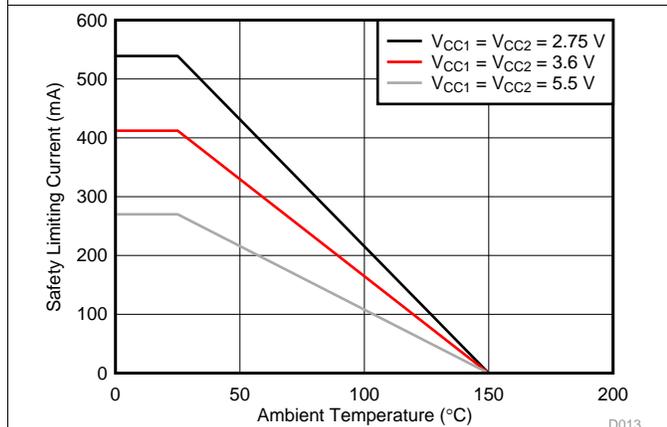


Figure 3. Thermal Derating Curve for Limiting Current per VDE for DWV-8 Package

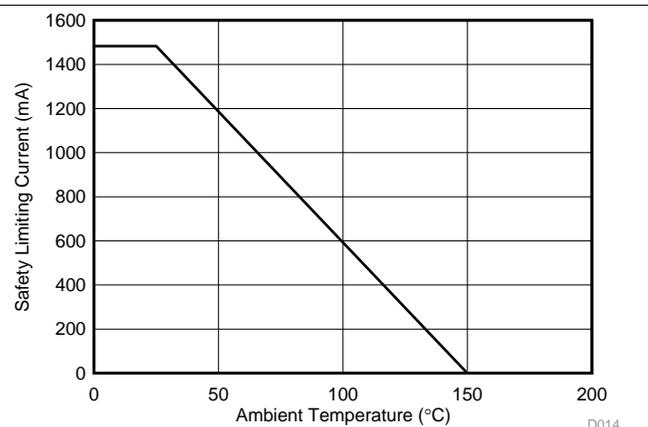


Figure 4. Thermal Derating Curve for Limiting Power per VDE for DWV-8 Package

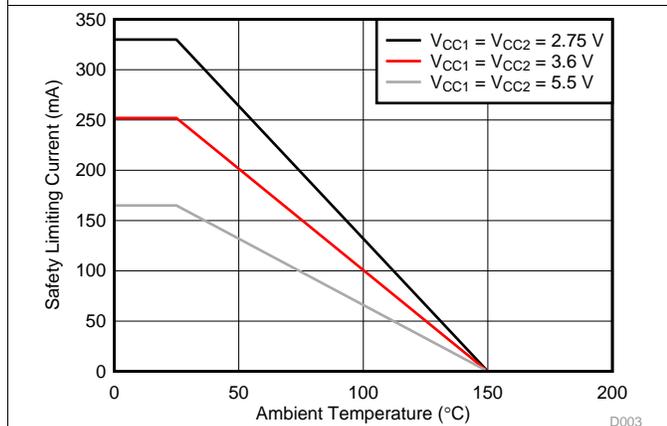


Figure 5. Thermal Derating Curve for Limiting Current per VDE for D-8 Package

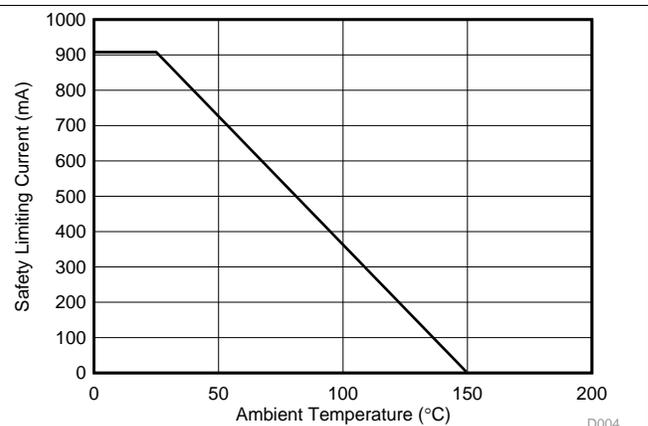
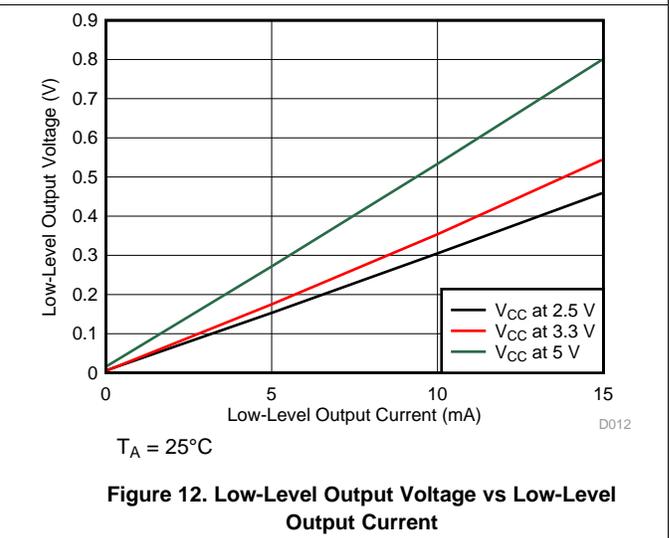
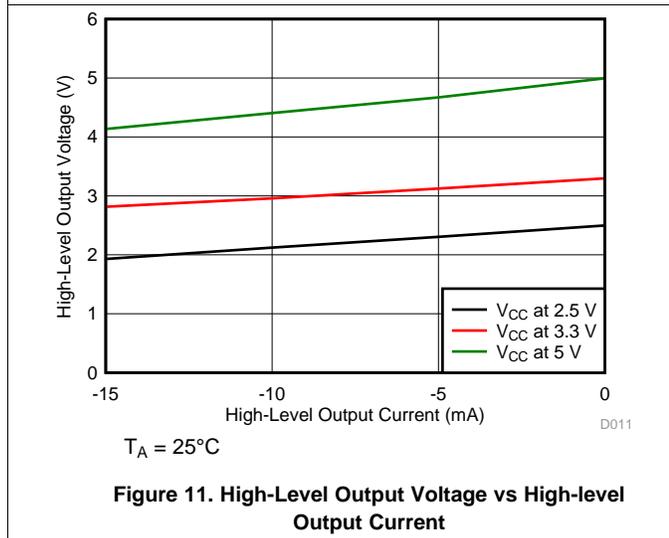
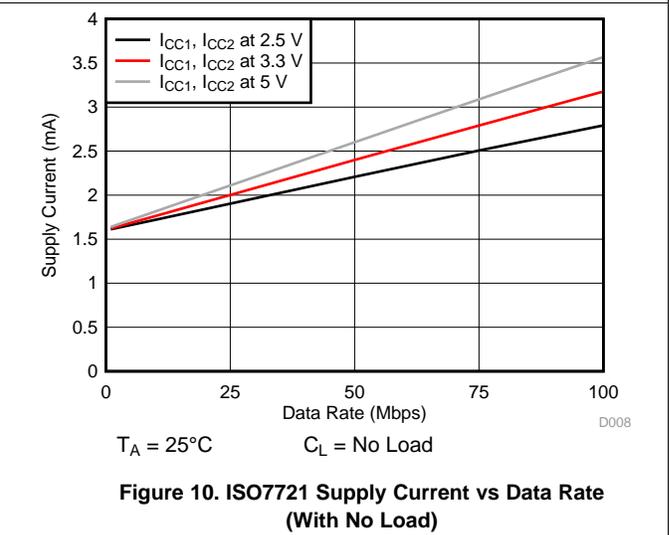
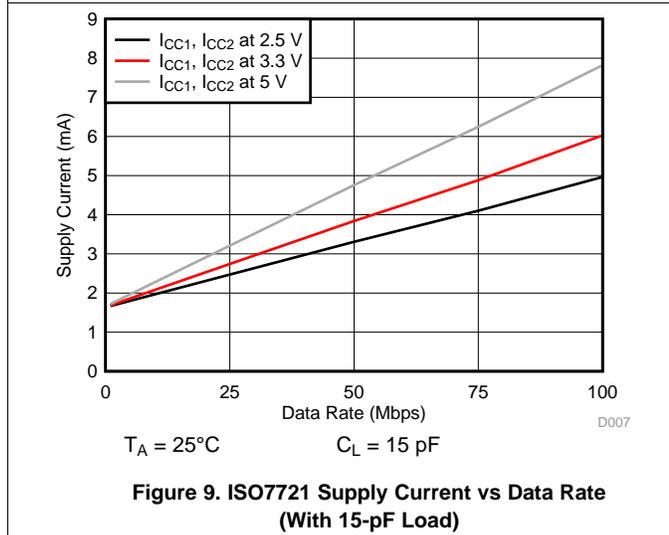
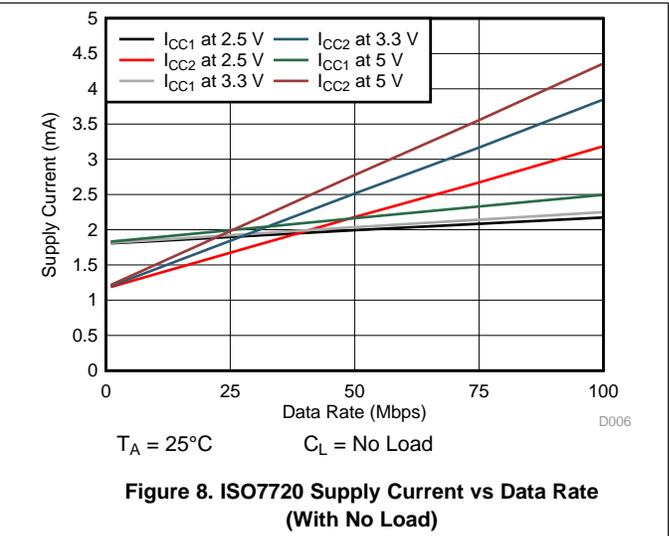
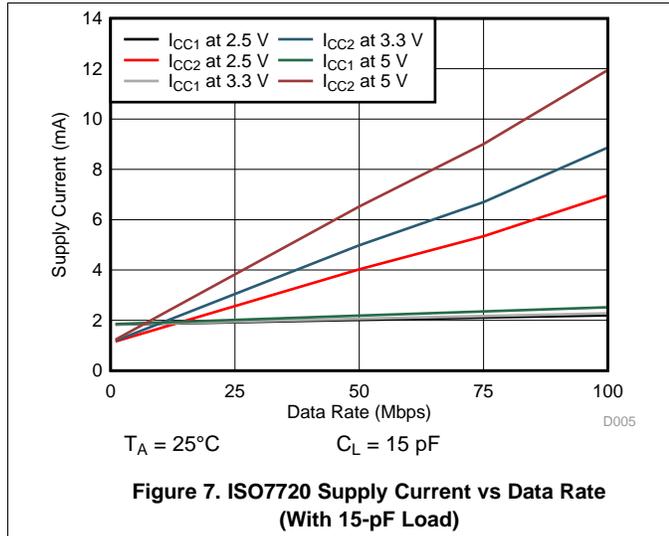
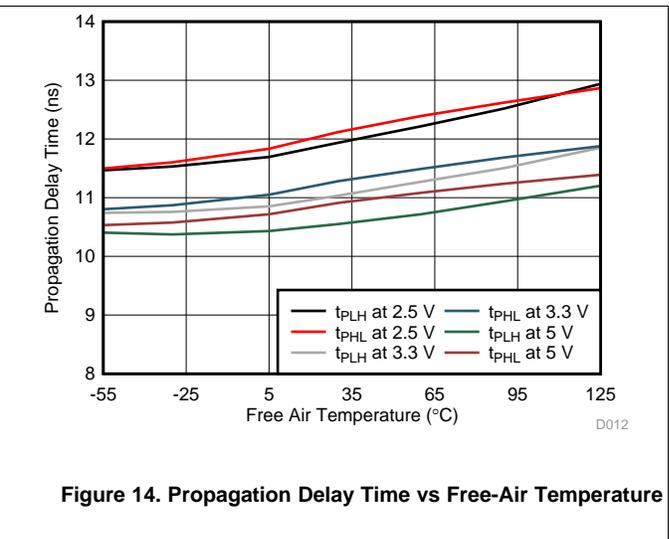
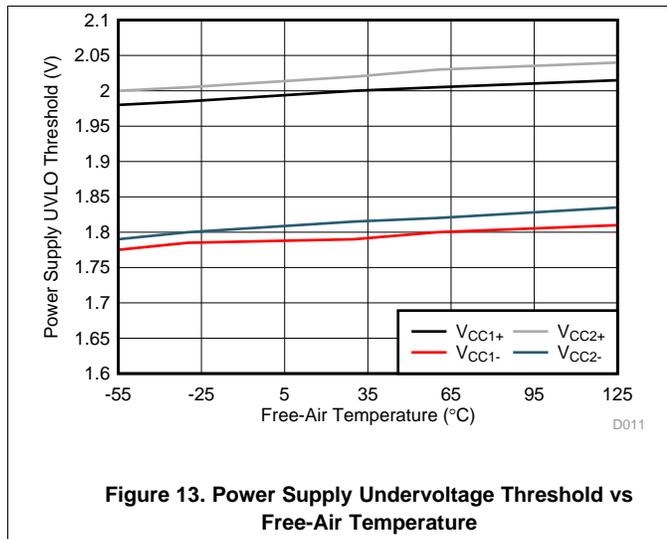


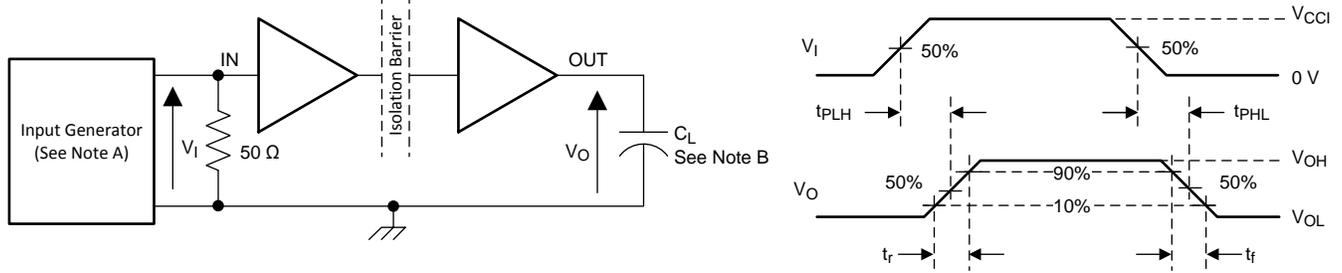
Figure 6. Thermal Derating Curve for Limiting Power per VDE for D-8 Package

6.19 Typical Characteristics



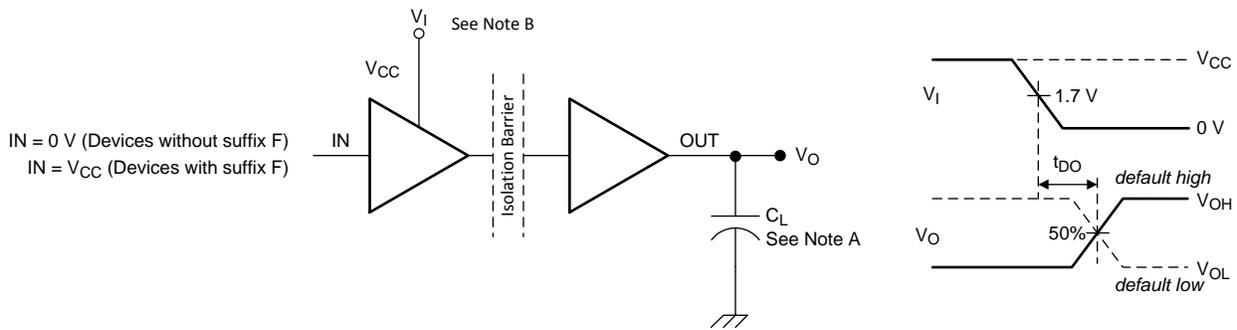
Typical Characteristics (continued)


7 Parameter Measurement Information



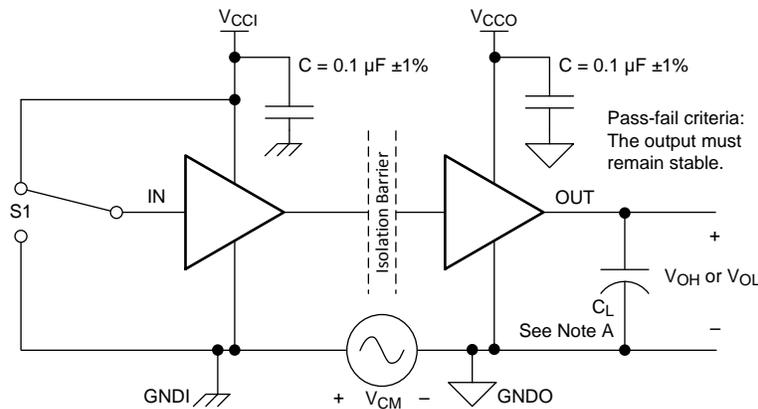
- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within ±20%.

Figure 15. Switching Characteristics Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within ±20%.
- B. Power Supply Ramp Rate = 10 mV/ns

Figure 16. Default Output Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within ±20%.

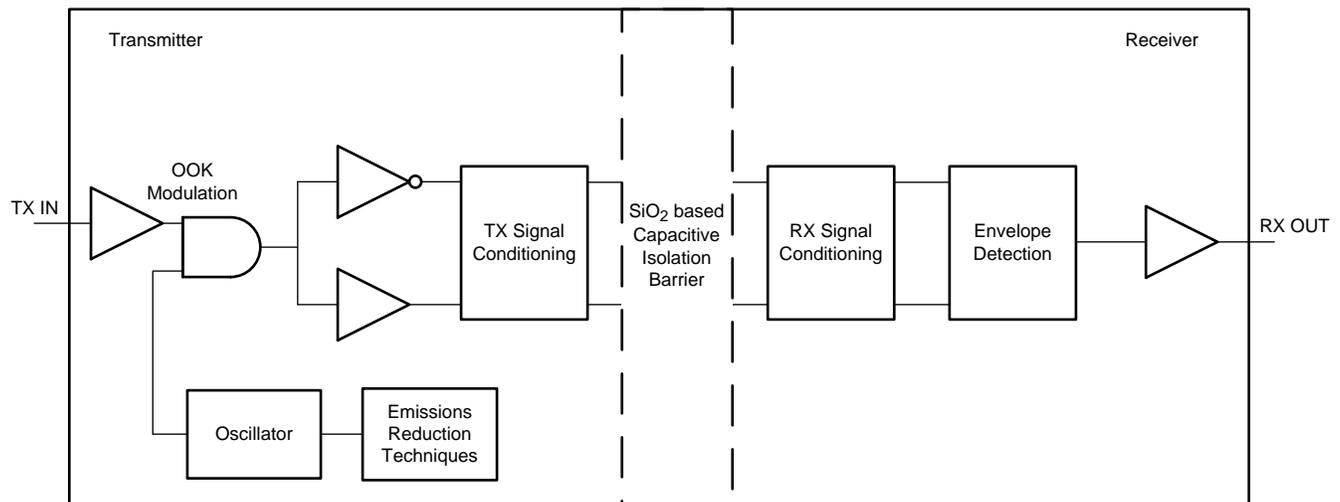
Figure 17. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO772x family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 18](#), shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram



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Figure 18. Conceptual Block Diagram of a Digital Capacitive Isolator

[Figure 19](#) shows a conceptual detail of how the OOK scheme works.

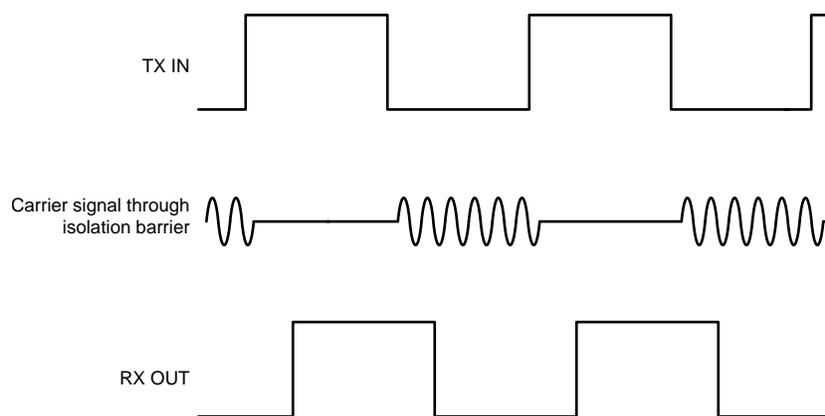


Figure 19. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISO772x family of devices is available in two channel configurations and default output state options to enable a variety of application uses. [Table 1](#) lists the device features of the ISO772x devices.

Table 1. Device Features

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION ⁽¹⁾
ISO7720	100 Mbps	2 Forward, 0 Reverse	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DWV-8	5000 V _{RMS} / 7071 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}
ISO7720F	100 Mbps	2 Forward, 0 Reverse	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DWV-8	5000 V _{RMS} / 7071 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}
ISO7721	100 Mbps	1 Forward, 1 Reverse	High	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DWV-8	5000 V _{RMS} / 7071 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}
ISO7721F	100 Mbps	1 Forward, 1 Reverse	Low	DW-16	5000 V _{RMS} / 8000 V _{PK}
				DWV-8	5000 V _{RMS} / 7071 V _{PK}
				D-8	3000 V _{RMS} / 4242 V _{PK}

(1) See the [Safety-Related Certifications](#) section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO772x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

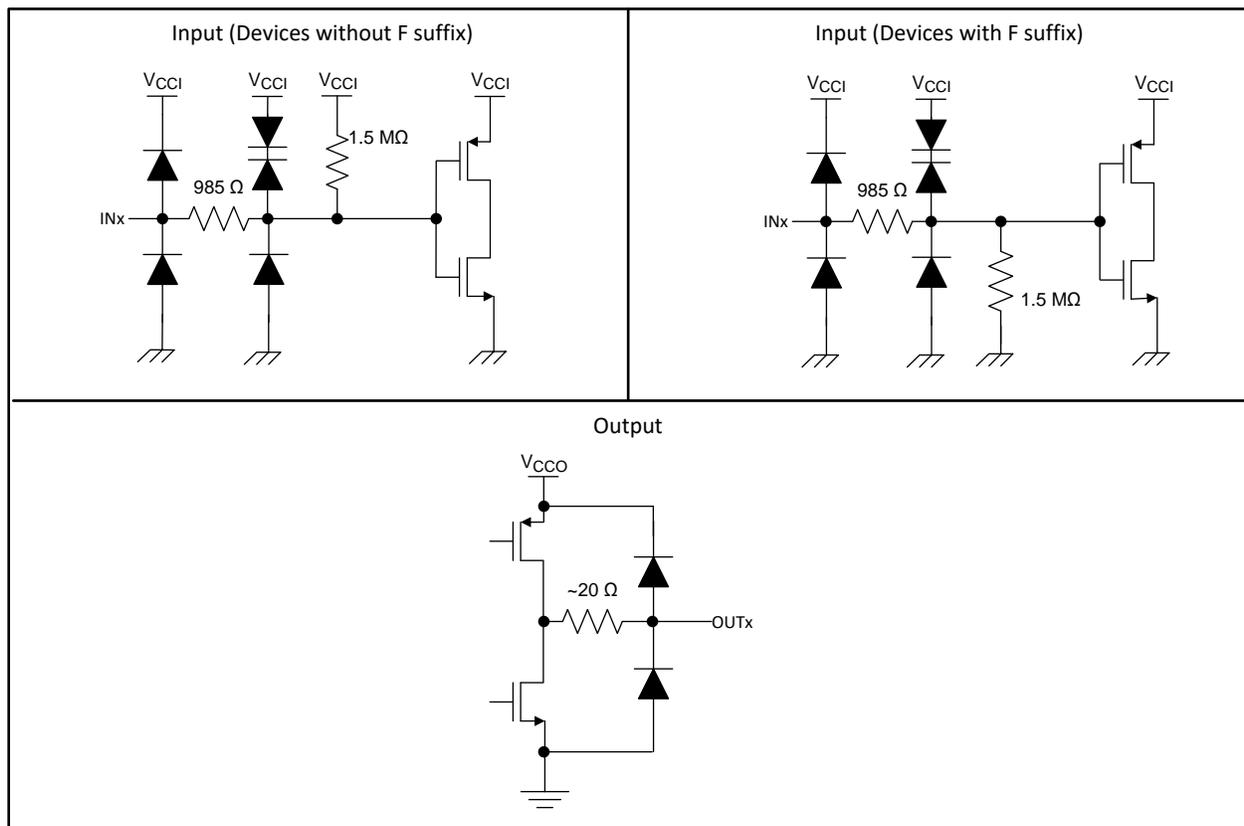
Table 2 lists the functional modes for the ISO772x devices.

Table 2. Function Table⁽¹⁾

V _{CCI}	V _{CCO}	INPUT (IN _x) ⁽²⁾	OUTPUT (OUT _x)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When IN _x is open, the corresponding channel output goes to the default logic state. The default is <i>High</i> for ISO772x and <i>Low</i> for ISO772x with F suffix.
PD	PU	X	Default	Default mode: When V _{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. The default is <i>High</i> for ISO772x and <i>Low</i> for ISO772x with F suffix. When V _{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V _{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V _{CCO} is unpowered, a channel output is undetermined ⁽³⁾ . When V _{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

- (1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
- (2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
- (3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics



Copyright © 2016, Texas Instruments Incorporated

Figure 20. Device I/O Schematics

9 Application and Implementation

NOTE

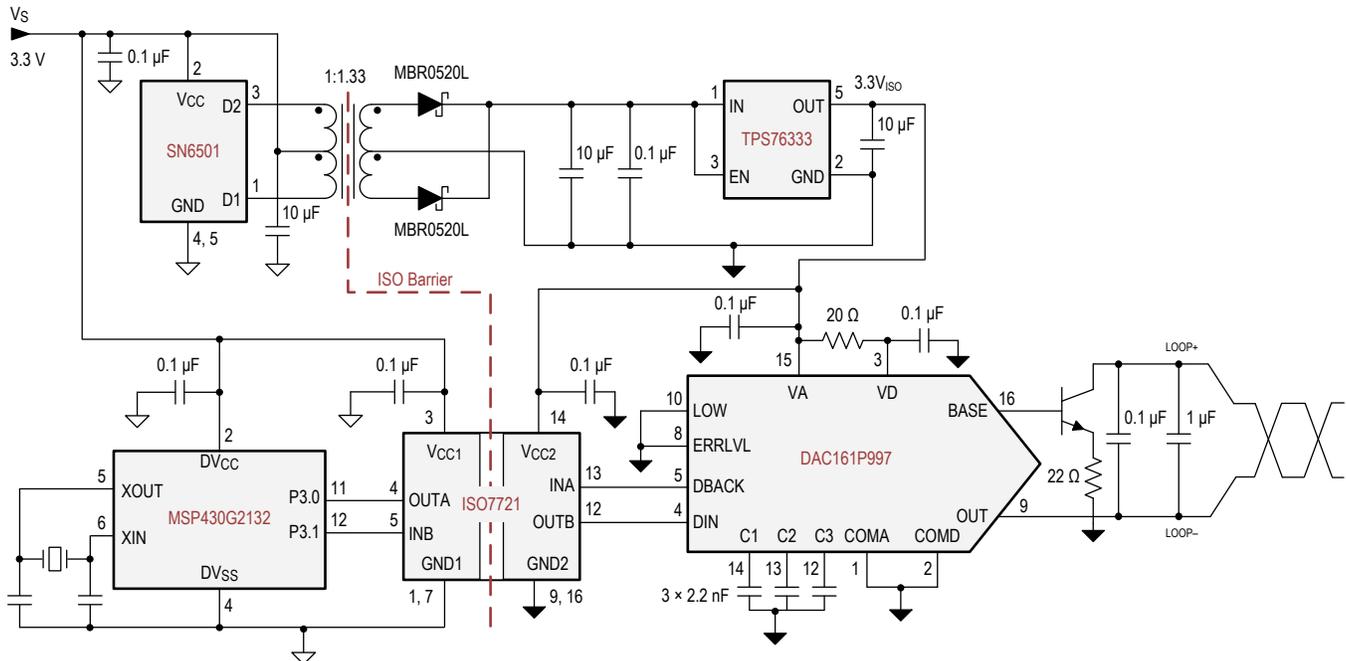
Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO772x devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7721 device can be used with Texas Instruments' mixed signal microcontroller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-mA to 20-mA current loop.



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Figure 21. Isolated 4-mA to 20-mA Current Loop

Typical Application (continued)

9.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 3](#).

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μF
Decoupling capacitor from V_{CC2} and GND2	0.1 μF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO772x devices only require two external bypass capacitors to operate.

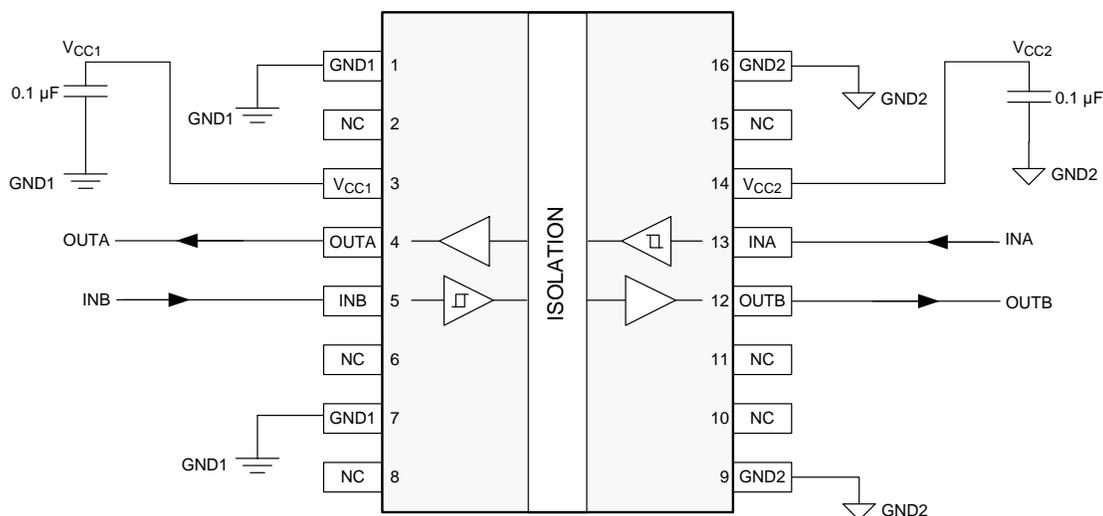
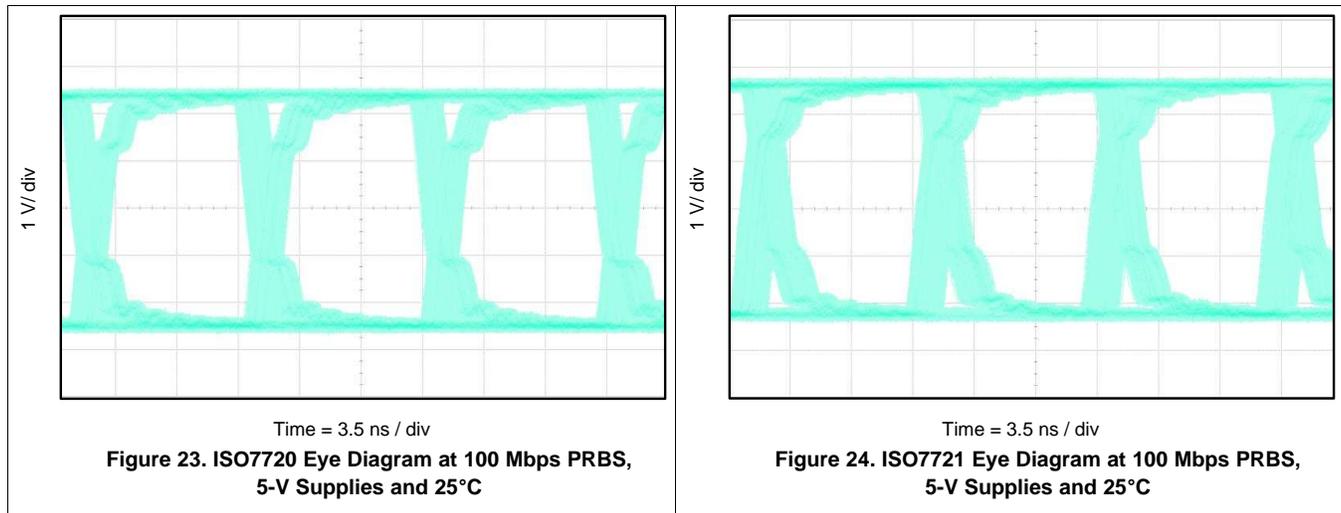


Figure 22. Typical ISO7721 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO772x family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.



9.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 25](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

[Figure 26](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 135 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 and DWV-8 packages is specified up to 1500 V_{RMS} and D-8 package up to 450 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 135 years.

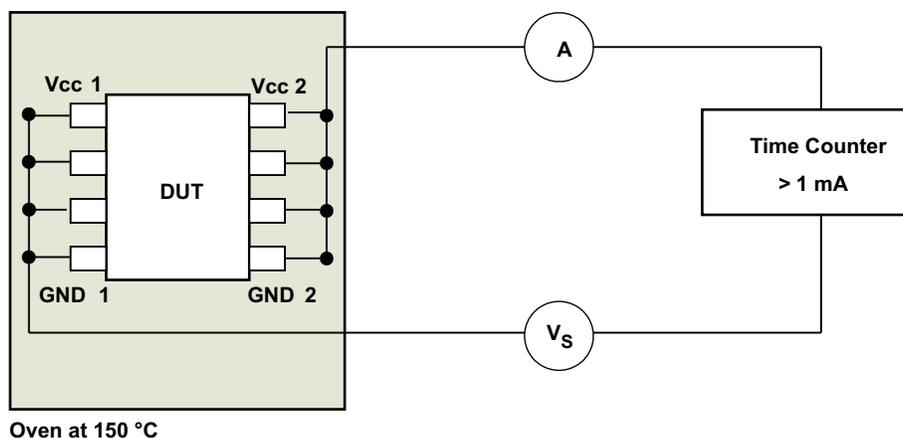


Figure 25. Test Setup for Insulation Lifetime Measurement

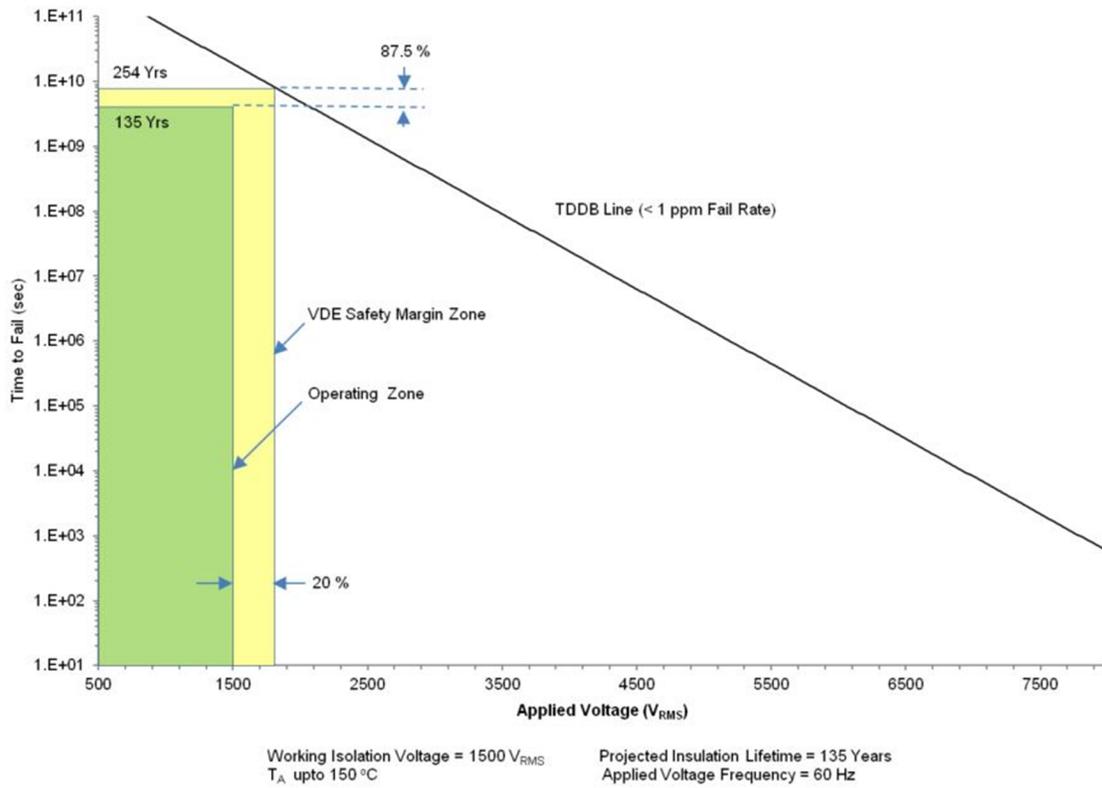


Figure 26. Insulation Lifetime Projection Data

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1- μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501](#) or [SN6505A](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies](#) or [SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 27](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

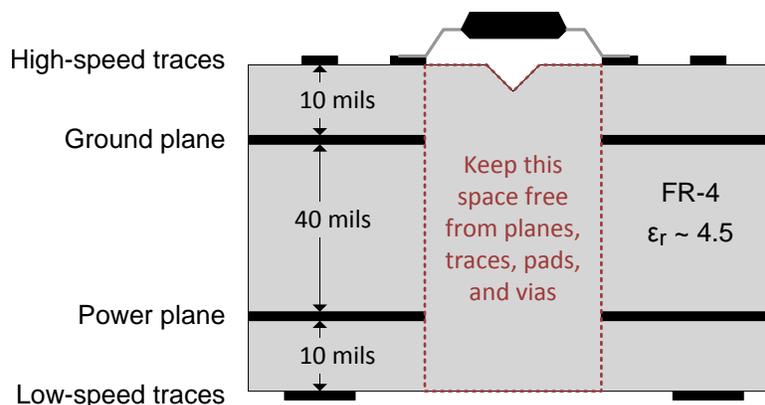


Figure 27. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For development support, refer to:

- [Isolated CAN Flexible Data \(FD\) Rate Repeater Reference Design](#)
- [Isolated 16-Channel AC Analog Input Module Reference Design Using Dual Simultaneously Sampled ADCs](#)
- [Polyphase Shunt Metrology with Isolated AFE Reference Design](#)
- [Reference Design for Power-Isolated Ultra-Compact Analog Output Module](#)

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [How to use isolation to improve ESD, EFT and Surge immunity in industrial systems application report](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops data sheet](#)
- Texas Instruments, [MSP430G2132 Mixed Signal Microcontroller data sheet](#)
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#)
- Texas Instruments, [TPS76333 Low-Power 150-mA Low-Dropout Linear Regulators data sheet](#)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7720	Click here				
ISO7721	Click here				

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

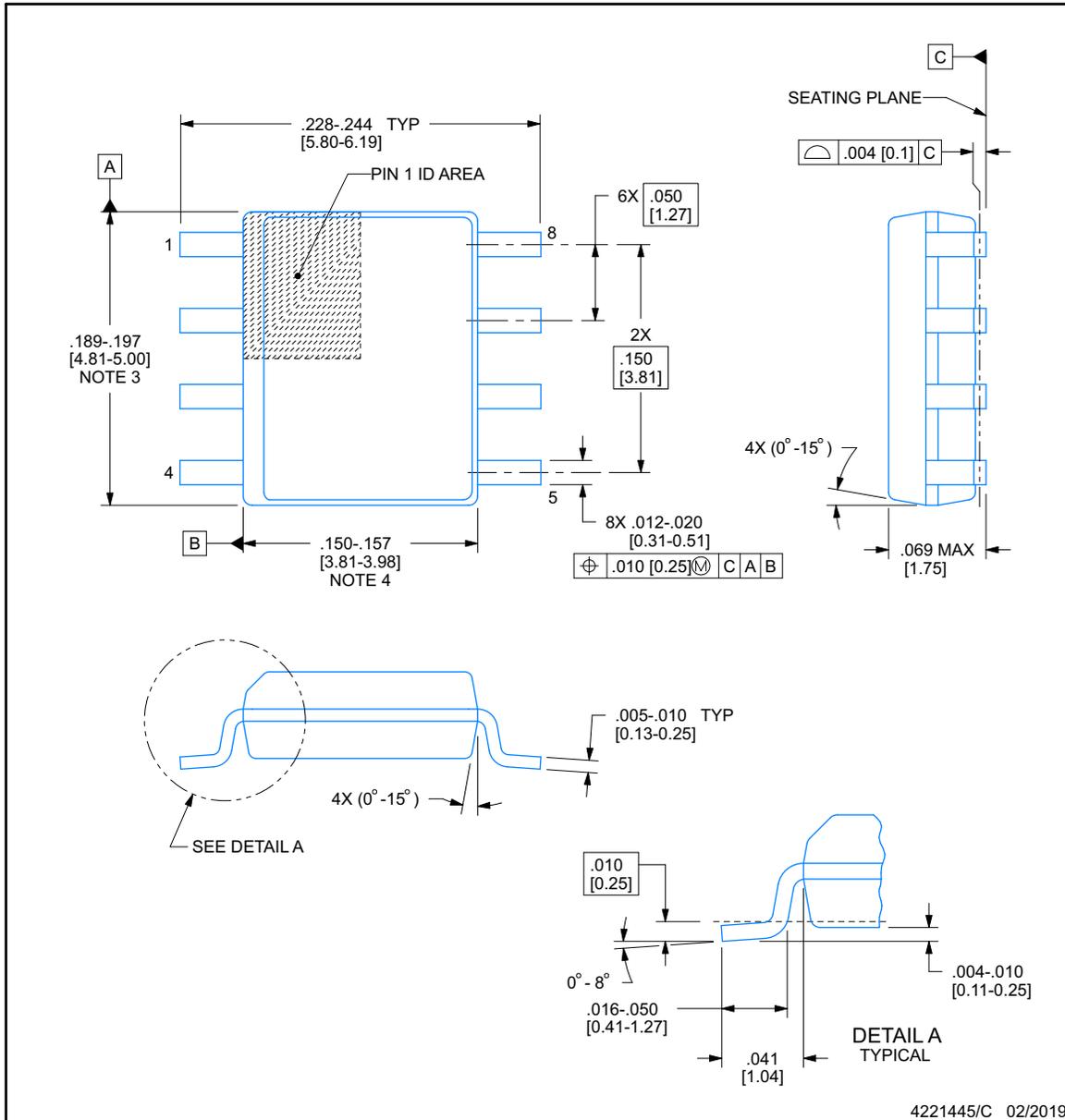


D0008B

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

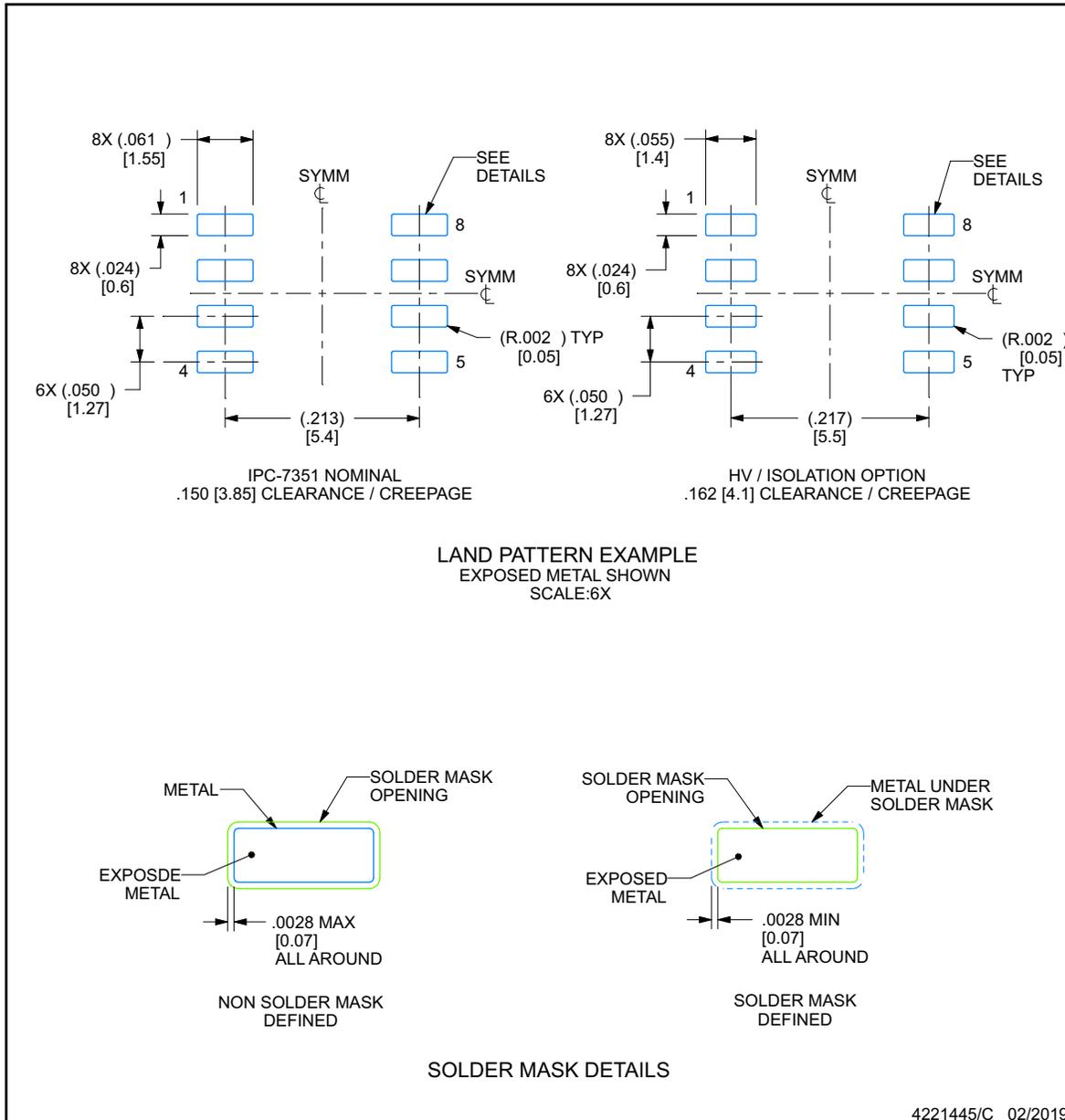
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

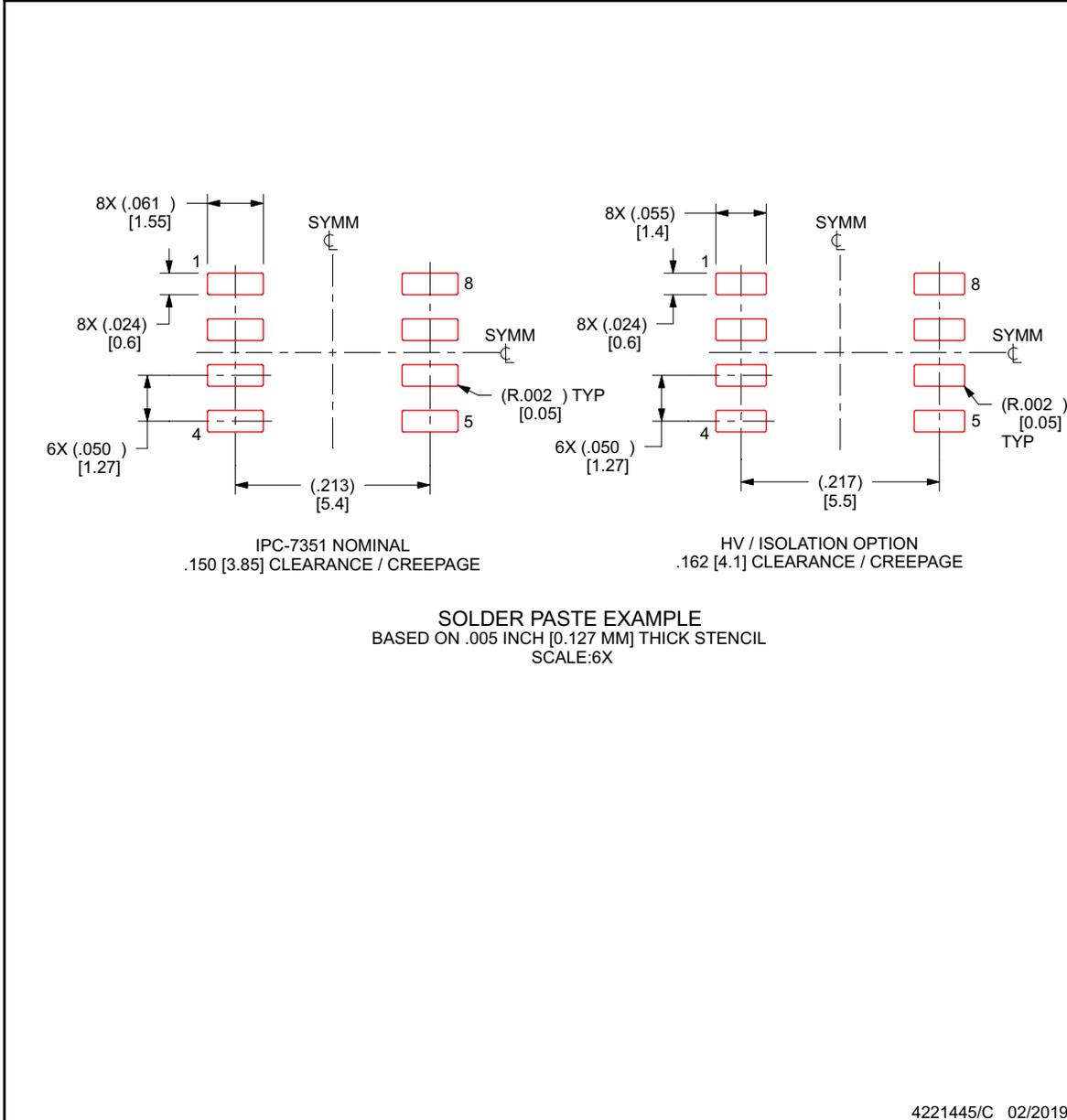
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

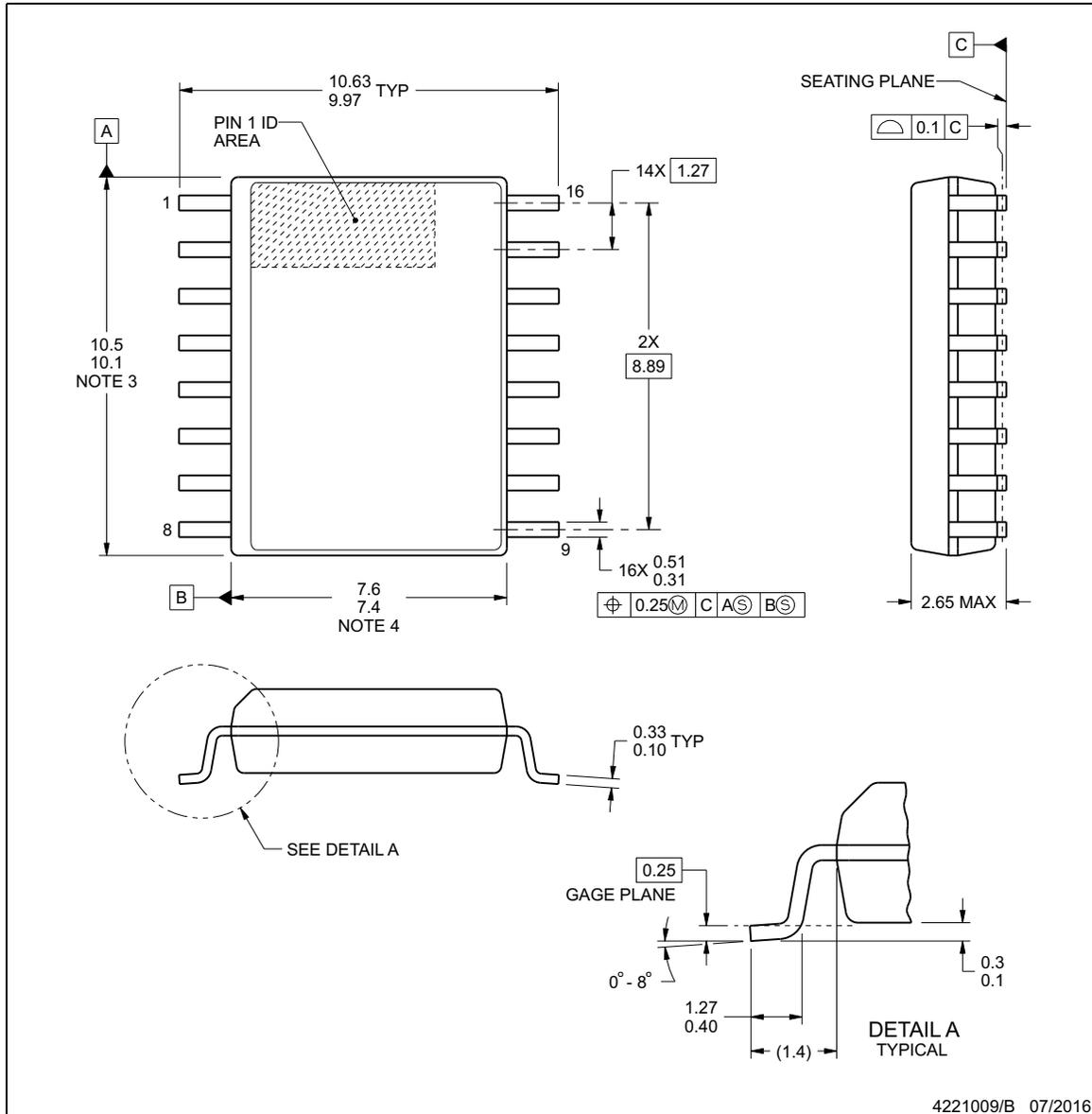


NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.


DW0016B
PACKAGE OUTLINE
SOIC - 2.65 mm max height

SOIC


NOTES:

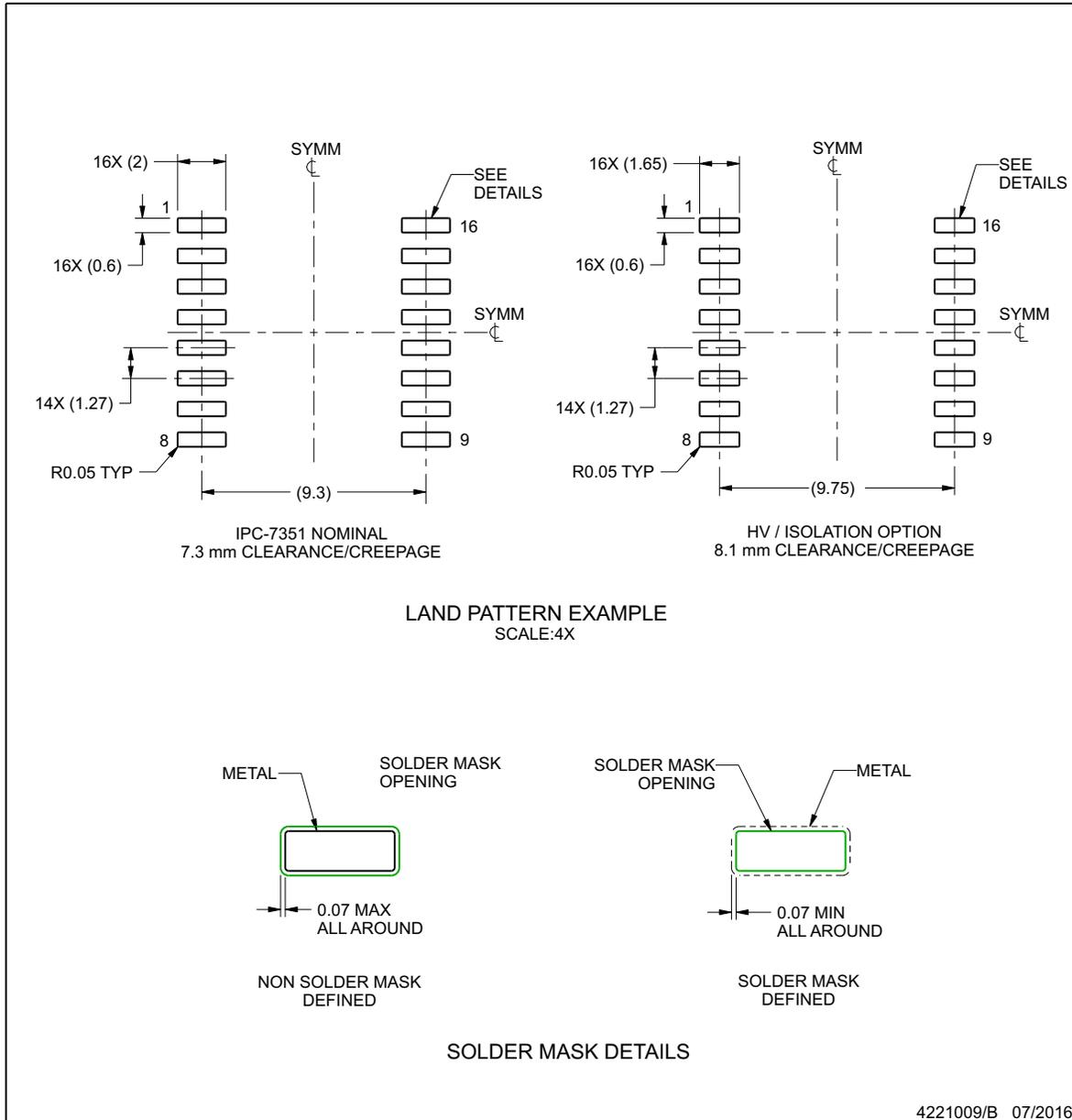
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

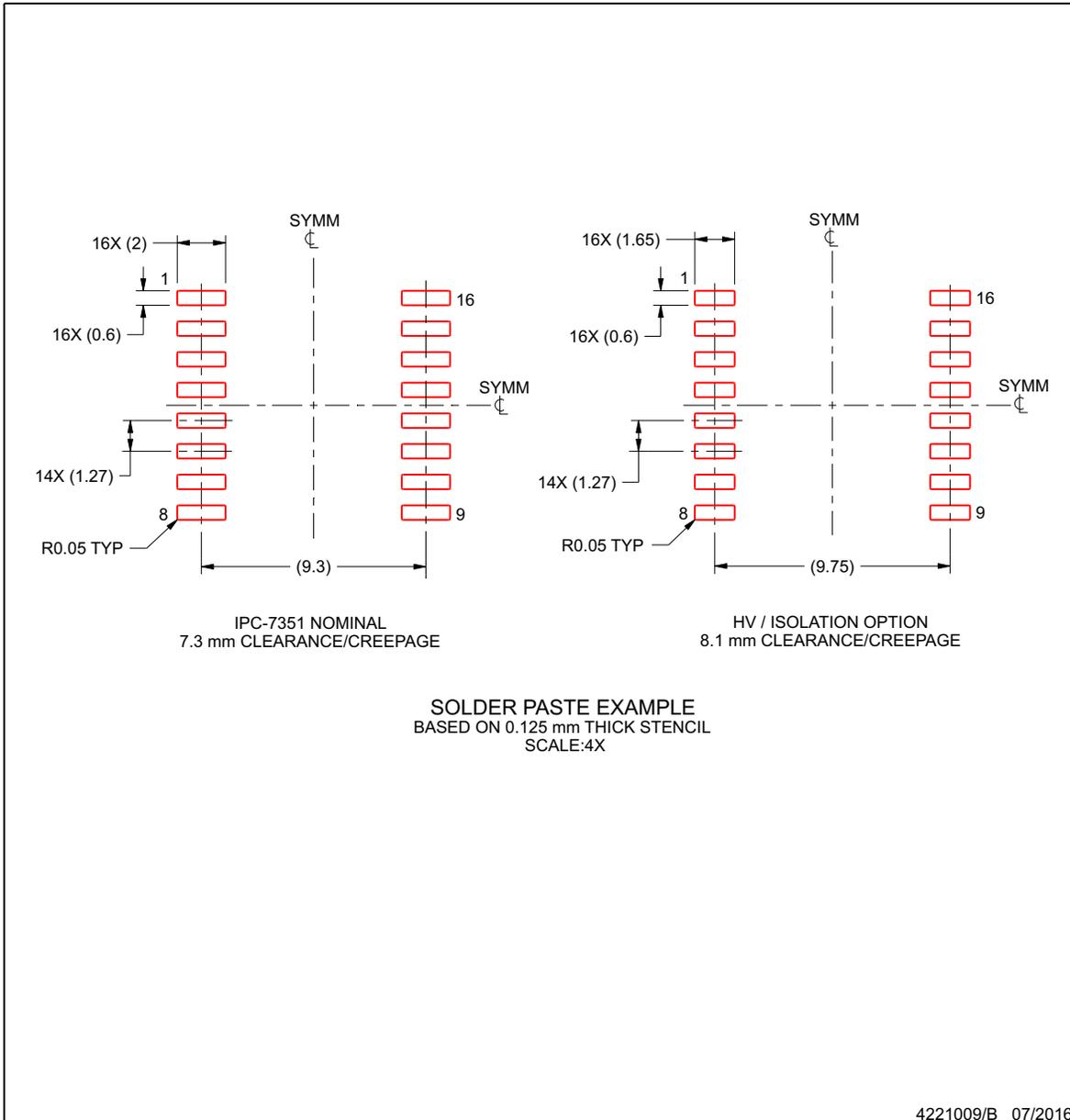
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

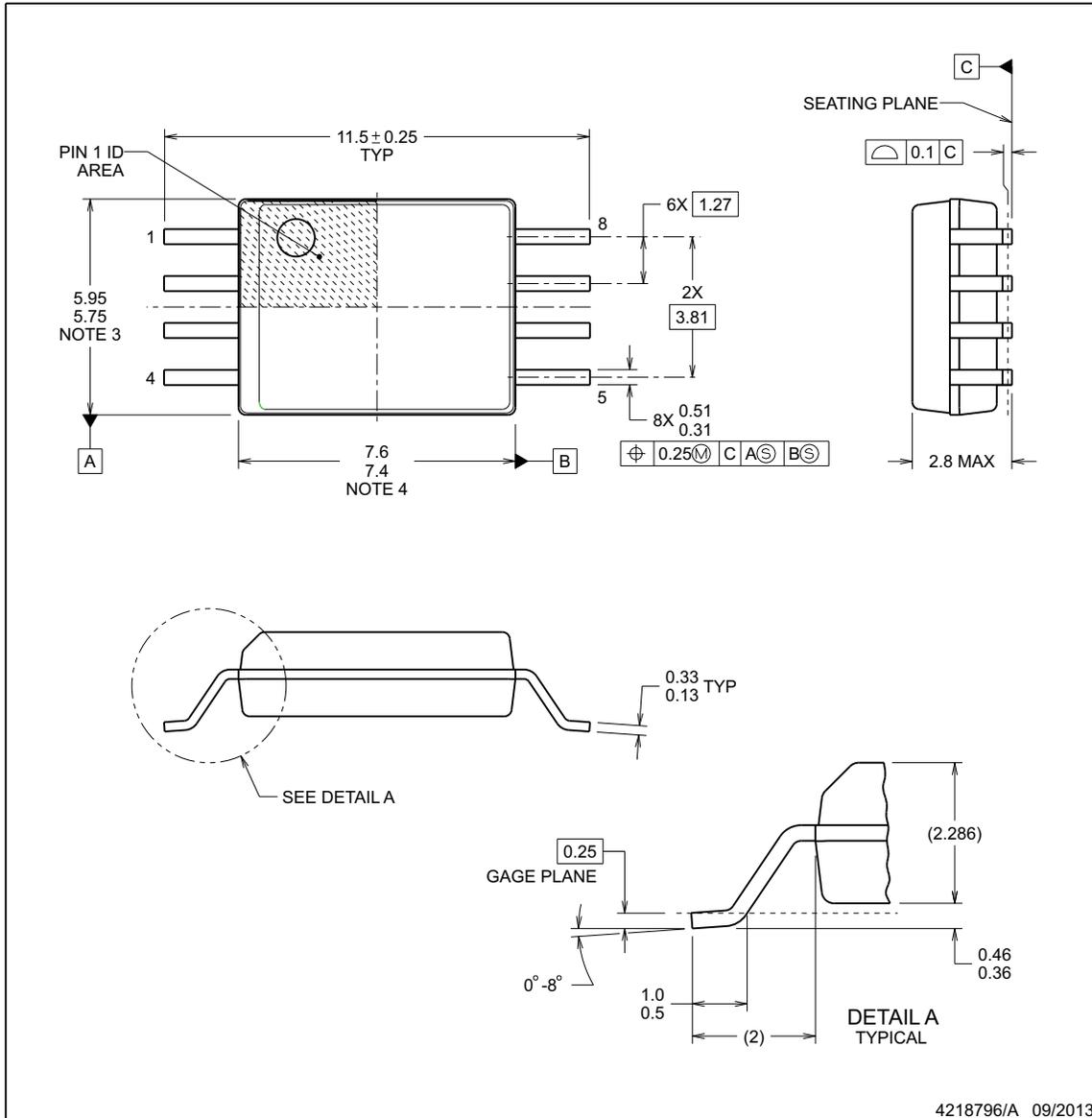
PACKAGE OUTLINE

DWV0008A



SOIC - 2.8 mm max height

SOIC



NOTES:

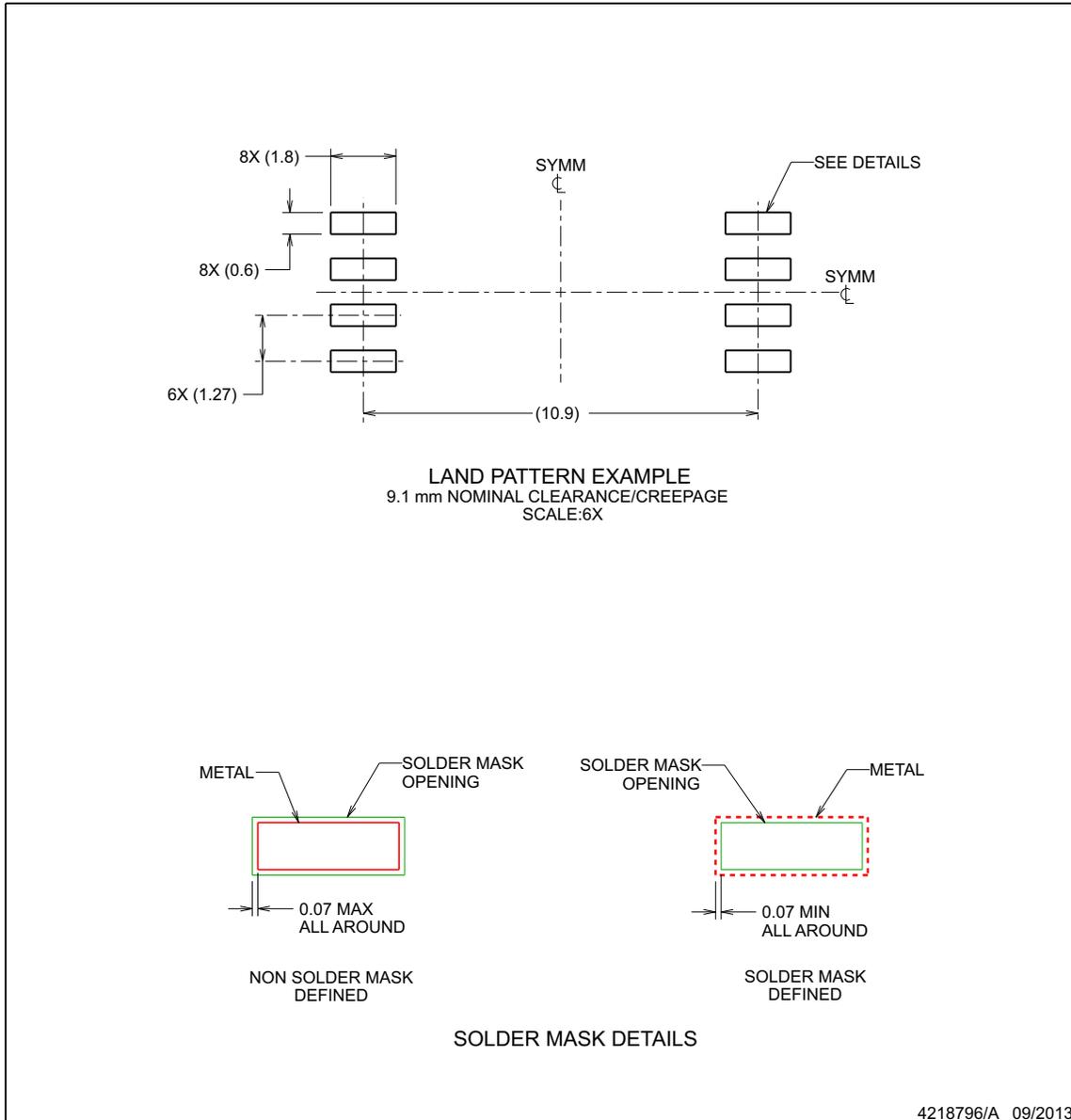
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

DWV0008A

SOIC - 2.8 mm max height

SOIC



NOTES: (continued)

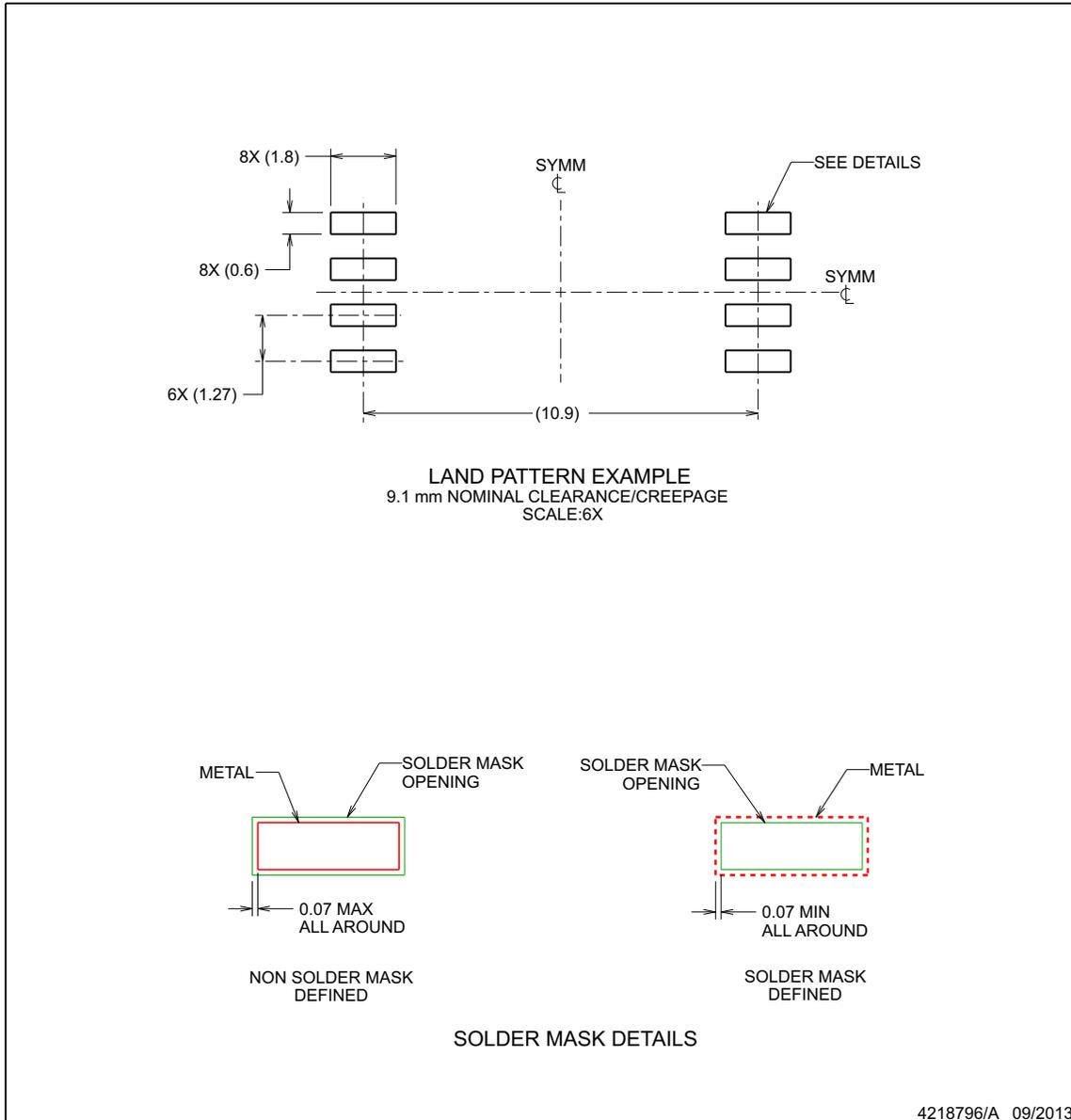
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE BOARD LAYOUT

DWV0008A

SOIC - 2.8 mm max height

SOIC



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7720D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	Samples
ISO7720DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	Samples
ISO7720DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720FD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7720FDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7720FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	Samples
ISO7720FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	Samples
ISO7720FDWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7720FDWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7721D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples
ISO7721DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples
ISO7721DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	Samples
ISO7721DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	Samples
ISO7721DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7721DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples
ISO7721FD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples
ISO7721FDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples
ISO7721FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	Samples
ISO7721FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	Samples
ISO7721FDWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples
ISO7721FDWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

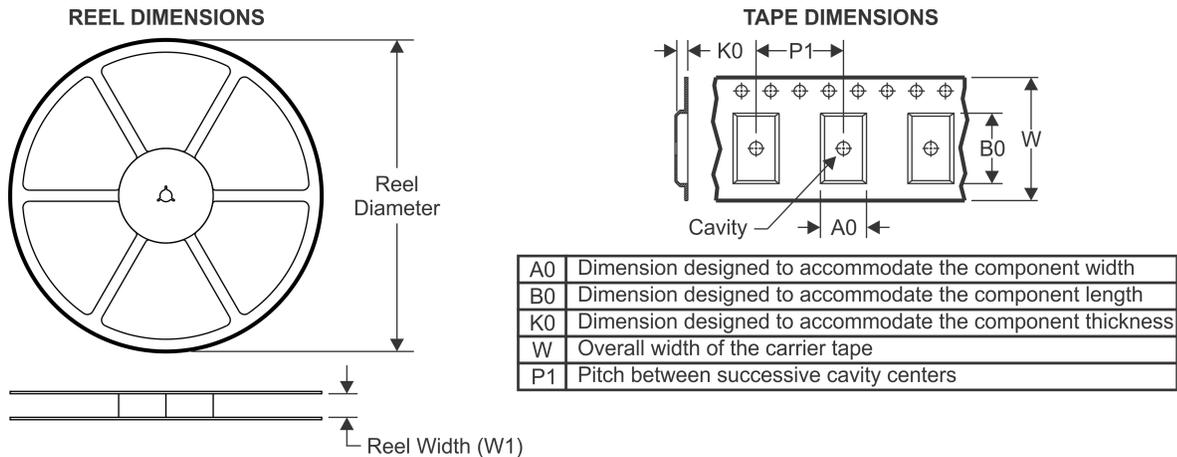
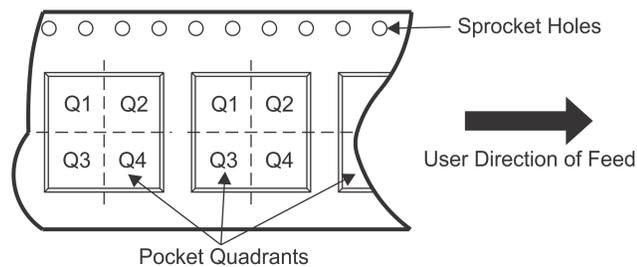
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7720, ISO7721 :

- Automotive: [ISO7720-Q1](#), [ISO7721-Q1](#)

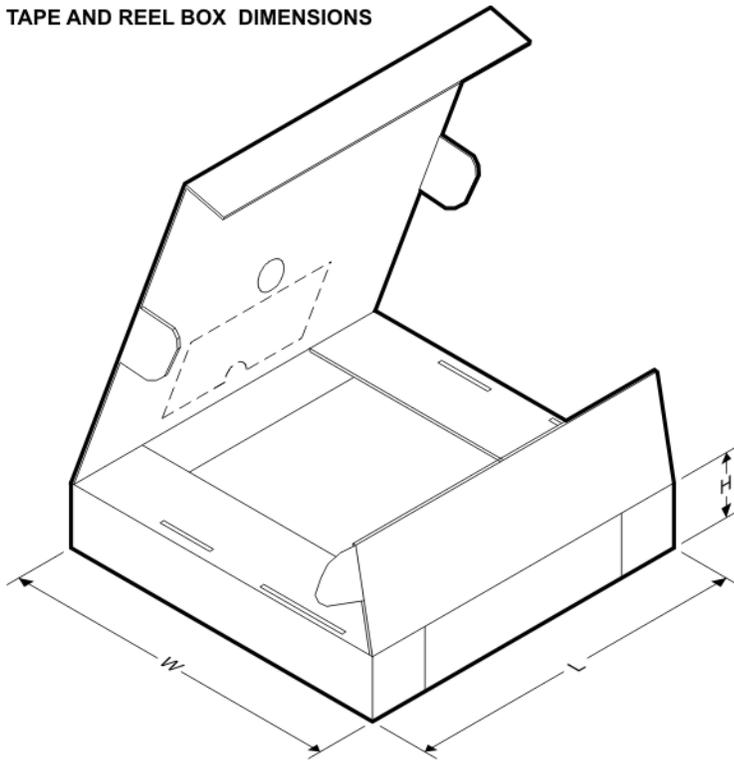
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7720DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7720DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7720FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7720FDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7721DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7721FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721FDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7720DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7720DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO7720FDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7720FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7720FDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO7721DR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7721DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO7721FDR	SOIC	D	8	2500	350.0	350.0	43.0
ISO7721FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7721FDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0

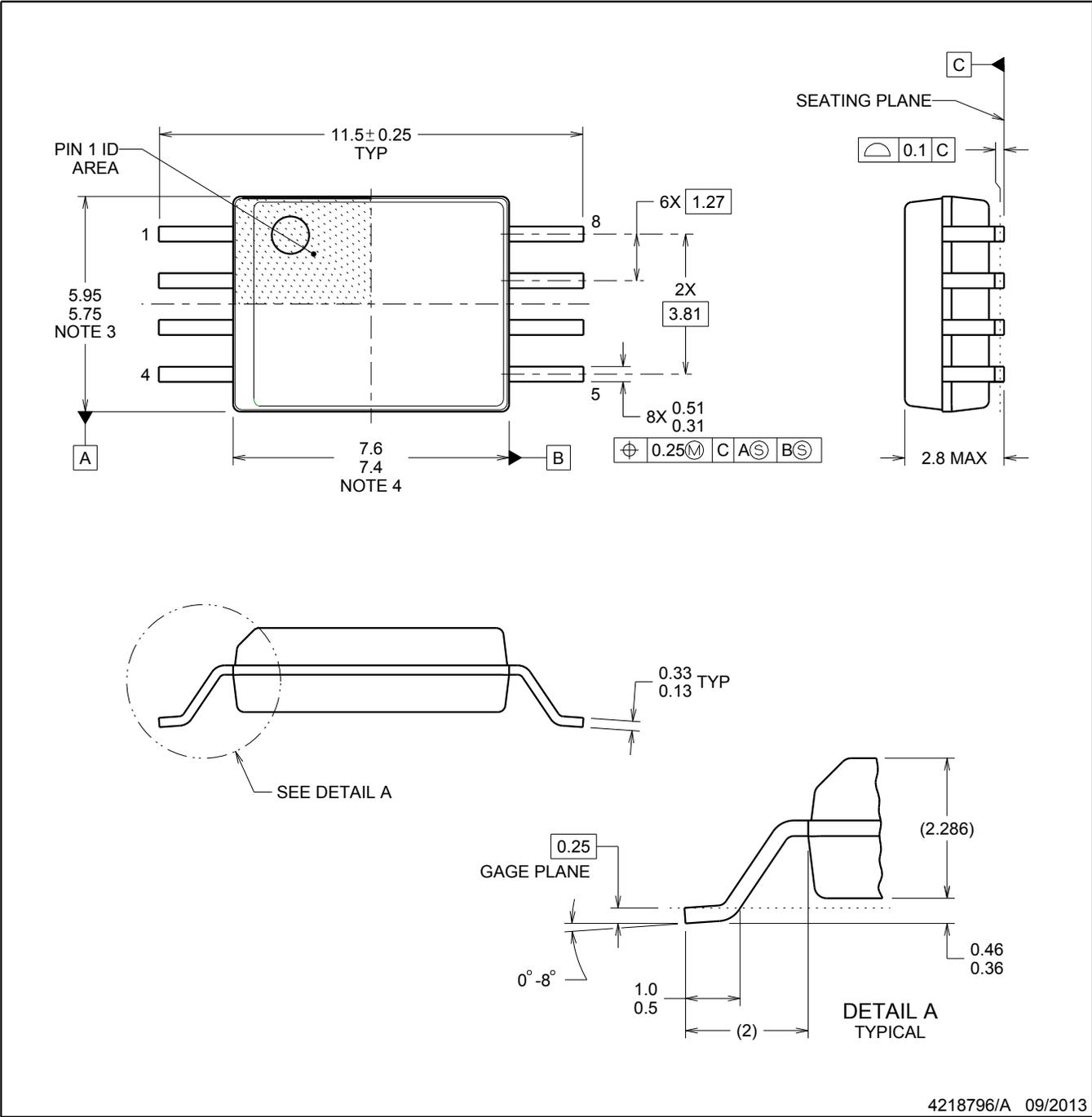
PACKAGE OUTLINE

DWV0008A



SOIC - 2.8 mm max height

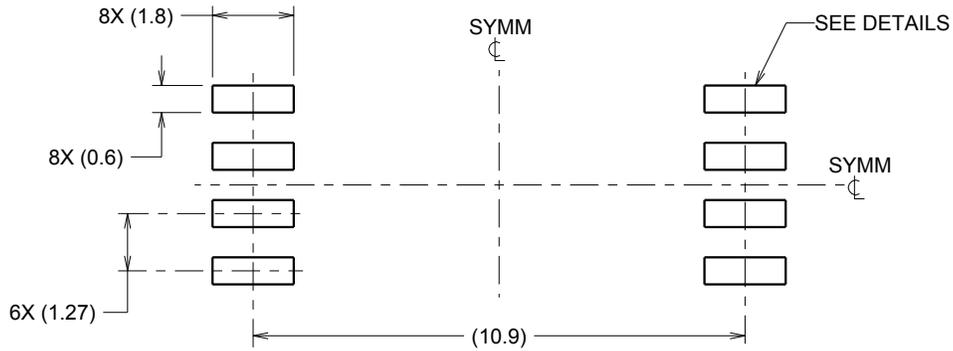
SOIC



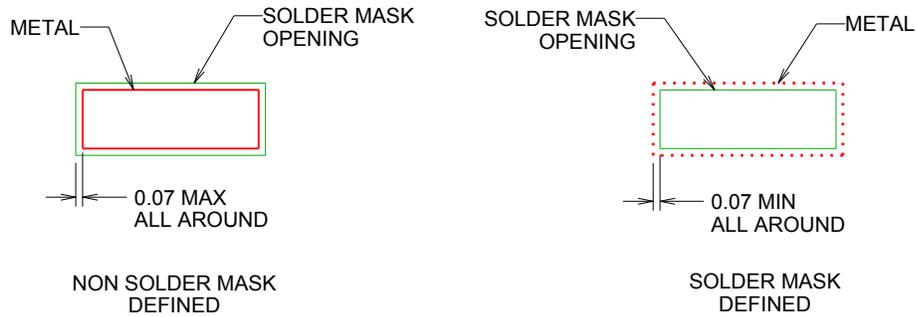
4218796/A 09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

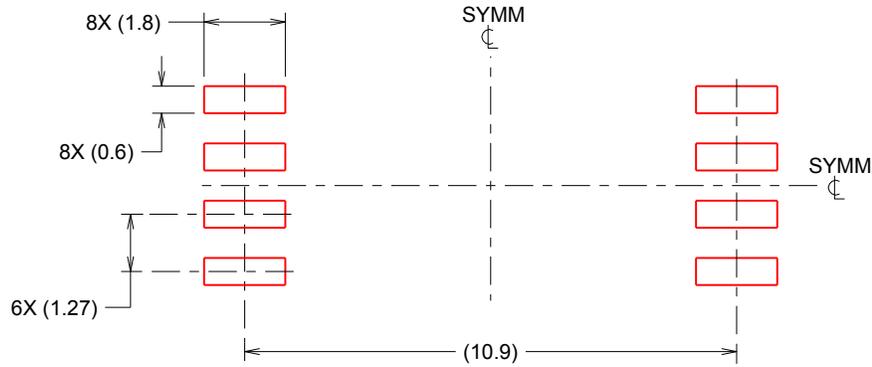


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:6X

4218796/A 09/2013

NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

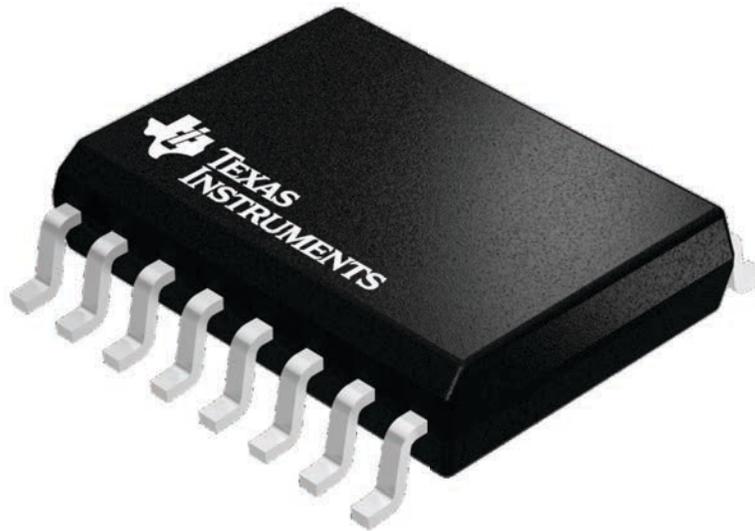
DW 16

SOIC - 2.65 mm max height

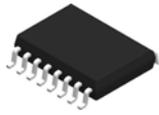
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



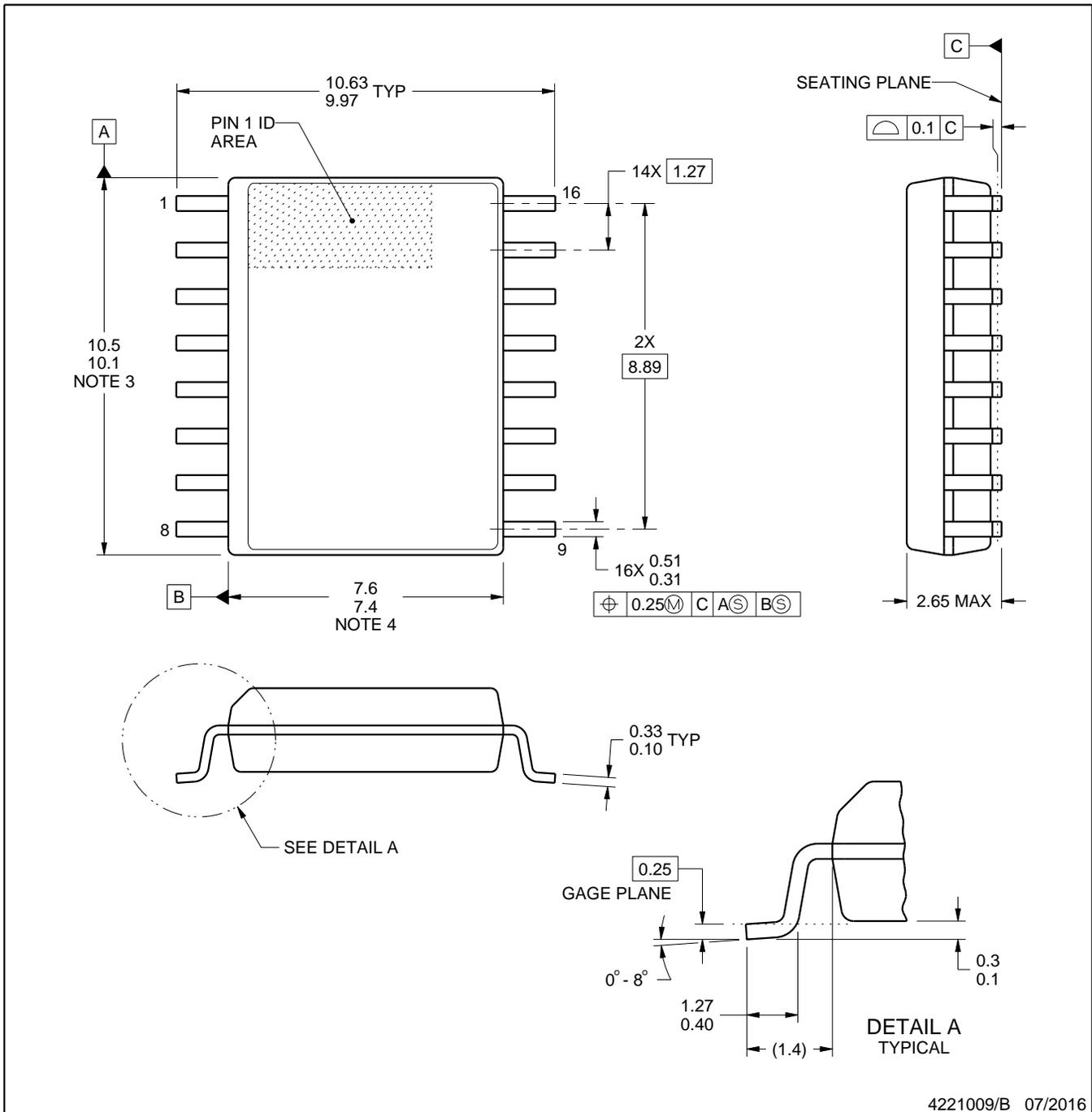
4224780/A



DW0016B

PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

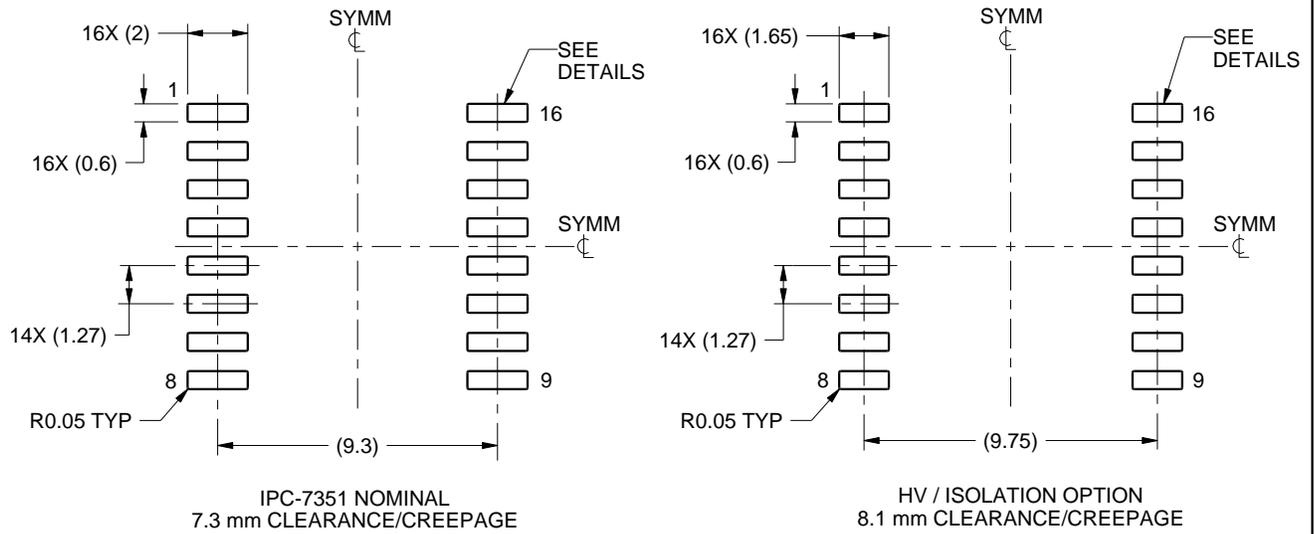
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

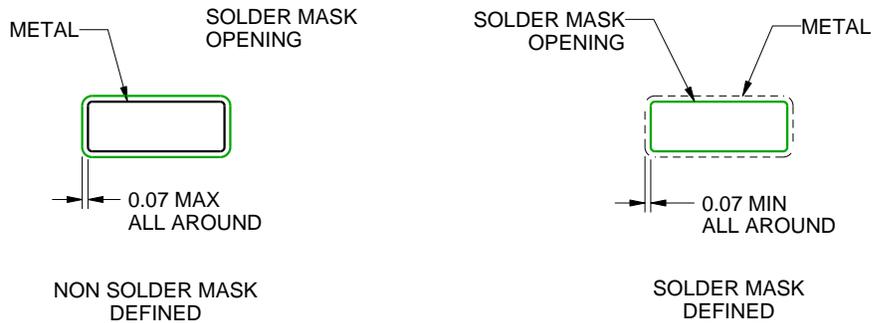
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

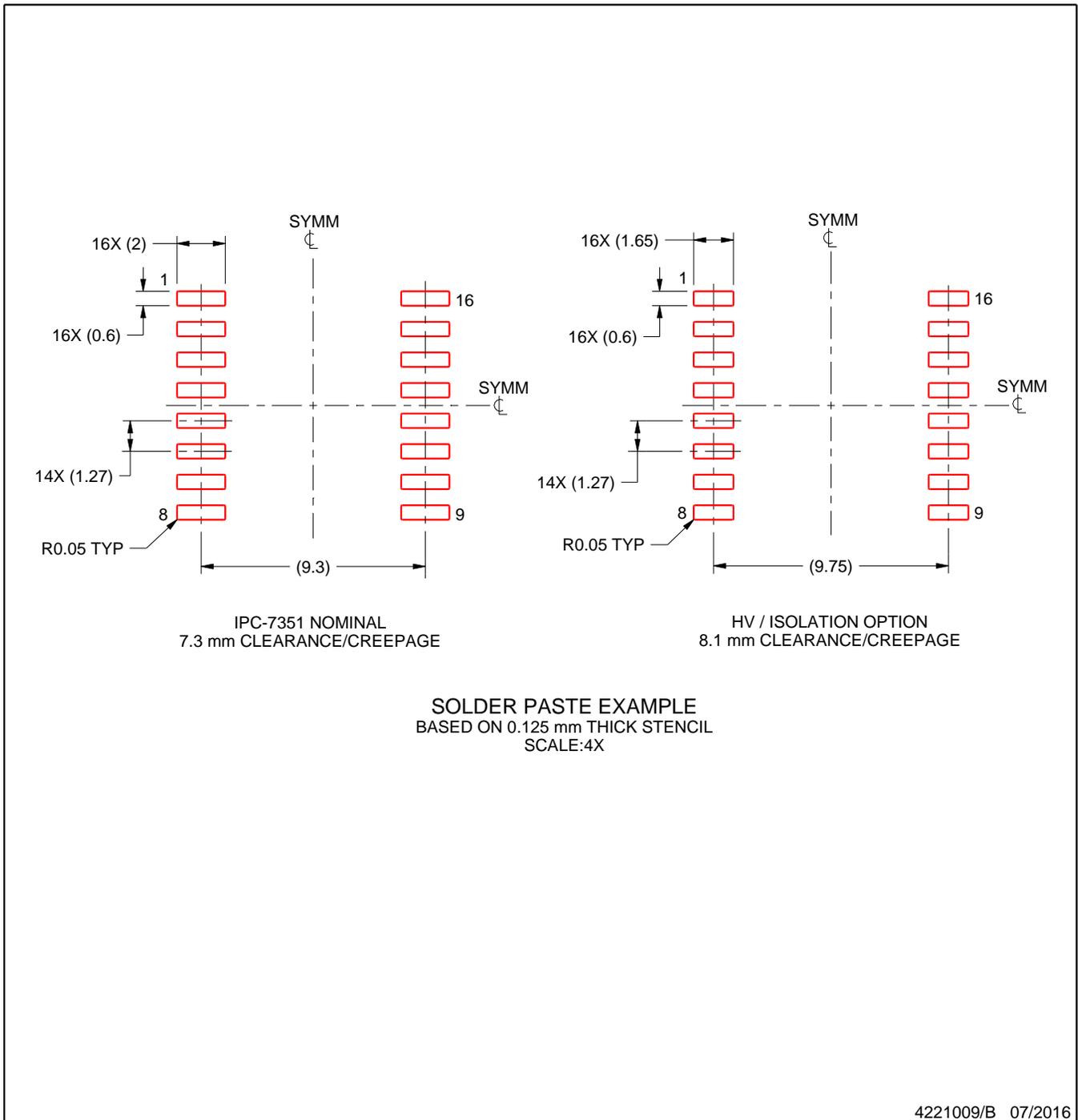
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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