S-35190A H Series

FOR AUTOMOTIVE 105°C OPERATION
3-WIRE REAL-TIME CLOCK

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The S-35190A H Series is a 105°C operation CMOS 3-wire real-time clock IC which operates with the very low current consumption in the wide range of operation voltage. The operation voltage is 1.3 V to 5.5 V so that the S-35190A H Series can be used for various power supplies from main supply to backup battery. Due to the 0.25 μA current consumption and wide range of power supply voltage at time keeping, the S-35190A H Series makes the battery life longer. In the system which operates with a backup battery, the included free registers can be used as the function for user's backup memory. Users always can take back the information in the registers which is stored before power-off the main power supply, after the voltage is restored.
The S-35190A H Series has the function to correct advance / delay of the clock data speed, in the wide range, which is caused by the crystal oscillation circuit's frequency deviation. Correcting according to the temperature change by combining this function and a temperature sensor, it is possible to make a high precise clock function which is not affected by the ambient temperature.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to SII Semiconductor Corporation is indispensable.**

■ Features

- Low current consumption: 0.25 μA typ. (V_{DD} = 3.0 V, Ta = +25°C)
- Wide range of operating voltage: 1.3 V to 5.5 V
- Built-in clock correction function
- Built-in free user register
- 3-wire (MICROWIRE) CPU interface
- Built-in alarm interrupter
- Built-in flag generator during detection of low power voltage or at power-on
- Auto calendar up to the year 2099, automatic leap year calculation function
- Built-in constant-voltage circuit
- Built-in 32.768 kHz crystal oscillator (built-in C_d, external C_g)
- Operating temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

***1.** Contact our sales office for details.

■ Packages

- 8-Pin SOP (JEDEC)
- 8-Pin TSSOP

■ Block Diagram

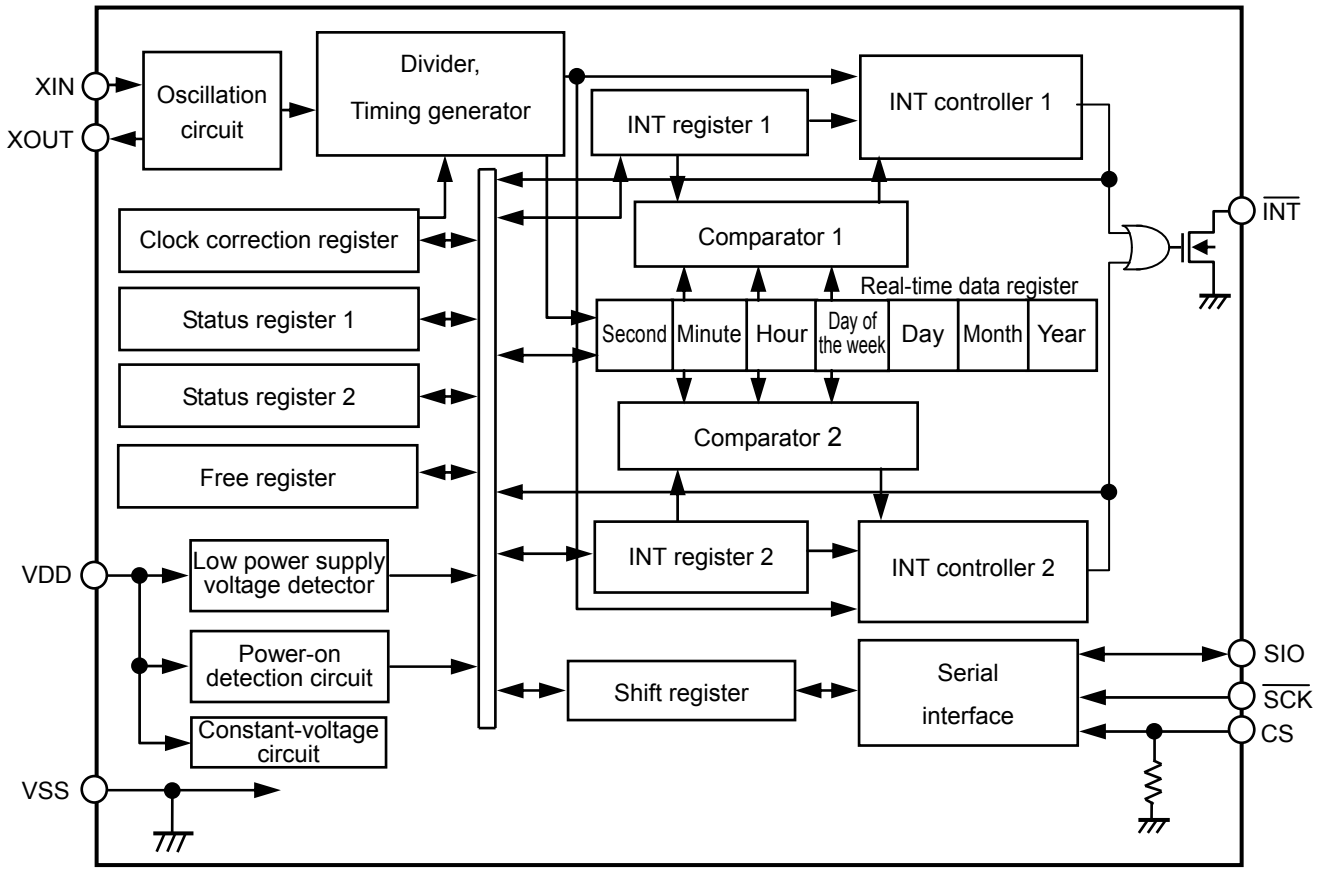


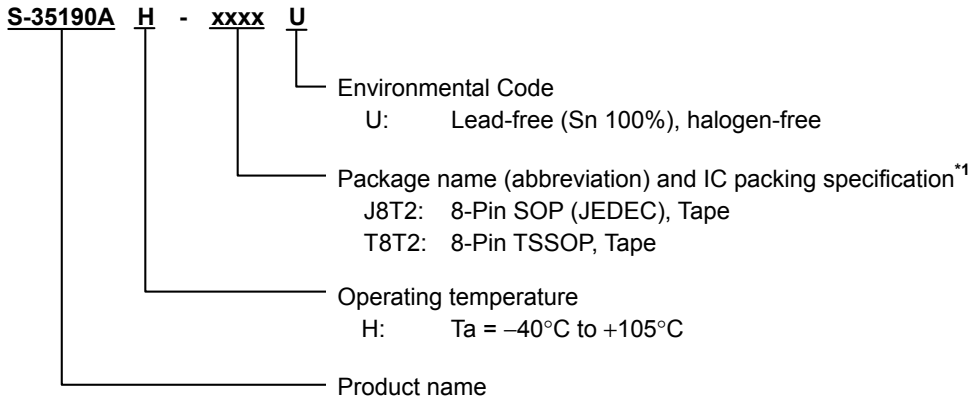
Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 2.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
8-PinSOP (JEDEC)	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-S1
8-Pin TSSOP	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1

■ Pin Configurations

1. 8-Pin SOP (JEDEC)

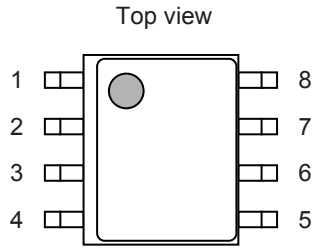


Figure 2 S-35190AH-J8T2U

2. 8-Pin TSSOP

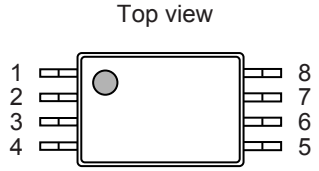


Figure 3 S-35190AH-T8T2U

Table 2 List of Pins

Pin No	Symbol	Description	I/O	Configuration
1	$\overline{INT}$	Output pin for interrupt signal	Output	Nch open-drain output (no protective diode at VDD)
2	XOUT	Connection pin for crystal oscillator	–	–
3	XIN			
4	VSS	GND pin	–	–
5	CS	Input pin for chip select	Input	CMOS input (built-in pull-down resistor. no protective diode at VDD)
6	$\overline{SCK}$	Input pin for serial clock	Input	CMOS input (no protective diode at VDD)
7	SIO	I/O pin for serial data	Bi-directional	Nch open-drain output (no protective diode at VDD) CMOS input
8	VDD	Pin for positive power supply	–	–

■ Pin Functions

1. CS (input for chip select) pin

This pin is to input chip select, has a pull-down resistor. Communication is available when this pin is in "H". If not using communication, set this pin "L" or open.

2. $\overline{\text{SCK}}$ (input for serial clock) pin

This pin is to input a clock pulse for serial interface. When the CS pin is in "H", the SIO pin inputs / outputs data by synchronizing with the clock pulse. When the CS pin is in "L" or open, the $\overline{\text{SCK}}$ pin does not accept inputting a clock pulse.

3. SIO (I/O for serial data) pin

This is a data input / output pin of serial interface. When the CS pin is in "H", the SIO pin inputs / outputs data by synchronizing with a clock pulse from the $\overline{\text{SCK}}$ pin. The status is in "High-Z" when the CS pin is in "L" or open, so that the S-35190A H Series does not transmit data. Setting the CS pin to "H" level from "L" or open, this SIO pin goes in the input status so that it receives the command data. This pin has CMOS input and Nch open drain output.

4. XIN, XOUT (crystal oscillator connect) pin

Connect a crystal oscillator between XIN and XOUT.

5. $\overline{\text{INT}}$ (output for interrupt signal) pin

This pin outputs a signal of interrupt, or a clock pulse. By using the status register 2, users can select either of; alarm 1 interrupt, alarm 2 interrupt, output of user-set frequency, minute-periodical interrupt 1, minute-periodical interrupt 2, or 32.768 kHz output. This pin has Nch open drain output.

6. VDD (positive power supply) pin

Connect this VDD pin with a positive power supply. Regarding the values of voltage to be applied, refer to "**■ Recommended Operation Conditions**".

7. VSS pin

Connect the VSS pin to GND.

■ Equivalent Circuits of Pins

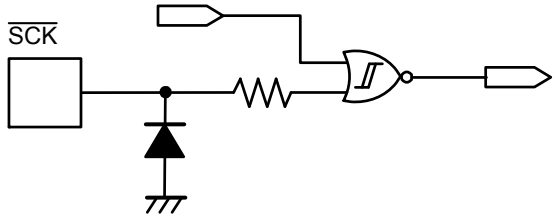


Figure 4 $\overline{\text{SCK}}$ Pin

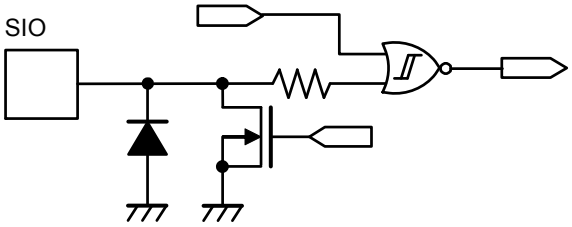


Figure 5 SIO Pin

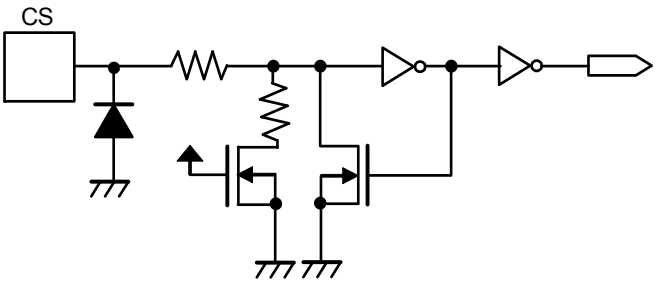


Figure 6 CS Pin

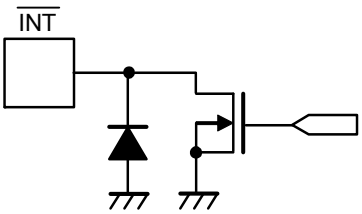


Figure 7 $\overline{\text{INT}}$ Pin

■ Absolute Maximum Ratings

Table 3

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	–	V_{SS} – 0.3 to V_{SS} + 6.5	V
Input voltage	V_{IN}	CS, $\overline{SCK}$, SIO	V_{SS} – 0.3 to V_{SS} + 6.5	V
Output voltage	V_{OUT}	SIO, $\overline{INT}$	V_{SS} – 0.3 to V_{SS} + 6.5	V
Operating ambient temperature*1	T_{opr}	–	–40 to +105	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

***1.** Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operation Conditions

Table 4

(V_{SS} = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage*1	V_{DD}	Ta = –40°C to +105°C	1.3	3.0	5.5	V
Time keeping power supply voltage*2	V_{DDT}	Ta = –40°C to +105°C	V_{DET} – 0.05	–	5.5	V
Crystal oscillator C_L value	C_L	–	–	6	7	pF

***1.** The power supply voltage that allows communication under the conditions shown in **Table 9** of "**■ AC Electrical Characteristics**".

***2.** The power supply voltage that allows time keeping. For the relationship with V_{DET} (low power supply voltage detection voltage), refer to "**■ Characteristics (Typical Data)**".

■ Oscillation Characteristics

Table 5

(Ta = +25°C, V_{DD} = 3.0 V, V_{SS} = 0 V, DMX-26S crystal oscillator (C_L = 6 pF, 32.768 kHz) manufactured by Daishinku corp.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	Within 10 seconds	1.1	–	5.5	V
Oscillation start time	t_{STA}	–	–	–	1	s
IC-to-IC frequency deviation*1	δIC	–	–10	–	+10	ppm
Frequency voltage deviation	δV	V_{DD} = 1.3 V to 5.5 V	–3	–	+3	ppm/V
External capacitance	C_g	Applied to XIN pin	–	–	9.1	pF
Internal oscillation capacitance	C_d	Applied to XOUT pin	–	8	–	pF

***1.** Reference value

■ DC Electrical Characteristics

Table 6 DC Characteristics (V_{DD} = 3.0 V)

(Ta = −40°C to +105°C, V_{SS} = 0 V, DMX-26S crystal oscillator (C_L = 6 pF, 32.768 kHz, C_g = 9.1 pF) manufactured by by Daishinku corp.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	Out of communication	–	0.25	1.2	µA
Current consumption 2	I_{DD2}	–	During communication ($\overline{SCK}$ = 100 kHz)	–	3.3	8	µA
Input current leakage 1	I_{IZH}	$\overline{SCK}$, SIO	$V_{IN} = V_{DD}$	−0.5	–	0.5	µA
Input current leakage 2	I_{IZL}	$\overline{SCK}$, SIO	$V_{IN} = V_{SS}$	−0.5	–	0.5	µA
Input current 1	I_{IH1}	CS	$V_{IN} = V_{DD}$	2	6	16	µA
Input current 2	I_{IH2}	CS	V_{IN} = 0.4 V	40	100	300	µA
Input current 3	I_{IH3}	CS	V_{IN} = 1.0 V	–	215	–	µA
Output current leakage 1	I_{OZH}	SIO, $\overline{INT}$	$V_{OUT} = V_{DD}$	−0.5	–	0.5	µA
Output current leakage 2	I_{OZL}	SIO, $\overline{INT}$	$V_{OUT} = V_{SS}$	−0.5	–	0.5	µA
Input voltage 1	V_{IH}	CS, $\overline{SCK}$, SIO	–	0.8 × V_{DD}	–	V_{SS} + 5.5	V
Input voltage 2	V_{IL}	CS, $\overline{SCK}$, SIO	–	V_{SS} − 0.3	–	0.2 × V_{DD}	V
Output current 1	I_{OL1}	$\overline{INT}$	V_{OUT} = 0.4 V	3	5	–	mA
Output current 2	I_{OL2}	SIO	V_{OUT} = 0.4 V	5	10	–	mA
Power supply voltage detection voltage	V_{DET}	–	–	0.60	1	1.35	V

Table 7 DC Characteristics (V_{DD} = 5.0 V)

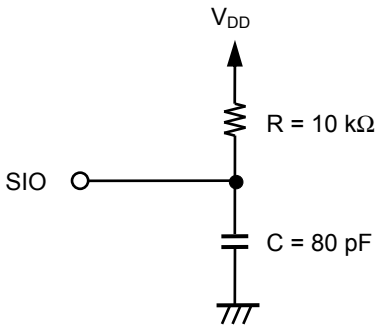
(Ta = −40°C to +105°C, V_{SS} = 0 V, DMX-26S crystal oscillator (C_L = 6 pF, 32.768 kHz, C_g = 9.1 pF) manufactured by by Daishinku corp.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I_{DD1}	–	Out of communication	–	0.3	1.4	µA
Current consumption 2	I_{DD2}	–	During communication ($\overline{SCK}$ = 100 kHz)	–	6	14	µA
Input current leakage 1	I_{IZH}	$\overline{SCK}$, SIO	$V_{IN} = V_{DD}$	−0.5	–	0.5	µA
Input current leakage 2	I_{IZL}	$\overline{SCK}$, SIO	$V_{IN} = V_{SS}$	−0.5	–	0.5	µA
Input current 1	I_{IH1}	CS	$V_{IN} = V_{DD}$	8	16	50	µA
Input current 2	I_{IH2}	CS	V_{IN} = 0.4 V	40	150	350	µA
Input current 3	I_{IH3}	CS	V_{IN} = 2.0 V	–	610	–	µA
Output current leakage 1	I_{OZH}	SIO, $\overline{INT}$	$V_{OUT} = V_{DD}$	−0.5	–	0.5	µA
Output current leakage 2	I_{OZL}	SIO, $\overline{INT}$	$V_{OUT} = V_{SS}$	−0.5	–	0.5	µA
Input voltage 1	V_{IH}	CS, $\overline{SCK}$, SIO	–	0.8 × V_{DD}	–	V_{SS} + 5.5	V
Input voltage 2	V_{IL}	CS, $\overline{SCK}$, SIO	–	V_{SS} − 0.3	–	0.2 × V_{DD}	V
Output current 1	I_{OL1}	$\overline{INT}$	V_{OUT} = 0.4 V	5	8	–	mA
Output current 2	I_{OL2}	SIO	V_{OUT} = 0.4 V	6	13	–	mA
Power supply voltage detection voltage	V_{DET}	–	–	0.60	1	1.35	V

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$V_{IH} = 0.8 \times V_{DD}$, $V_{IL} = 0.2 \times V_{DD}$
Input pulse rise / fall time	20 ns
Output determination voltage	$V_{OH} = 0.8 \times V_{DD}$, $V_{OL} = 0.2 \times V_{DD}$
Output load	80 pF + pull-up resistor 10 kΩ



Remark The power supplies of the IC and load have the same electrical potential.

Figure 8 Output Load Circuit

Table 9 AC Electrical Characteristics

(Ta = −40°C to +105°C)

Item	Symbol	V_{DD}*2 ≥ 1.3 V			V_{DD}*2 ≥ 3.0 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse width	t_{SCK}	5	–	250000	1	–	250000	µs
Setup time before CS rise	t_{DS}	1	–	–	0.2	–	–	µs
Hold time after CS rise	t_{CSH}	1	–	–	0.2	–	–	µs
Input data setup time	t_{ISU}	1	–	–	0.2	–	–	µs
Input data hold time	t_{IHO}	1	–	–	0.2	–	–	µs
Output data definition time*1	t_{ACC}	–	–	3.5	–	–	1	µs
Setup time before CS fall	t_{CSS}	1	–	–	0.2	–	–	µs
Hold time after CS fall	t_{DH}	1	–	–	0.2	–	–	µs
Input rise / fall time	t_R, t_F	–	–	0.1	–	–	0.05	µs

***1.** Since the output format of the SIO pin is Nch open-drain output, output data definition time is determined by the values of the load resistance (R_L) and load capacity (C_L) outside the IC. Therefore, use this value only as a reference value.

***2.** Regarding the power supply voltage, refer to "**■ Recommended Operation Conditions**".

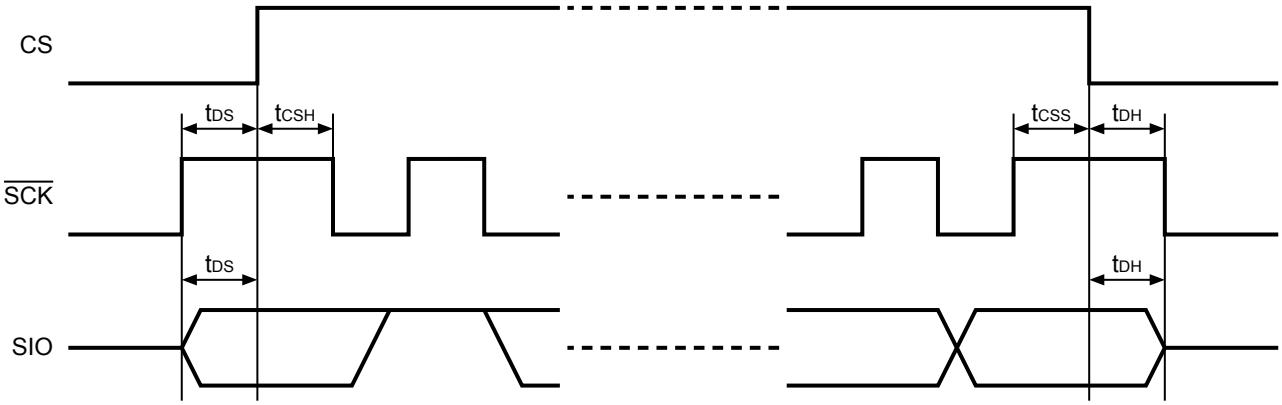


Figure 9 Timing Diagram 1 during 3-wire Communication

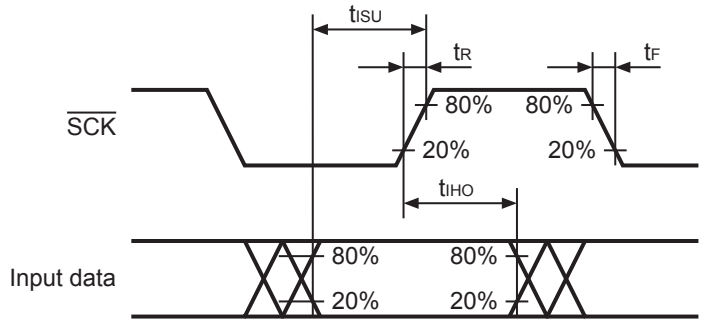


Figure 10 Timing Diagram 2 during 3-wire Communication

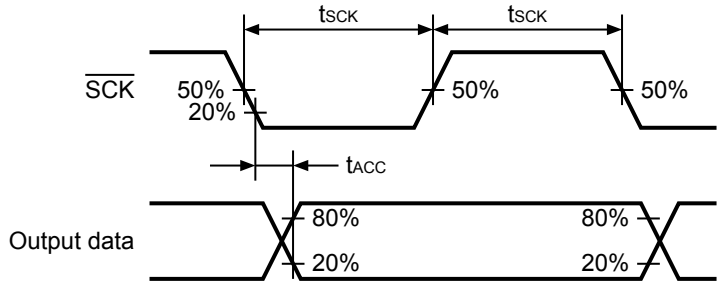


Figure 11 Timing Diagram 3 during 3-wire Communication

■ Configuration of Data Communication

1. Data communication

After setting the CS pin "H", transmit the 4-bit fixed code "0110", after that, transmit a 3-bit command and 1-bit read / write command. Next, data is output or input from B7. Regarding details, refer to "■ **Serial Interface**".

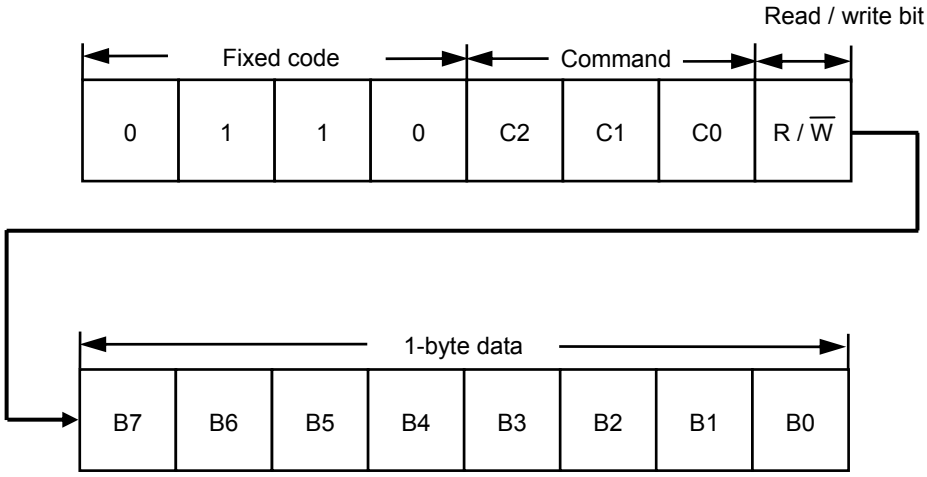


Figure 12 Data Communication

2. Configuration of command

8 types of command are available for the S-35190A H Series. The S-35190A H Series reads / writes the various registers by inputting these fixed codes and commands. The S-35190A H Series does not perform any operation with any codes and commands other than those below. However, in case that the fixed codes or the commands are failed to be recognized in the 1st byte but are successfully recognized in the 2nd and higher bytes, the commands are executed.

Table 10 List of Commands

Fixed Code	Command				Data							
	C2	C1	C0	Description	B7	B6	B5	B4	B3	B2	B1	B0
0110	0	0	0	Status register 1 access	RESET*1	$\overline{12}$ / 24	SC0*2	SC1*2	INT1*3	INT2*3	BLD*4	POC*4
	0	0	1	Status register 2 access	INT1FE	INT1ME	INT1AE	32kE	SC2*2	SC3*2	INT2AE	TEST*5
	0	1	0	Real-time data 1 access (year data to)	Y1 M1 D1 W1 H1 m1 s1	Y2 M2 D2 W2 H2 m2 s2	Y4 M4 D4 W4 H4 m4 s4	Y8 M8 D8 –*6 H8 m8 s8	Y10 M10 D10 –*6 H10 m10 s10	Y20 –*6 D20 –*6 H20 m20 s20	Y40 –*6 –*6 –*6 $\overline{AM}$ / PM m40 s40	Y80 –*6 –*6 –*6 –*6 –*6 –*6
	0	1	1	Real-time data 2 access (hour data to)	H1 m1 s1	H2 m2 s2	H4 m4 s4	H8 m8 s8	H10 m10 s10	H20 m20 s20	$\overline{AM}$ / PM m40 s40	–*6 –*6 –*6
	1	0	0	INT register 1 access (alarm time 1: week / hour / minute) (INT1AE = 1, INT1ME = 0, INT1FE = 0)	W1 H1 m1	W2 H2 m2	W4 H4 m4	–*6 H8 m8	–*6 H10 m10	–*6 H20 m20	–*6 $\overline{AM}$ / PM m40	A1WE A1HE A1mE
				INT register 1 access (output of user-set frequency) (INT1ME = 0, INT1FE = 1)	1 Hz	2 Hz	4 Hz	8 Hz	16 Hz	SC4 *2	SC5 *2	SC6 *2
	1	0	1	INT register 2 access (alarm time 2: week / hour / minute) (INT2AE = 1)	W1 H1 m1	W2 H2 m2	W4 H4 m4	–*6 H8 m8	–*6 H10 m10	–*6 H20 m20	–*6 $\overline{AM}$ / PM m40	A2WE A2HE A2mE
	1	1	0	Clock correction register access	V0	V1	V2	V3	V4	V5	V6	V7
	1	1	1	Free register access	F0	F1	F2	F3	F4	F5	F6	F7

***1.** Write-only flag. The S-35190A H Series initializes by writing "1" in this register.

***2.** Scratch bit. This is a register which is available for read / write operations and can be used by users freely.

***3.** Read-only flag. Valid only when using the alarm function. When the alarm time matches, this flag is set to "1", and it is cleared to "0" when reading.

***4.** Read-only flag. "POC" is set to "1" when power is applied. It is cleared to "0" when reading. Regarding "BLD", refer to "■ **Low Power Supply Voltage Detection Circuit**".

***5.** Test bit for SII Semiconductor Corporation. Be sure to set to "0" in use.

***6.** No effect when writing. It is "0" when reading.

■ Configuration of Registers

1. Real-time data register

The real-time data register is a 7-byte register that stores the data of year, month, day, day of the week, hour, minute, and second in the BCD code. To write / read real-time data 1 access, transmit / receive the data of year in B7, month, day, day of the week, hour, minute, second in B0, in 7-byte. When you skip the procedure to access the data of year, month, day, day of the week, read / write real-time data 2 accesses. In this case, transmit / receive the data of hour in B7, minute, second in B0, in 3-byte.
The S-35190A H Series transfers a set of data of time to the real-time data register when it recognizes a reading instruction. Therefore, the S-35190A H Series keeps precise time even if time-carry occurs during the reading operation of the real-time data register.

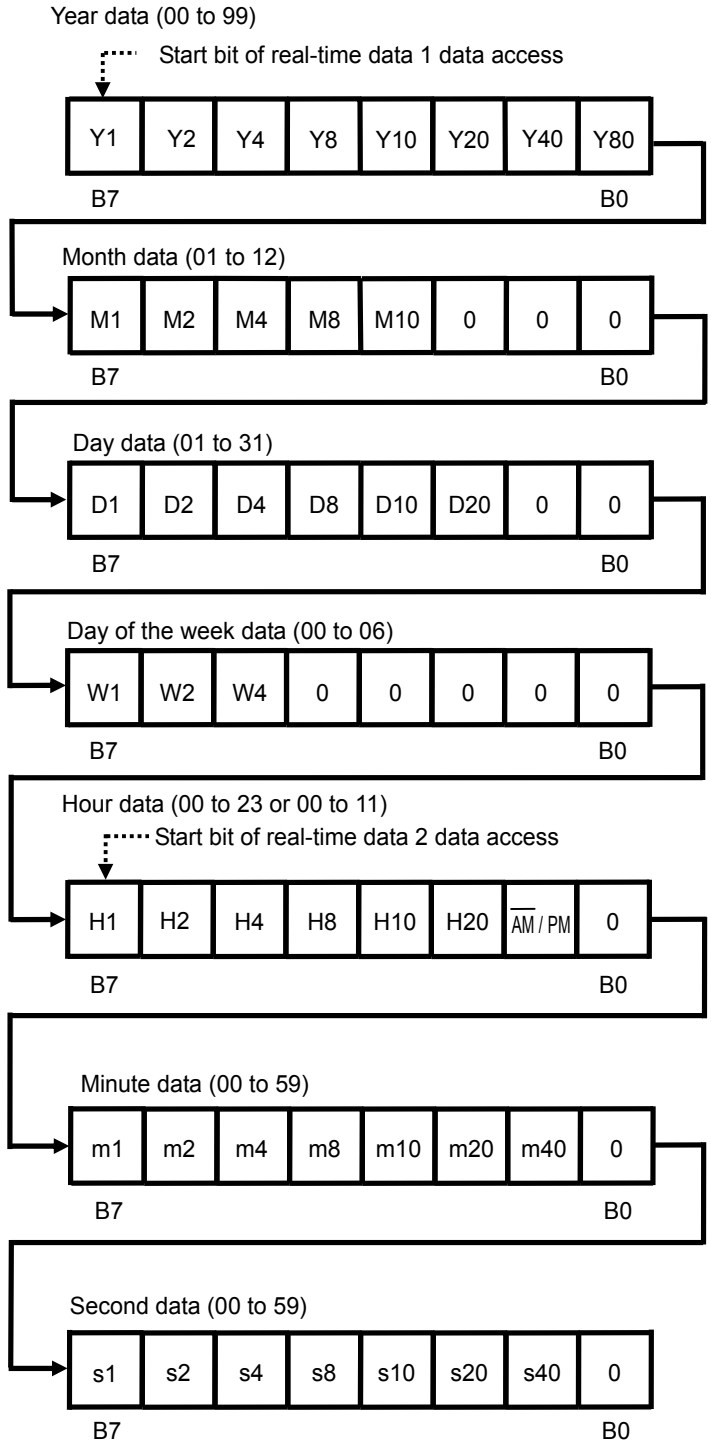


Figure 13 Real-time Data Register

Year data (00 to 99): Y1, Y2, Y4, Y8, Y10, Y20, Y40, Y80

Sets the lower two digits of the Western calendar year (00 to 99) and links together with the auto calendar function until 2099.
Example: 2053 (Y1, Y2, Y4, Y8, Y10, Y20, Y40, Y80) = (1, 1, 0, 0, 1, 0, 1, 0)

Month data (01 to 12): M1, M2, M4, M8, M10

Example: December (M1, M2, M4, M8, M10, 0, 0, 0) = (0, 1, 0, 0, 1, 0 ,0 ,0)

Day data (01 to 31): D1, D2, D4, D8, D10, D20

The count value is automatically changed by the auto calendar function.
1 to 31: Jan., Mar., May, July, Aug., Oct., Dec., 1 to 30: April, June, Sep., Nov.
1 to 29: Feb. (leap year), 1 to 28: Feb. (non-leap year)
Example: 29 (D1, D2, D4, D8, D10, D20, 0, 0) = (1, 0, 0, 1, 0, 1, 0, 0)

Day of the week data (00 to 06): W1, W2, W4

A septenary up counter. Day of the week is counted in the order of 00, 01, 02, …, 06, and 00. Set up day of the week and the count value.

Hour data (00 to 23 or 00 to 11): H1, H2, H4, H8, H10, H20, $\overline{\text{AM}}$ / PM

In 12-hour mode, write 0; AM, 1; PM in the $\overline{\text{AM}}$ / PM bit. In 24-hour mode, users can write either 0 or 1. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.

Example (12-hour mode): 11 p.m. (H1, H2, H4, H8, H10, H20, $\overline{\text{AM}}$ / PM, 0) = (1, 0, 0, 0, 1, 0, 1, 0)
Example (24-hour mode): 22 (H1, H2, H4, H8, H10, H20, $\overline{\text{AM}}$ / PM, 0) = (0, 1, 0, 0, 0, 1, 1, 0)

Minute data (00 to 59): m1, m2, m4, m8, m10, m20, m40

Example: 32 minutes (m1, m2, m4, m8, m10, m20, m40, 0) = (0, 1, 0, 0, 1, 1, 0, 0)
Example: 55 minutes (m1, m2, m4, m8, m10, m20, m40, 0) = (1, 0, 1, 0, 1, 0, 1, 0)

Second data (00 to 59): s1, s2, s4, s8, s10, s20, s40

Example: 19 seconds (s1, s2, s4, s8, s10, s20, s40, 0) = (1, 0, 0, 1, 1, 0, 0, 0)

2. Status register 1

Status register 1 is a 1-byte register that is used to display and set various modes. The bit configuration is shown below.

B7	B6	B5	B4	B3	B2	B1	B0
RESET	$\overline{12}$ / 24	SC0	SC1	INT1	INT2	BLD	POC
W	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R	R	R	R

R: Read
W: $\overline{\ }$ Write
R / $\overline{W}$: Read / write

Figure 14 Status Register 1

B0: POC

This flag is used to confirm whether the power is on. The power-on detection circuit operates at power-on and B0 is set to "1". This flag is read-only. Once it is read, it is automatically set to "0". When this flag is "1", be sure to initialize. Regarding the operation after power-on, refer to "■ **Power-on Detection Circuit and Register Status**".

B1: BLD

This flag is set to "1" when the power supply voltage decreases to the level of detection voltage (V_{DET}) or less. Users can detect a drop in the power supply voltage. Once this flag is set to "1", it is not set to "0" again even if the power supply increases to the level of detection voltage (V_{DET}) or more. This flag is read-only. When this flag is "1", be sure to initialize. Regarding the operation of the power supply voltage detection circuit, refer to "■ **Low Power Supply Voltage Detection Circuit**".

B2: INT2, B3: INT1

This flag indicates the time set by alarm and when the time has reached it. This flag is set to "1" when the time that users set by using the alarm interrupt function has come. The INT1 flag at alarm 1 interrupt mode and the INT2 flag at alarm 2 interrupt mode are set to "1". Set "0" in INT1AE (B5 in the status register 2) or in INT2AE (B1 in the status register 2) after reading "1" in the INT1 flag or in the INT2 flag. This flag is read-only. Once this flag is read, it is set to "0" automatically.

B4: SC1, B5: SC0

These flags are SRAM type registers, they are 2 bits as a whole, can be freely set by users.

B6: $\overline{12}$ / 24

This flag is used to set 12-hour or 24-hour mode. Set the flag ahead of write operation of the real-time data register in case of 24-hour mode.

0: 12-hour mode
1: 24-hour mode

B7: RESET

The internal IC is initialized by setting this bit to "1". This bit is write-only. It is always "0" when reading. When applying the power supply voltage to the IC, be sure to write "1" to this bit to initialize the circuit. Regarding each status of data after initialization, refer to "■ **Register Status After Initialization**".

3. Status register 2

Status register 2 is a 1-byte register that is used to display and set various modes. The bit configuration is shown below.

B7	B6	B5	B4	B3	B2	B1	B0
INT1FE	INT1ME	INT1AE	32kE	SC2	SC3	INT2AE	TEST
R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$

R / $\overline{W}$: Read / write

Figure 15 Status Register 2

B0: TEST

This is a test flag for SII Semiconductor Corporation. Be sure to set this flag to "0" in use. If this flag is set to "1", be sure to initialize to set "0".

B1: INT2AE

This is an enable bit for alarm 2 interrupt. When this bit is "0", alarm 2 interrupt is disabled. When it is "1", it is enabled. To use alarm 2 interrupt, access the INT register 2 after enabling this flag.

Caution Note that alarm 2 interrupt is output from the $\overline{INT}$ pin regardless of the settings in flags B4 to B7.

B2: SC3, B3: SC2

These are 2-bit SRAM type registers that can be freely set by users.

B4: 32kE, B5: INT1AE, B6: INT1ME, B7: INT1FE

These bits are used to select the output mode for the $\overline{INT}$ pin. **Table 11** shows how to select the mode. To use alarm 1 interrupt, access the INT register 1 after setting the alarm 1 interrupt mode.

Table 11 Output Modes for $\overline{INT}$ Pin

32kE	INT1AE	INT1ME	INT1FE	$\overline{INT}$ Pin Output Mode
0	0	0	0	No interrupt
0	–*1	0	1	Output of user-set frequency
0	–*1	1	0	Per-minute edge interrupt
0	0	1	1	Minute-periodical interrupt 1 (50% duty)
0	1	0	0	Alarm 1 interrupt
0	1	1	1	Minute-periodical interrupt 2
1	–*1	–*1	–*1	32.768 kHz output

***1.** Don't care (both of 0 and 1 are acceptable).

4. INT register 1 and INT register 2

The INT register 1 is to set up the output of user-set frequency, or to set up alarm 1 interrupt. The INT register 2 is for setting alarm 2 interrupt. Users are able to switch the output mode by using the status register 2. If selecting to use the output mode for alarm interrupt by status register 2; this register works as the alarm-time data register. In the INT register 1, if selecting the output of user-set frequency by status register 2; this register works as the data register to set the frequency for clock output. From the $\overline{\text{INT}}$ pin, a clock pulse and alarm interrupt are output, according to the or-condition that these two registers have.

4. 1 Alarm interrupt

Users can set the alarm time (the data of day of the week, hour, minute) by using the INT register 1 and 2 which are 3-byte data registers. The configuration of register is as well as the data register of day of the week, hour, minute, in the real-time data register; is expressed by the BCD code. Do not set a nonexistent day. Users are necessary to set up the alarm-time data according to the 12 / 24 hour expression that they set by using the status register 1.

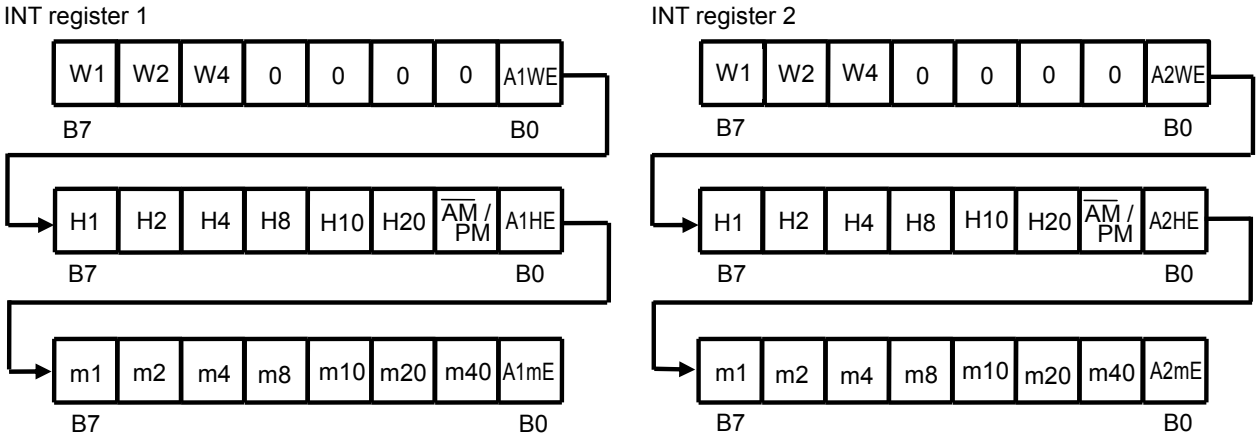


Figure 16 INT Register 1 and INT Register 2 (Alarm-Time Data)

The INT register 1 has A1WE, A1HE, A1mE at B0 in each byte. It is possible to make data valid; the data of day of the week, hour, minute which are in the corresponded byte; by setting these bits to "1". This is as well in A2WE, A2HE, A2mE in the INT register 2.

Setting example: alarm time "7:00 pm" in the INT register 1

(1) 12-hour mode (status register 1 B6 = 0)

set up 7:00 PM
Data written to INT register 1

	B7							B0
Day of the week	_*1	_*1	_*1	_*1	_*1	_*1	_*1	0
Hour	1	1	1	0	0	0	1	1
Minute	0	0	0	0	0	0	0	1

***1.** Don't care (both of 0 and 1 are acceptable).

(2) 24-hour mode (status register 1 B6 = 1)

set up 19:00 PM
Data written to INT register 1

	B7							B0
Day of the week	_*1	_*1	_*1	_*1	_*1	_*1	_*1	0
Hour	1	0	0	1	1	0	1*2	1
Minute	0	0	0	0	0	0	0	1

***1.** Don't care (both of 0 and 1 are acceptable).

***2**. Set up $\overline{\text{AM}}$ / PM flag along with the time setting.

4. 2 Output of user-set frequency

The INT register 1 is a 1-byte data register to set up the output frequency. Setting each bit B7 to B3 in the register to "1", the frequency which corresponds to the bit is output in the AND-form. SC4 to SC6 is 3-bit SRAM type registers that can be freely set by users.

B7	B6	B5	B4	B3	B2	B1	B0
1 Hz	2 Hz	4 Hz	8 Hz	16 Hz	SC4	SC5	SC6
R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$

R / $\overline{W}$: Read / write

Figure 17 INT Register 1 (Data Register for Output Frequency)

Example: B7 to B3 = 50h

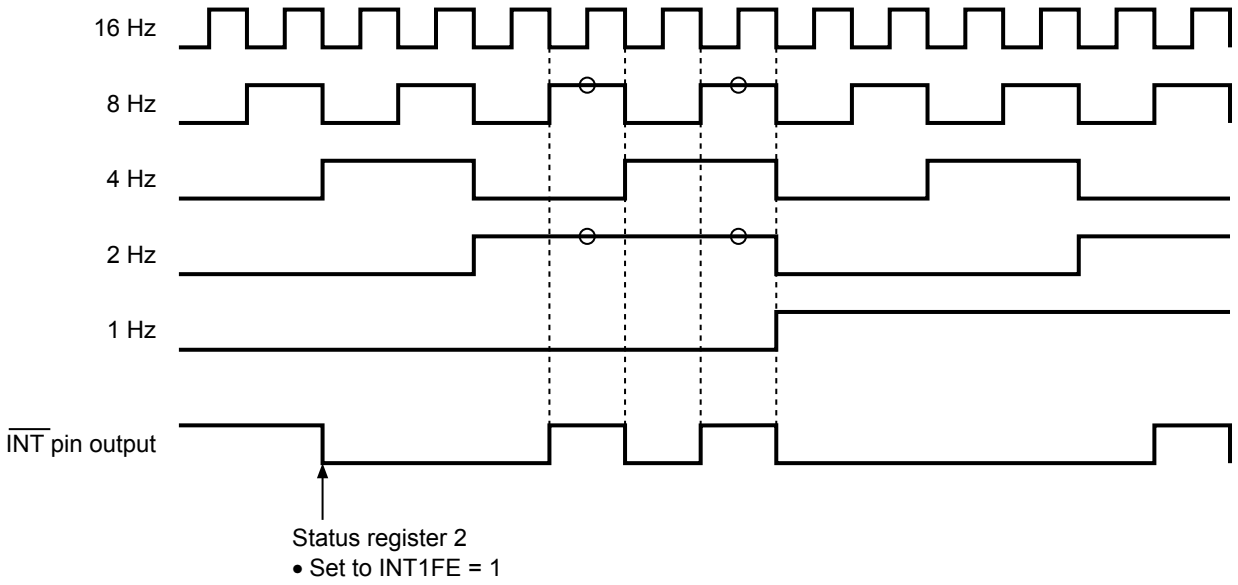


Figure 18 Example of Output from INT Register 1 (Data Register for Output Frequency)

1 Hz clock output is synchronized with second-counter of the S-35190A H Series

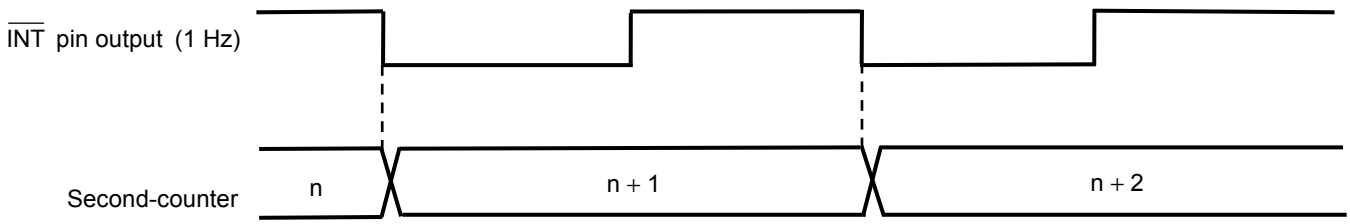


Figure 19 1 Hz Clock Output and Second-counter

5. Clock correction register

The clock correction register is a 1-byte register that is used to correct advance / delay of the clock. When not using this function, set this register to "00h". Regarding the register values, refer to "■ **Function of Clock Correction**".

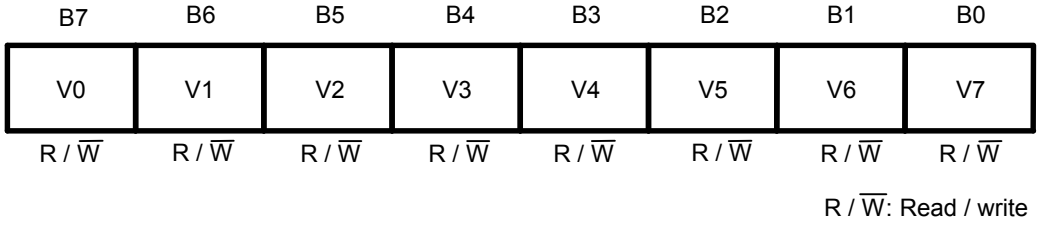


Figure 20 Clock Correction Register

6. Free register

The free register is a 1-byte SRAM type register that can be set freely by users.

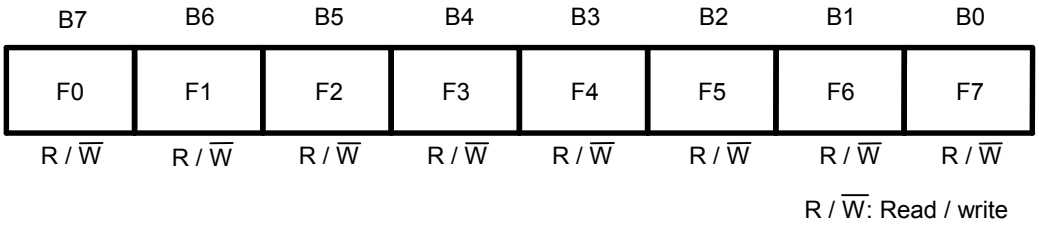


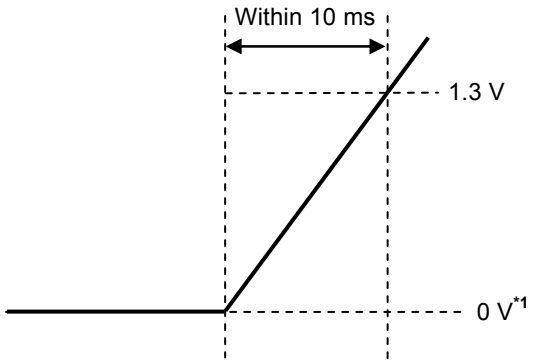
Figure 21 Free Register

■ Power-on Detection Circuit and Register Status

The power-on detection circuit operates by power-on the S-35190A H Series, as a result each register is cleared; each register is set as follows.

Real-time data register:	00 (Y), 01 (M), 01 (D), 0 (day of the week), 00 (H), 00 (M), 00 (S)
Status register 1:	"01h"
Status register 2:	"80h"
INT register 1:	"80h"
INT register 2:	"00h"
Clock correction register:	"00h"
Free register:	"00h"

"1" is set in the POC flag (B0 in the status register 1) to indicate that power has been applied. To correct the oscillation frequency, the status register 2 goes in the mode the output of user-set frequency, so that 1 Hz clock pulse is output from the $\overline{INT}$ pin. When "1" is set in the POC flag, be sure to initialize. The POC flag is set to "0" due to initialization so that the output of user-set frequency mode is cleared. (Refer to "**■ Register Status After Initialization**".)
For the regular operation of power-on detection circuit, as seen in **Figure 22**, the period to power-up the S-35190A H Series is that the voltage reaches 1.3 V within 10 ms after setting the IC's power supply voltage at 0 V. When the power-on detection circuit is not working normally is; the POC flag (B0 in the status register 1) is not in "1", or 1 Hz is not output from the $\overline{INT}$ pin. In this case, power-on the S-35190A H Series once again because the internal data may be in the indefinite status.
Moreover, regarding the processing right after power-on, refer to "**■ Flowchart of Initialization and Example of Real-time Data Set-up**".



***1.** 0 V indicates that there are no potential differences between the VDD pin and VSS pin of the S-35190A H Series.

Figure 22 How to Raise the Power Supply Voltage

■ Register Status After Initialization

The status of each register after initialization is as follows.

Real-time data register:	00 (Y), 01 (M), 01 (D), 0 (day of the week), 00 (H), 00 (M), 00 (S)
Status register 1:	"0 B6 B5 B4 0 0 0 0 b" (In B6, B5, B4, the data of B6, B5, B6 in the status register 1 at initialization is set. Refer to **Figure 23**.)
Status register 2:	"00h"
INT register 1:	"00h"
INT register 2:	"00h"
Clock correction register:	"00h"
Free register:	"00h"

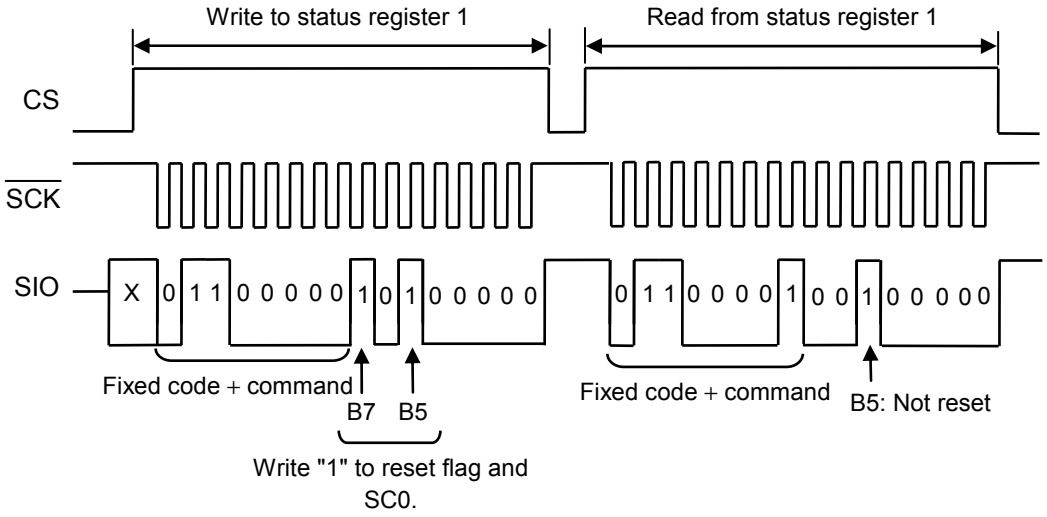


Figure 23 Status Register 1 Data at Initialization

■ Low Power Supply Voltage Detection Circuit

The S-35190A H Series has a low power supply voltage detection circuit, so that users can monitor drops in the power supply voltage by reading the BLD flag (B1 in the status register 1). There is a hysteresis width of approx. 0.15 V typ. between detection voltage and release voltage (refer to "■ **Characteristics (Typical Data)**"). The low power supply voltage detection circuit does the sampling operation only once in one sec for 15.6 ms.
If the power supply voltage decreases to the level of detection voltage (V_{DET}) or less, "1" is set to the BLD flag so that sampling operation stops. Once "1" is detected in the BLD flag, no sampling operation is performed even if the power supply voltage increases to the level of release voltage or more, and "1" is held in the BLD flag.
Furthermore, the S-35190A H Series does not initialize the internal circuit even if "1" is set to the BLD flag. If the BLD flag is "1" even after the power supply voltage is recovered, the internal circuit may be in the indefinite status. In this case, be sure to initialize the circuit. Without initializing, if the next BLD flag reading is done after sampling, the BLD flag gets reset to "0". In this case, be sure to initialize although the BLD flag is in "0" because the internal circuit may be in the indefinite status.

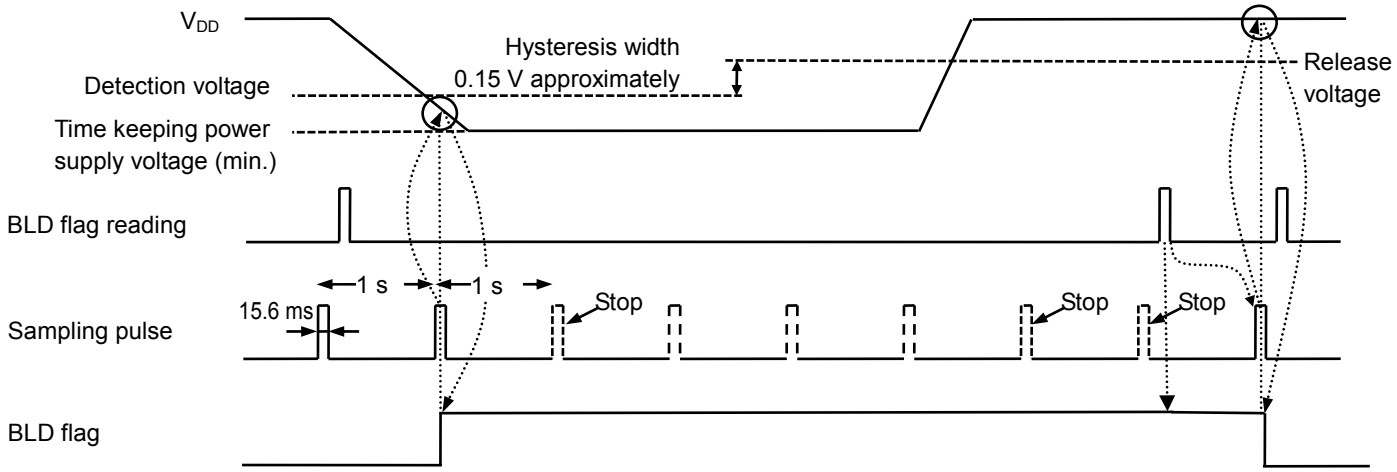


Figure 24 Timing of Low Power Supply Voltage Detection Circuit

■ Circuits Power-on and Low Power Supply Voltage Detection

Figure 25 shows the changes of the POC flag and BLD flag due to V_{DD} fluctuation.

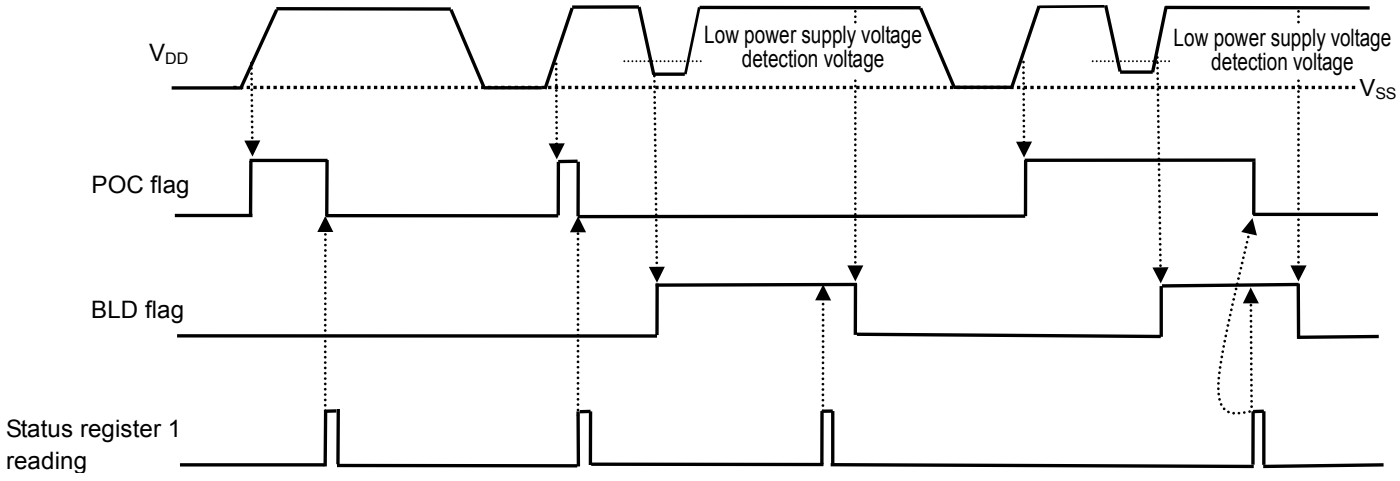


Figure 25 POC Flag and BLD Flag

■ Correction of Nonexistent Data and End-of-Month

When users write the real-time data, the S-35190A H Series checks it. In case that the data is invalid, the S-35190A H Series does the following procedures.

1. Processing of nonexistent data

Table 12 Processing of Nonexistent Data

Register		Normal Data	Nonexistent Data	Result
Year data		00 to 99	XA to XF, AX to FX	00
Month data		01 to 12	00, 13 to 19, XA to XF	01
Day data		01 to 31	00, 32 to 39, XA to XF	01
Day of the week data		0 to 6	7	0
Hour data*1	24-hour	0 to 23	24 to 29, 3X, XA to XF	00
	12-hour	0 to 11	12 to 20, XA to XF	00
Minute data		00 to 59	60 to 79, XA to XF	00
Second data*2		00 to 59	60 to 79, XA to XF	00

***1.** In 12-hour mode, write the $\overline{\text{AM}}$ / PM flag (B1 in hour data in the real-time data register).

In 24-hour mode, the $\overline{\text{AM}}$ / PM flag in the real-time data register is omitted. However in the flag of reading, users are able to read 0; 0 to 11, 1; 12 to 23.

***2.** Processing of nonexistent data, regarding second data, is done by a carry pulse which is generated in 1 second, after writing. At this point the carry pulse is sent to the minute-counter.

2. Correction of end-of-month

A nonexistent day, such as February 30 and April 31, is set to the first day of the next month.

■ $\overline{\text{INT}}$ Pin Output Mode

These are selectable for the $\overline{\text{INT}}$ pin output mode;
Alarm 1 interrupt, alarm 2 interrupt, the output of user-set frequency, per-minute edge interrupt output, minute-periodical interrupt output 1 and 2, 32.768 kHz output.
In alarm 1 interrupt / output of frequency; set data in the INT register 1. In alarm 2 interrupt, set data in the INT register 2. To swith the output mode, use the status register 2. Refer to "**3. Status register 2**" in "**■ Configuration of Registers**".
When switching the output mode, be careful of the output status of the pin. Especially, when using alarm interrupt / output of frequency, switch the output mode after setting "00h" in the INT register 1 or 2. Alarm 2 interrupt is dependent from other modes. Regardless of other settings of mode if alarm 2 interrupt was generated, be careful that "L" is output from the $\overline{\text{INT}}$ pin. In 32.768 kHz output / per-minute edge interrupt output / minute-periodical interrupt output, it is unnecessary to set data in the INT register 1 or 2 for users.
Refer to the followings regarding each operation of output modes.

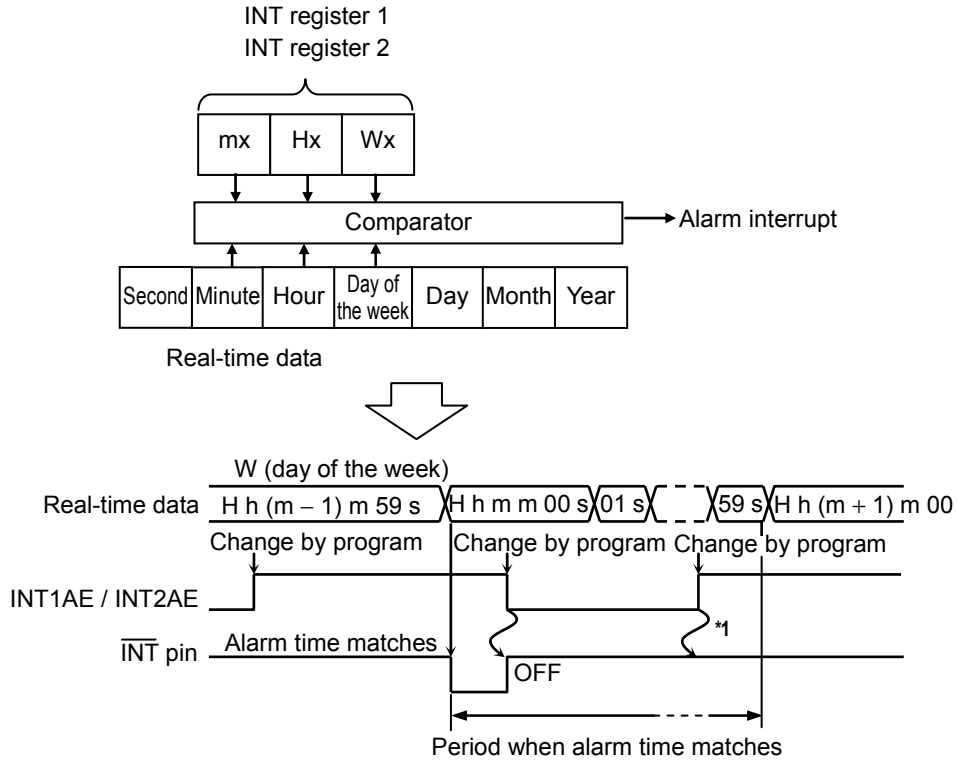
1. Alarm interrupt output

Alarm interrupt output is the function to output "L" from the $\overline{\text{INT}}$ pin, at the alarm time which is set by user has come. If setting the pin output to "H", turn off the alarm function by setting "0" in INT1AE / INT2AE in the status register 2.
To set the alarm time, set the data of day of the week, hour, minute in the INT register 1 or 2, set the data of year, month, day in the INT register 1 or 2. Refer to "**4. INT register 1 and INT register 2**" in "**■ Configuration of Register**".

1. 1 Alarm setting of "W (day of the week), H (hour), m (minute)"

Status register 2 setting
- Alarm 1 interrupt
  32kE = 0, INT1ME = INT1FE = 0
- Alarm 2 interrupt
  None

INT register x alarm enable flag
- AxHE = AxmE = AxWE = "1"



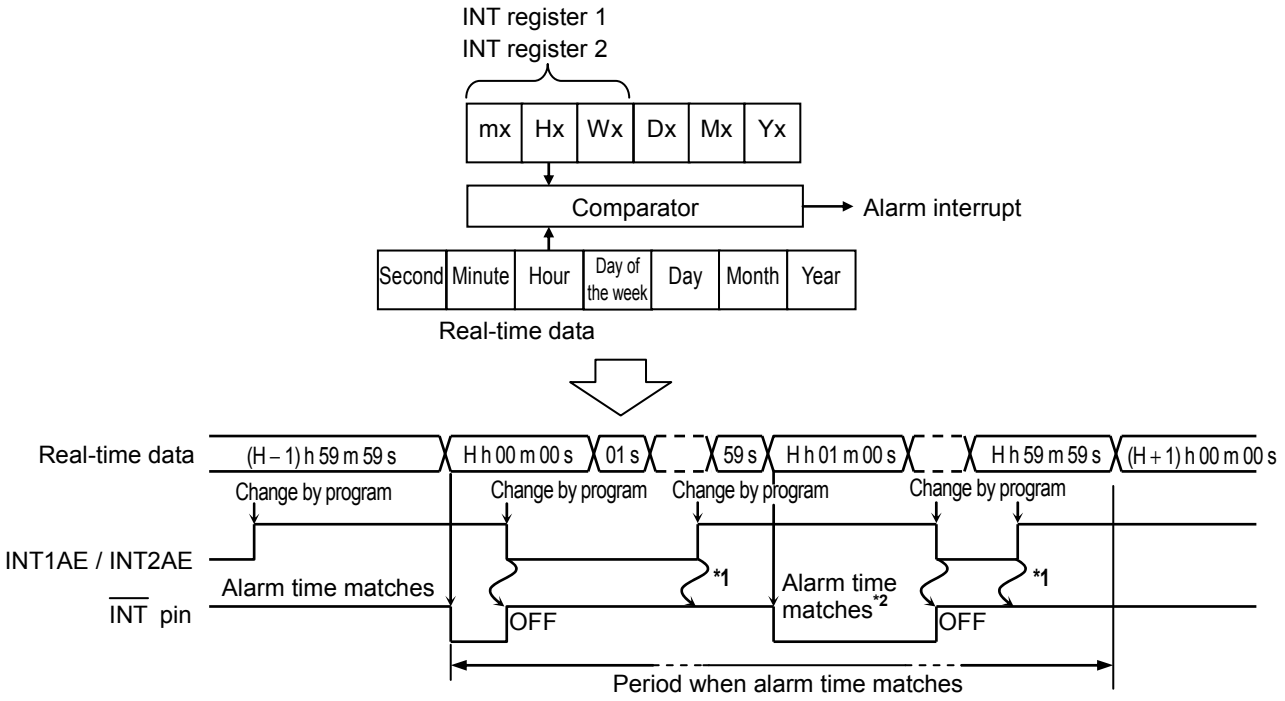
***1.** If users clear INT1AE / INT2AE once; "L" is not output from the $\overline{\text{INT}}$ pin by setting INT1AE / INT2AE enable again, within a period when the alarm time matches real-time data.

Figure 26 Alarm Interrupt Output Timing

1. 2 Alarm setting of "H (hour)"

Status register 2 setting
- Alarm 1 interrupt
  32kE = 0, INT1ME = INT1FE = 0
- Alarm 2 interrupt
  None

INT register x alarm enable flag
- AxWE = AxmE = "0", AxHE = "1"



***1.** If users clear INT1AE / INT2AE once; "L" is not output from the $\overline{\text{INT}}$ pin by setting INT1AE / INT2AE enable again, within a period when the alarm time matches real-time data.

***2.** If turning the alarm output on by changing the program, within the period when the alarm time matches real-time data, "L" is output again from the $\overline{\text{INT}}$ pin when the minute is counted up.

Figure 27 Alarm Interrupt Output Timing

2. Output of user-set frequency

The output of user-set frequency is the function to output the frequency which is selected by using data, from the INT pin, in the AND-form. Set up the data of frequency in the INT register 1.
Refer to "**4. INT register 1 and INT register 2**" in "**■ Configuration of Register**".

Status register 2 setting

32kE = 0, INT1AE = Don't care (0 or 1), INT1ME = 0

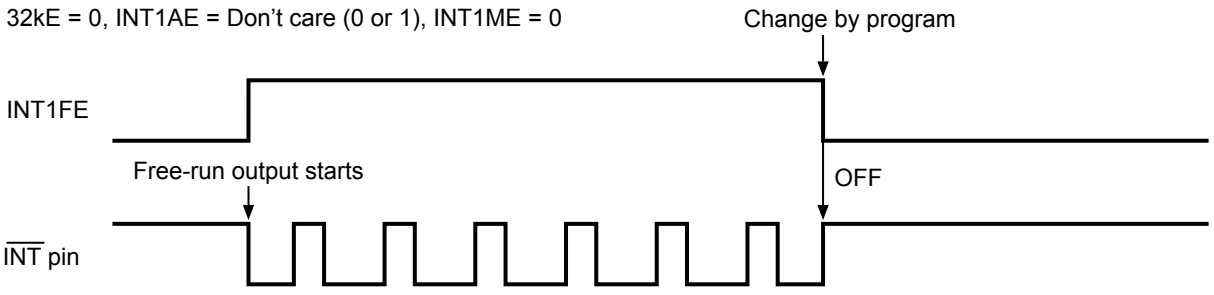


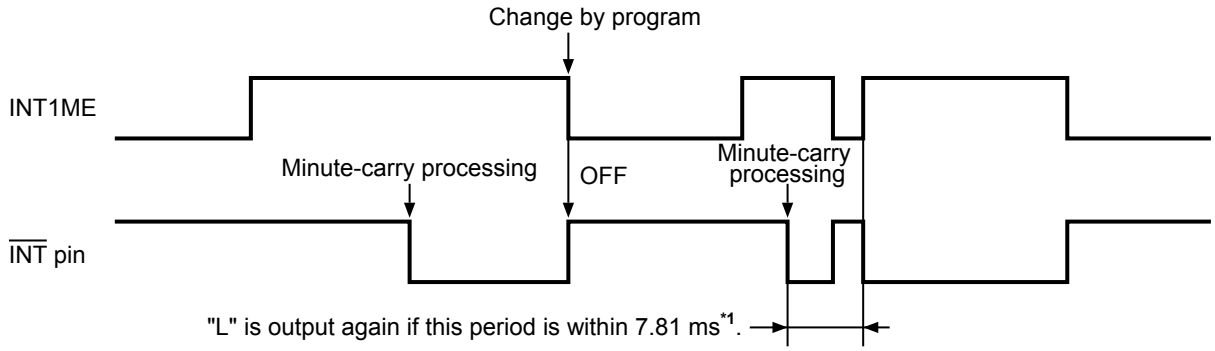
Figure 28 Output Timing of User-set Frequency

3. Per-minute edge interrupt output

Per-minute edge interrupt output is the function to output "L" from the $\overline{INT}$ pin, when the first minute-carry processing is done, after selecting the output mode. To set the pin output to "H", set "0" in INT1ME in the status register 2 to turn off the output mode of per-minute edge interrupt.

Status register 2 setting

- 32kE = 0, INT1AE = Don't care (0 or 1), INT1FE = 0



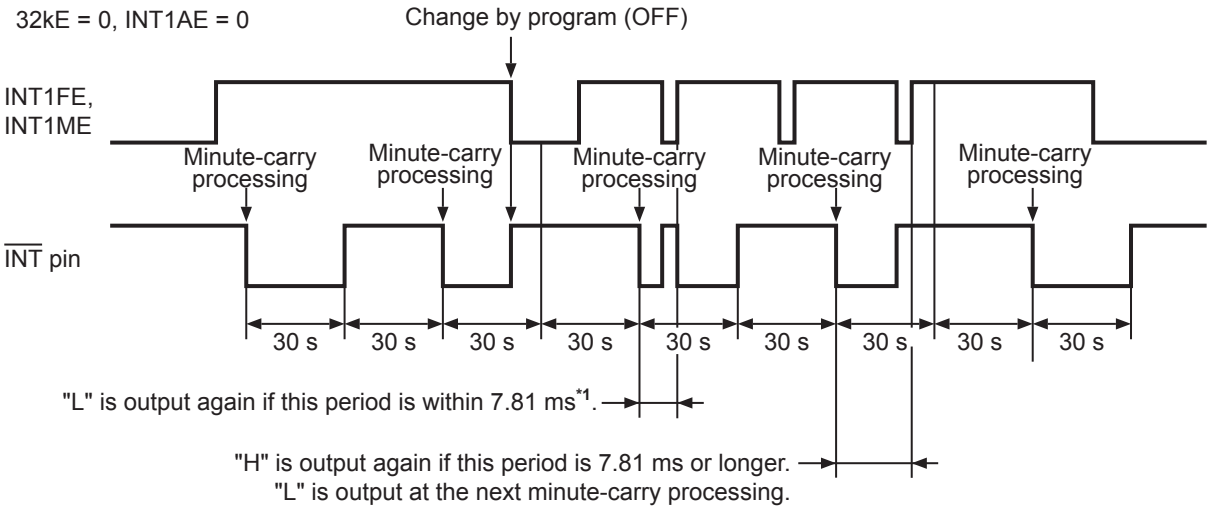
***1.** Pin output is set to "H" by disabling the output mode within 7.81 ms, because the signal of this procedure is maintained for 7.81 ms. Note that pin output is set to "L" by setting the output mode enable again.

Figure 29 Timing of Per-Minute Edge Interrupt Output

4. Minute-periodical interrupt output 1

The minute-periodical interrupt 1 is the function to output the one-minute clock pulse (Duty 50%) from the $\overline{INT}$ pin, when the first minute-carry processing is done, after selecting the output mode.

Status register 2 setting



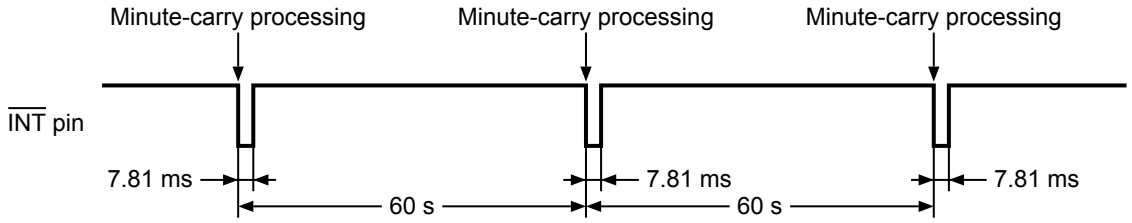
***1.** Setting the output mode disable makes the pin output "H", while the output from the $\overline{INT}$ pin is in "L". Note that pin output is set to "L" by setting the output mode enable again.

Figure 30 Timing of Minute-periodical Interrupt Output 1

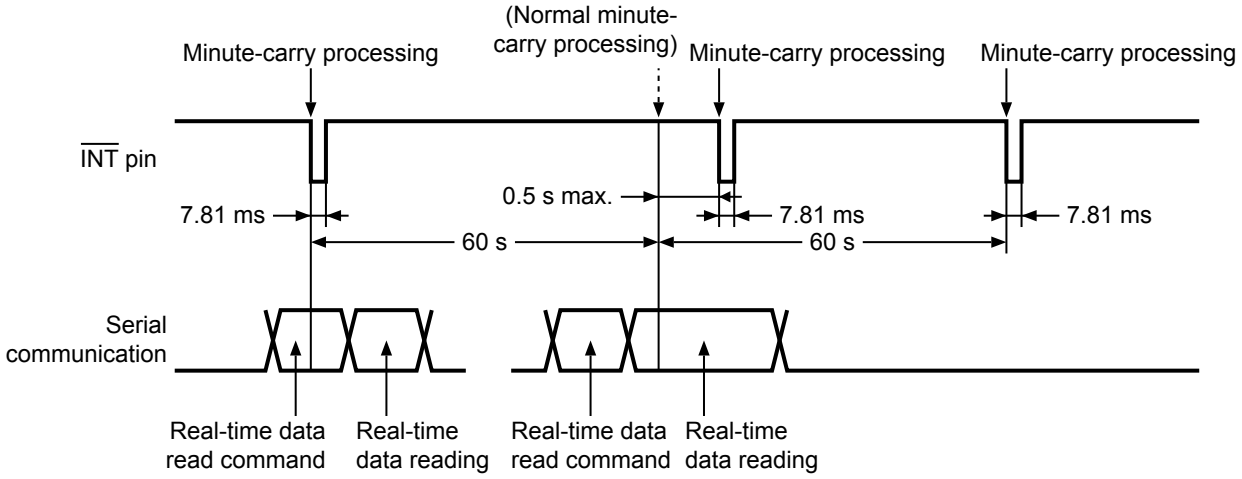
5. Minute-periodical interrupt output 2

The output of minute-periodical interrupt 2 is the function to output "L", for 7.81 ms, from the $\overline{\text{INT}}$ pin, synchronizing with the first minute-carry processing after selecting the output mode. However, during a reading operation in the real-time data register, the procedure delays at 0.5 seconds max. thus output "L" from the $\overline{\text{INT}}$ pin also delays at 0.5 seconds max. During a writing operation in the real-time data register, some delay is made in the output period due to write timing and the second-data of writing.

(1) During normal operation



(2) During reading operation in the real-time data register



(3) During writing operation in the real-time data register

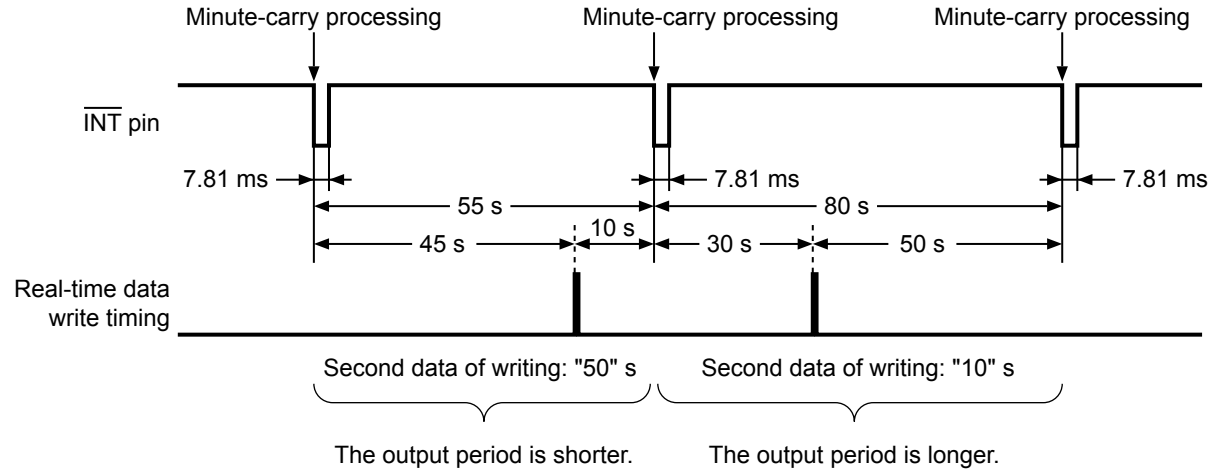


Figure 31 Timing of Minute-periodical Interrupt Output 2

6. Operation of power-on detection circuit

When power is applied to the S-35190A H Series, the power-on detection operates to set "1" in the POC flag (B0 in the status register 1). A 1 Hz clock pulse is output from the $\overline{\text{INT}}$ pin.

Status register 2 setting

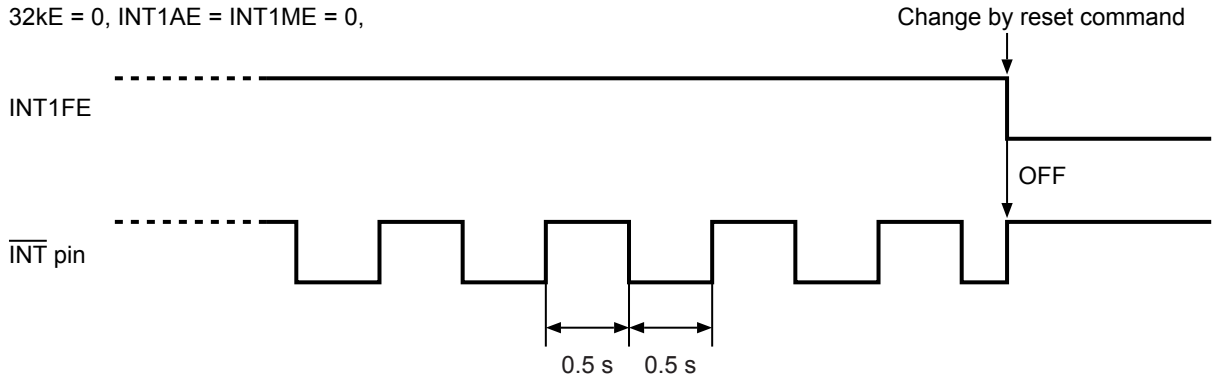


Figure 32 Output Timing of $\overline{\text{INT}}$ Pin during Operation of Power-on Detection Circuit

■ Function of Clock Correction

The function of clock correction is to correct advance / delay of the clock due to the deviation of oscillation frequency, in order to make a high precise clock. For correction, the S-35190A H Series adjusts the clock pulse by using a certain part of the dividing circuit, not adjusting the frequency of the crystal oscillator. Correction is performed once every 20 seconds (or 60 seconds). The minimum resolution is approx. 3 ppm (or approx. 1 ppm) and the S-35190A H Series corrects in the range of −195.3 ppm to +192.2 ppm (or of −65.1 ppm to +64.1 ppm) (Refer to **Table 13**). Users can set up this function by using the clock correction register. Regarding how to calculate the setting data, refer to "**1. How to calculate**". When not using this function, be sure to set "00h".

Table 13 Function of Clock Correction

Item	B0 = 0	B0 = 1
Correction	Every 20 seconds	Every 60 seconds
Minimum resolution	3.052 ppm	1.017 ppm
Correction range	−195.3 ppm to +192.2 ppm	−65.1 ppm to +64.1 ppm

1. How to calculate

1. 1 If current oscillation frequency > target frequency (in case the clock is fast)

$$\text{Correction value}^{*1} = 128 - \text{Integral value}\left(\frac{(\text{Current oscillation frequency actual measurement value}^{*2}) - (\text{Target oscillation frequency}^{*3})}{(\text{Current oscillation frequency actual measurement value}^{*2}) \times (\text{Minimum resolution}^{*4})}\right)$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 64.

***1.** Convert this value to be set in the clock correction register. For how to convert, refer to "**(1) Calculation example 1**".
***2.** Measurement value when 1 Hz clock pulse is output from the $\overline{\text{INT}}$ pin.
***3.** Target value of average frequency when the function of clock correction is used.
***4.** Refer to "**Table 13 Function of Clock Correction**".

(1) Calculation example 1

In case of current oscillation frequency actual measurement value = 1.000070 [Hz], target oscillation frequency = 1.000000 [Hz], B0 = 0 (Minimum resolution = 3.052 ppm)

$$\text{Correction value} = 128 - \text{Integral value}\left(\frac{(1.000070) - (1.000000)}{(1.000070) \times (3.052 \times 10^{-6})}\right)$$

$$= 128 - \text{Integral value}\,(22.93) = 128 - 22 = 106$$

Convert the correction value "106" to 7-bit binary and obtain "1101010b".
Reverse the correction value "1101010b" and set it to B7 to B1 of the clock correction register.
Thus, set the clock correction register:
(B7, B6, B5, B4, B3, B2, B1, B0) = (0, 1, 0, 1, 0, 1, 1, 0)

1. 2 If current oscillation frequency < target frequency (in case the clock is slow)

$$\text{Correction value} = \text{Integral value}\left(\frac{(\text{Target oscillation frequency}) - (\text{Current oscillation frequency actual measurement value})}{(\text{Current oscillation frequency actual measurement value}) \times (\text{Minimum resolution})}\right) + 1$$

Caution The figure range which can be corrected is that the calculated value is from 0 to 62.

(1) Calculation example 2

In case of current oscillation frequency actual measurement value = 0.999920 [Hz], target oscillation frequency = 1.000000 [Hz]. B0 = 0 (Minimum resolution = 3.052 ppm)

$$\text{Correction value} = \text{Integral value}\left(\frac{(1.000000) - (0.999920)}{(0.999920) \times (3.052 \times 10^{-6})}\right) + 1$$

$$= \text{Integral value}\,(26.21) + 1 = 26 + 1 = 27$$

Thus, set the clock correction register:
(B7, B6, B5, B4, B3, B2, B1, B0) = (1, 1, 0, 1, 1, 0, 0, 0)

(2) Calculation example 3

In case of current oscillation frequency actual measurement value = 0.999920 [Hz], target oscillation frequency = 1.000000 [Hz], B0 = 1 (Minimum resolution = 1.017 ppm)

$$\text{Correction value} = \text{Integral value}\left(\frac{(1.000000) - (0.999920)}{(0.999920) \times (1.017 \times 10^{-6})}\right) + 1$$

$$= \text{Integral value}\,(78.66) + 1$$

This calculated value exceeds the correctable range 0 to 62.
B0 = "1" (minimum resolution = 1.017 ppm) indicates the correction is impossible.

2. Setting values for registers and correction values

Table 14 Setting Values for Registers and Correction Values (Minimum Resolution: 3.052 ppm (B0 = 0))

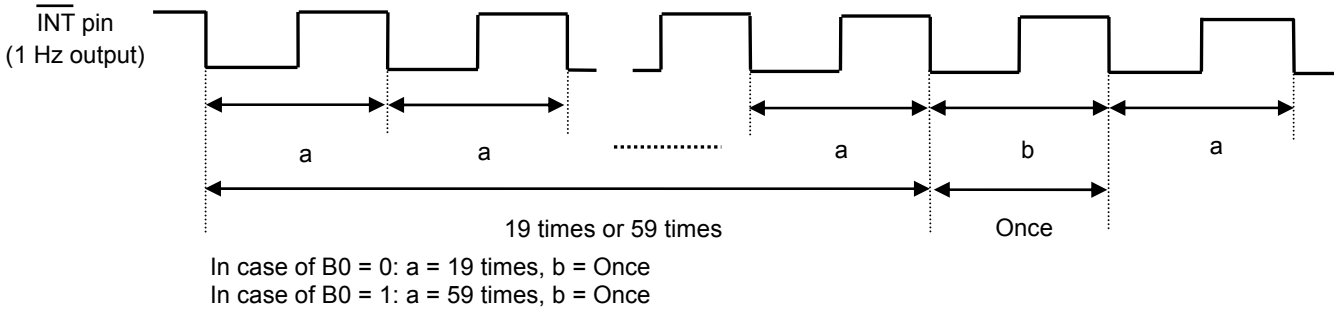
B7	B6	B5	B4	B3	B2	B1	B0	Correction Value [ppm]	Rate [s / day]
1	1	1	1	1	1	0	0	192.3	16.61
0	1	1	1	1	1	0	0	189.2	16.35
1	0	1	1	1	1	0	0	186.2	16.09
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	0	0	6.1	0.53
1	0	0	0	0	0	0	0	3.1	0.26
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	0	–3.1	–0.26
0	1	1	1	1	1	1	0	–6.1	–0.53
1	0	1	1	1	1	1	0	–9.2	–0.79
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	1	0	–189.2	–16.35
1	0	0	0	0	0	1	0	–192.3	–16.61
0	0	0	0	0	0	1	0	–195.3	–16.88

Table 15 Setting Values for Registers and Correction Values (Minimum Resolution: 1.017 ppm (B0 = 1))

B7	B6	B5	B4	B3	B2	B1	B0	Correction Value [ppm]	Rate [s / day]
1	1	1	1	1	1	0	1	64.1	5.54
0	1	1	1	1	1	0	1	63.1	5.45
1	0	1	1	1	1	0	1	62.0	5.36
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	0	1	2.0	0.18
1	0	0	0	0	0	0	1	1.0	0.09
0	0	0	0	0	0	0	1	0	0
1	1	1	1	1	1	1	1	–1.0	–0.09
0	1	1	1	1	1	1	1	–2.0	–0.18
1	0	1	1	1	1	1	1	–3.0	–0.26
				•				•	•
				•				•	•
				•				•	•
0	1	0	0	0	0	1	1	–63.1	–5.45
1	0	0	0	0	0	1	1	–64.1	–5.54
0	0	0	0	0	0	1	1	–65.1	–5.62

3. How to confirm a setting value for a register and the result of correction

The S-35190A H Series does not adjust the frequency of the crystal oscillation by using the function of clock correction. Therefore users cannot confirm if it is corrected or not by measuring output 32.768 kHz. When the function of clock correction is being used, the cycle of 1 Hz clock pulse output from the $\overline{\text{INT}}$ pin changes once in 20 times or 60 times, as shown in **Figure 33**.



In case of B0 = 0: a = 19 times, b = Once
In case of B0 = 1: a = 59 times, b = Once

Figure 33 Confirmation of Clock Correction

Measure a and b by using the frequency counter*1. Calculate the average frequency (Tave) based on the measurement results.

B0 = 0, Tave = (a × 19 + b) ÷ 20
B0 = 1, Tave = (a × 59 + b) ÷ 60

Calculate the error of the clock based on the average frequency (Tave). The following shows an example for confirmation.

Confirmation example: When B0 = 0, 66h is set

Measurement results: a = 1.000080 Hz, b = 0.998493 Hz

Clock Correction Register Setting Value		Average frequency [Hz]	Per Day [s]
Before correction	00 h (Tave = a)	1.000080	86393
After correction	66 h (Tave = (a × 19 + b) ÷ 20)	1.00000065	86399.9

Calculating the average frequency allows to confirm the result of correction.

***1.** Use a high-accuracy frequency counter of 7 digits or more.

Caution Measure the oscillation frequency under the usage conditions.

■ Serial Interface

The S-35190A H Series receives various commands via 3-wire serial interface to read / write data. Regarding transmission is as follows.

1. Data reading

When data is input from the SIO pin in synchronization with the falling of the $\overline{SCK}$ clock after setting the CS pin to "H", the data is loaded internally in synchronization with the next rising of the $\overline{SCK}$ clock. When R / $\overline{W}$ bit = "1" is loaded at the eighth rising of the $\overline{SCK}$ clock, the status of data reading is entered. Data corresponding to each command is then output in synchronization with the falling of the subsequent $\overline{SCK}$ clock input. When the $\overline{SCK}$ clock is less than 8, the IC is in the clock-wait status, and no processing is performed.

2. Data writing

When data is input from the SIO pin in synchronization with the falling of the $\overline{SCK}$ clock after setting the CS pin to "H", the data is loaded internally in synchronization with the next rising of the $\overline{SCK}$ clock. When R / $\overline{W}$ bit = "0" is loaded at the eighth rising of the $\overline{SCK}$ clock, the status of data writing is entered. In this status, the data, which is input in synchronization with the falling of the subsequent $\overline{SCK}$ clock input, is written to registers according to each command. In data writing, input a clock pulse which is equivalent to the byte of the register. As well as reading, when the $\overline{SCK}$ clock is less than 8, the IC is in the clock-wait status, and no processing is performed.

3. Data access

3. 1 Real-time data 1 access

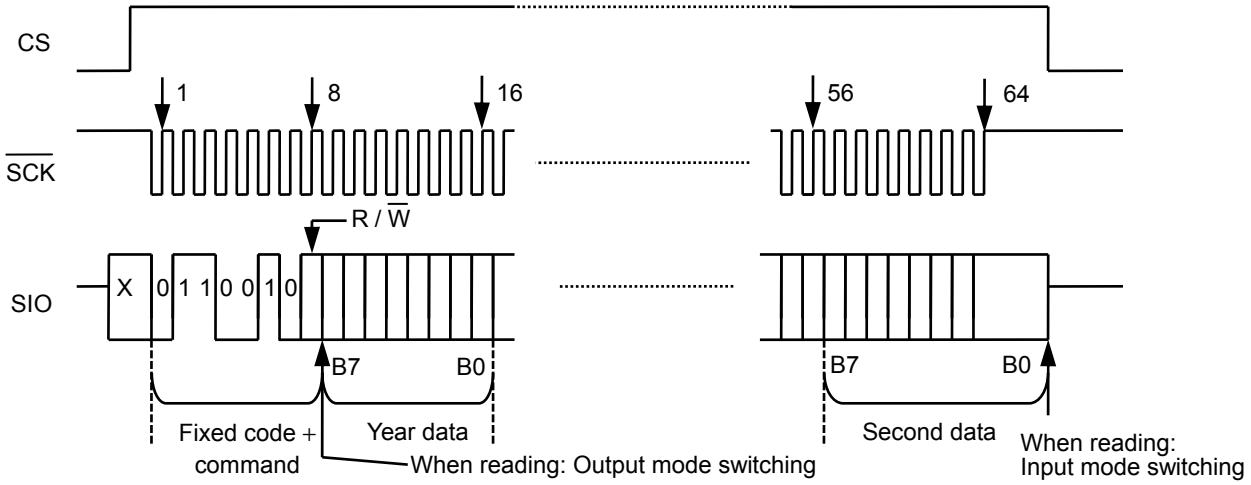


Figure 34 Real-Time Data 1 Access

3. 2 Real-time data 2 access

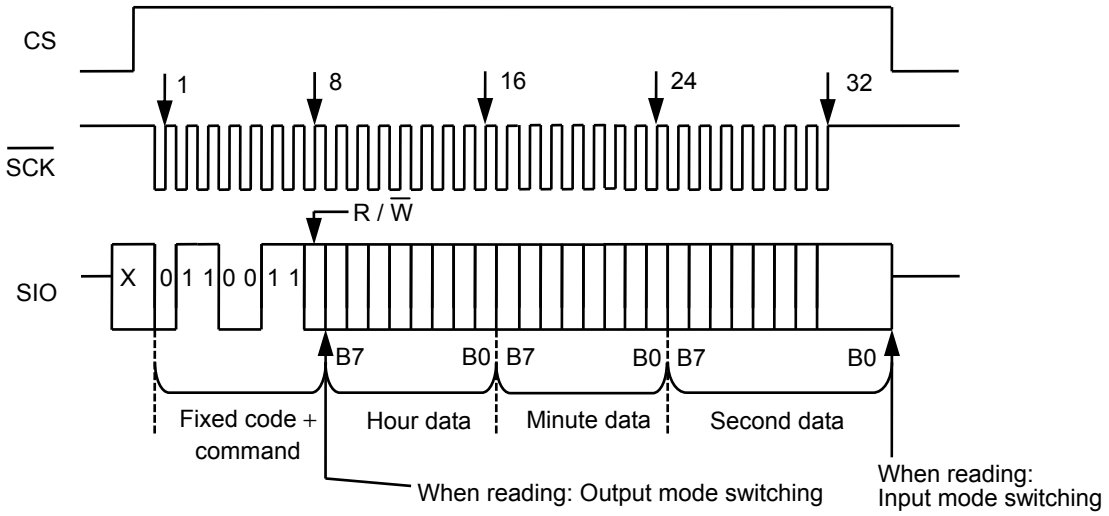
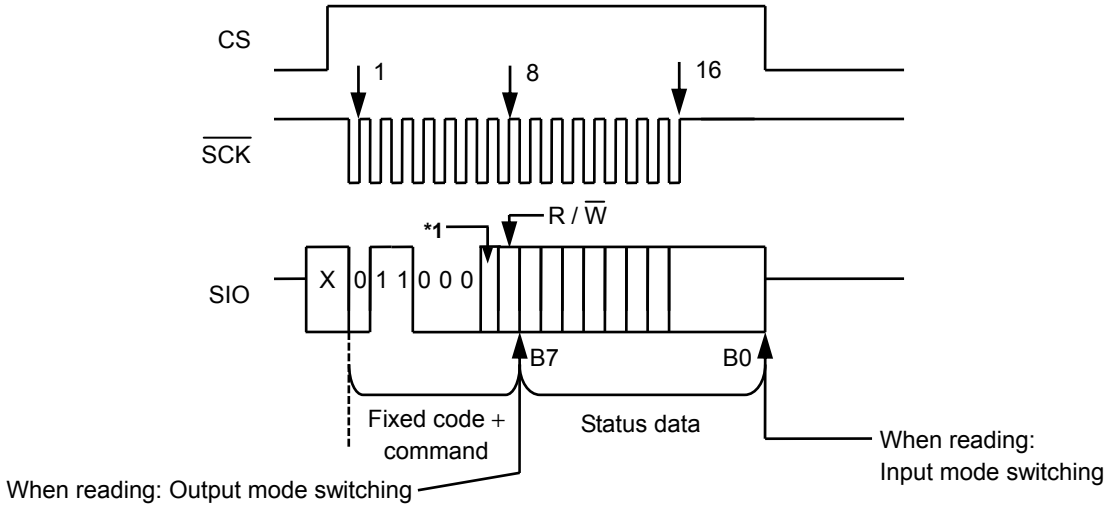


Figure 35 Real-Time Data 2 Access

3. 3 Status register 1 access and status register 2 access



***1.** 0: Status register 1 selected
1: Status register 2 selected

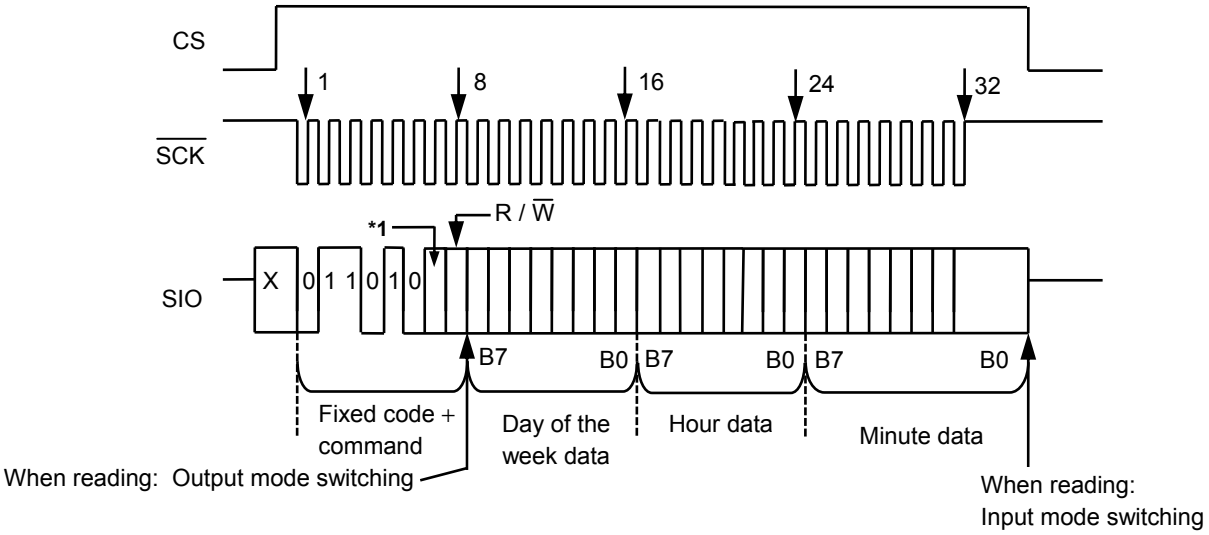
Figure 36 Status Register 1 Access and Status Register 2 Access

3. 4 INT register 1 access and INT register 2 access

In read / write the INT register 1, data varies depending on the setting of the status register 2. Be sure to read / write the INT register 1 after setting the status register 2. When setting the alarm by using the status register 2, these registers work as 3-byte alarm time data registers, in other statuses, they work as 1-byte registers. When outputting the user-set frequency, they are the data registers to set up the frequency.

Read / write the INT register 2 after setting INT2AE in the status register 2. When INT2AE is in "1", the INT register 2 works as for setting the 3-byte alarm time data. The INT register 2 does not have the function to output the user-set frequency. Regarding details of each data, refer to "**4. INT register 1 and INT register 2**" in "**■ Configuration of Register**".

Caution Users cannot use both functions of alarm 1 interrupt and the output of user-set frequency simultaneously.



***1.** 0: INT register 1 selected
1: INT register 2 selected

Figure 37 INT Register 1 Access and INT Register 2 Access

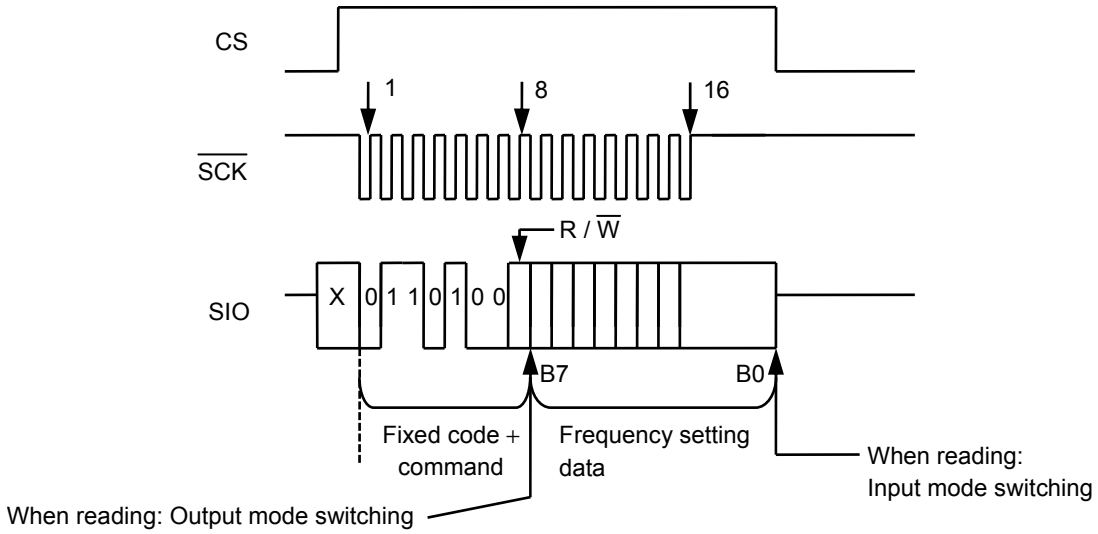


Figure 38 INT Register 1 (Data Register for output frequency) Access

3. 5 Clock correction register access

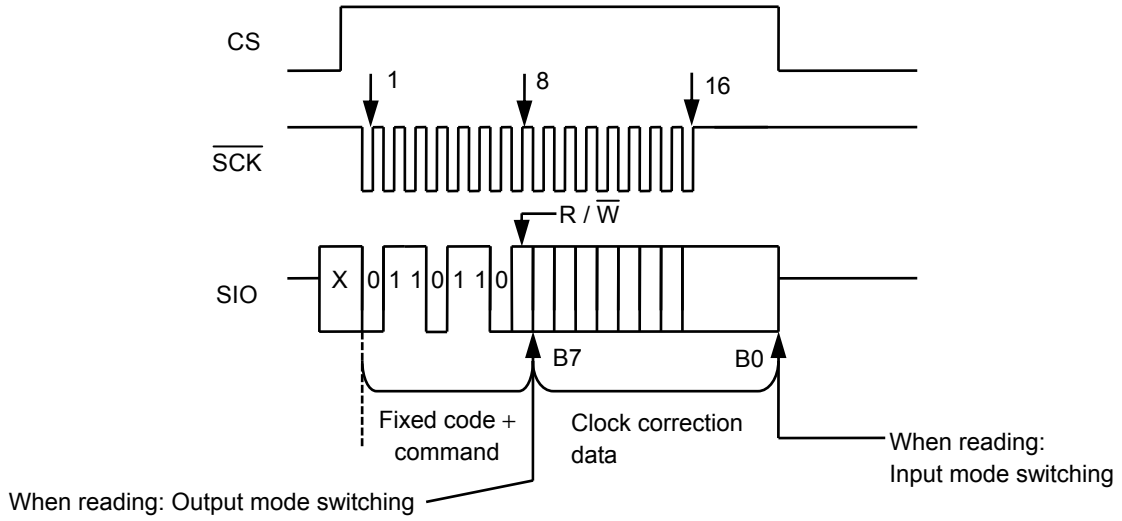


Figure 39 Clock Correction Register Access

3. 6 Free register access

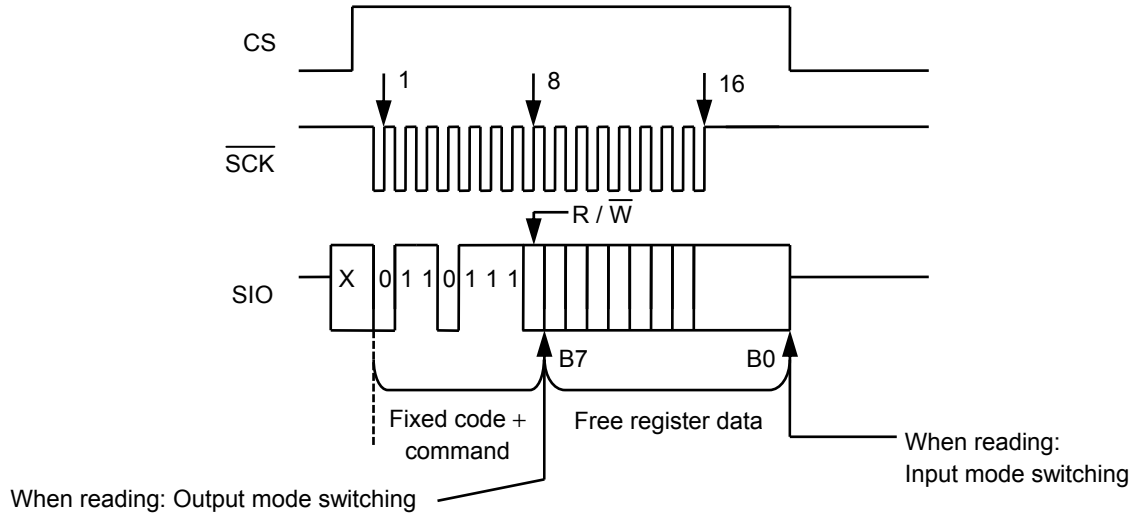
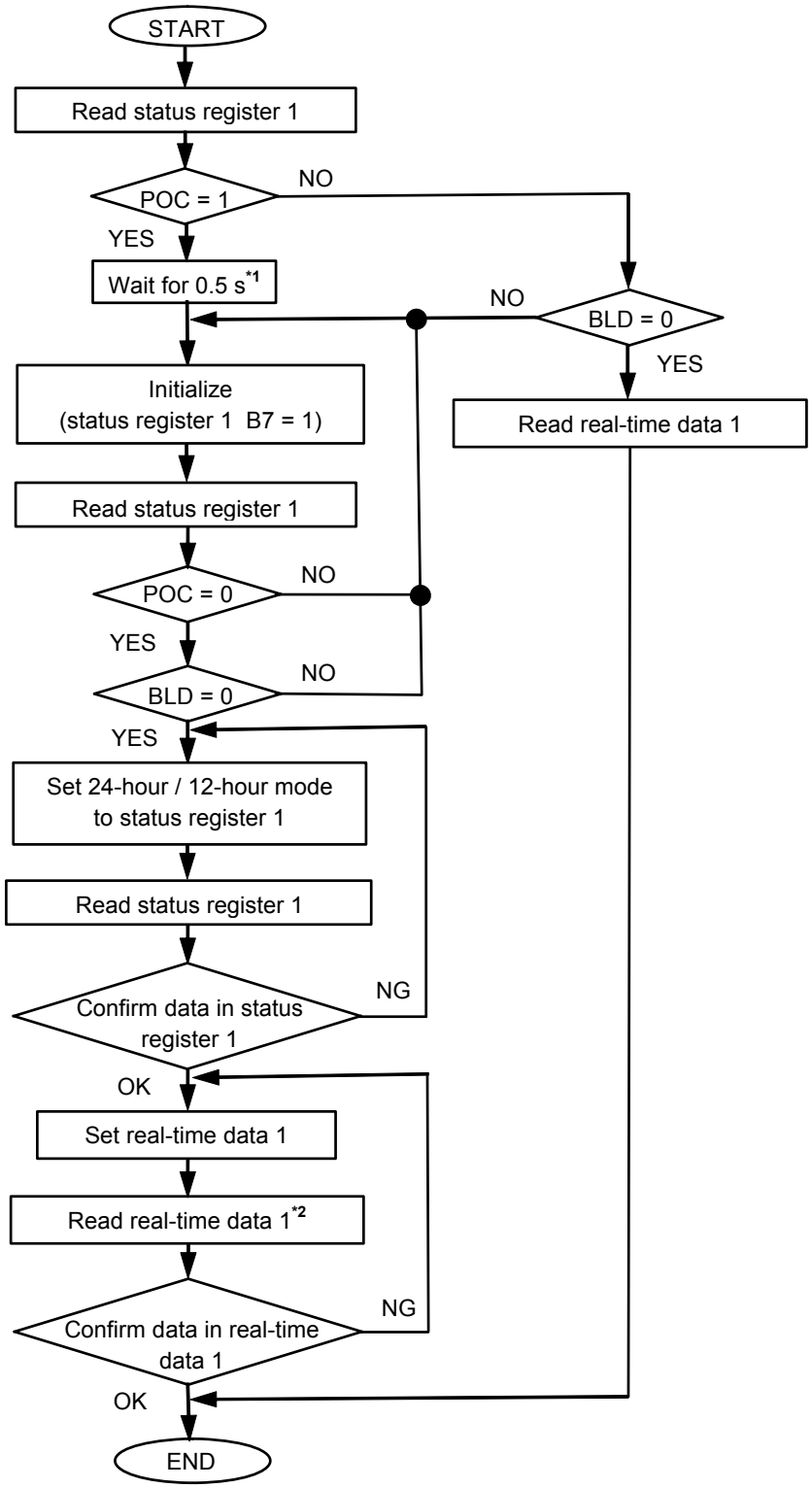


Figure 40 Free Register Access

■ Flowchart of Initialization and Example of Real-time Data Set-up

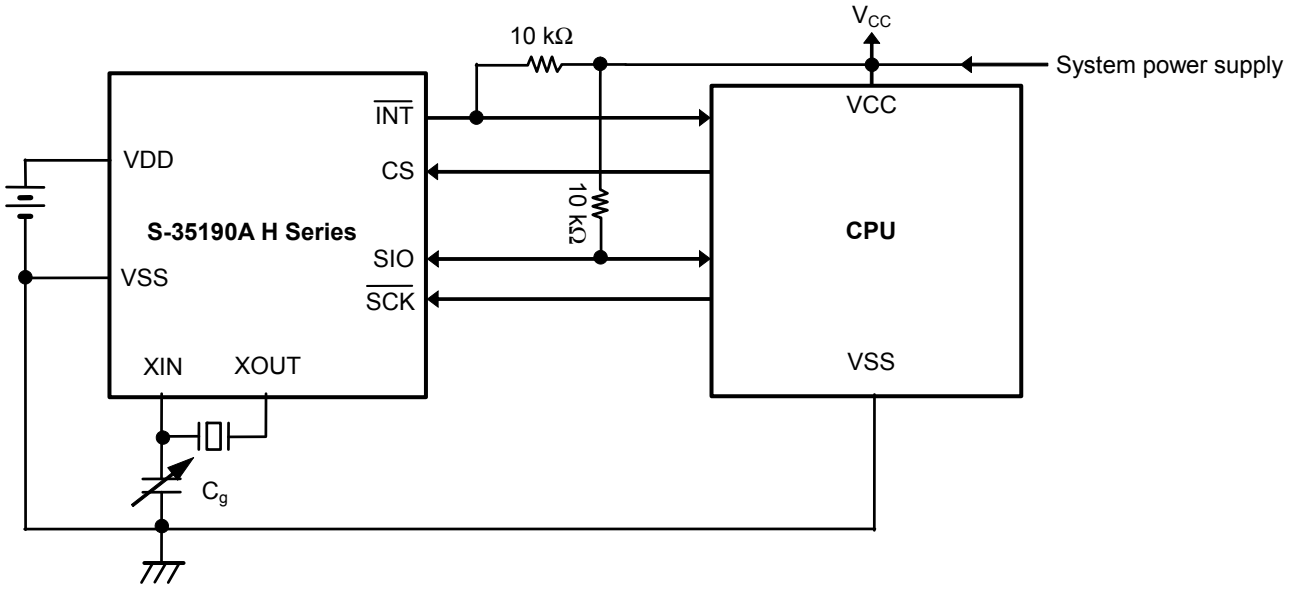
Figure 41 is a recommended flowchart when the master device shifts to a normal operation status and initiates communication with the S-35190A H Series. Regarding how to apply power, refer to "**■ Power-on Detection Circuit and Register Status**". It is unnecessary for users to comply with this flowchart of real-time data strictly. And if using the default data at initializing, it is also unnecessary to set up again.



***1.** Do not communicate for 0.5 seconds since the power-on detection circuit is in operation.
***2.** Reading the real-time data 1 should be completed within 1 second after setting the real-time data 1.

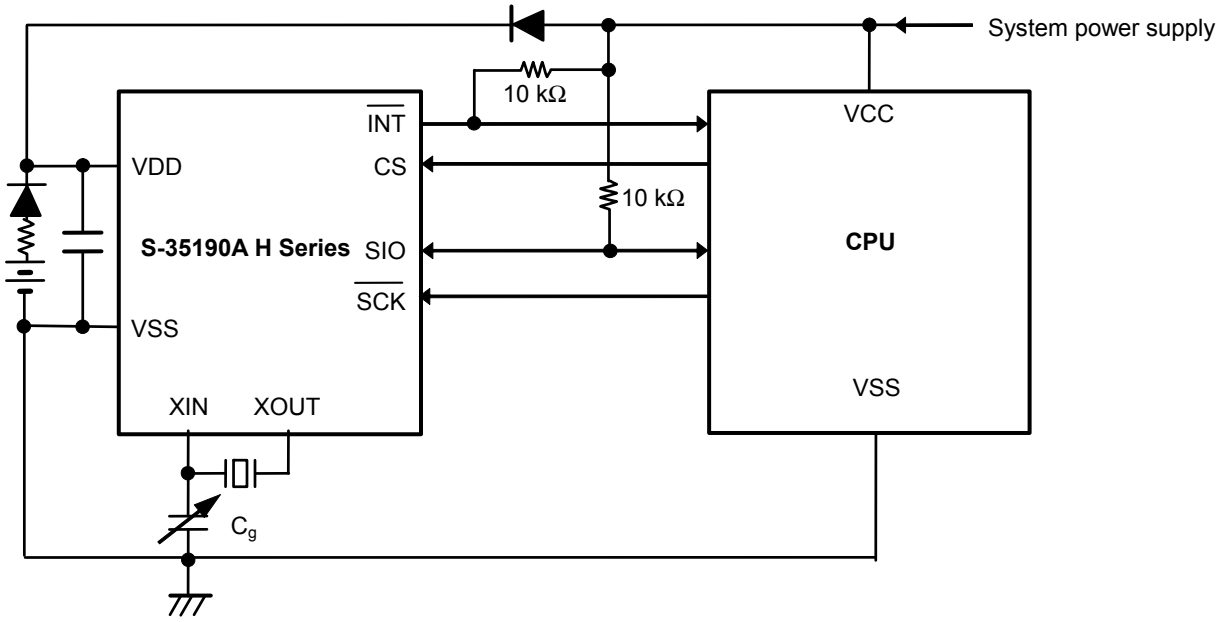
Figure 41 Example of Initialization Flowchart

■ Examples of Application Circuits



Caution 1. Because the I/O pin has no protective diode on the VDD side, the relation of $V_{CC} \geq V_{DD}$ is possible. But pay careful attention to the specifications.
2. Start communication under stable condition after power-on the power supply in the system.

Figure 42 Application Circuit 1



Caution Start communication under stable condition after power-on the power supply in the system.

Figure 43 Application Circuit 2

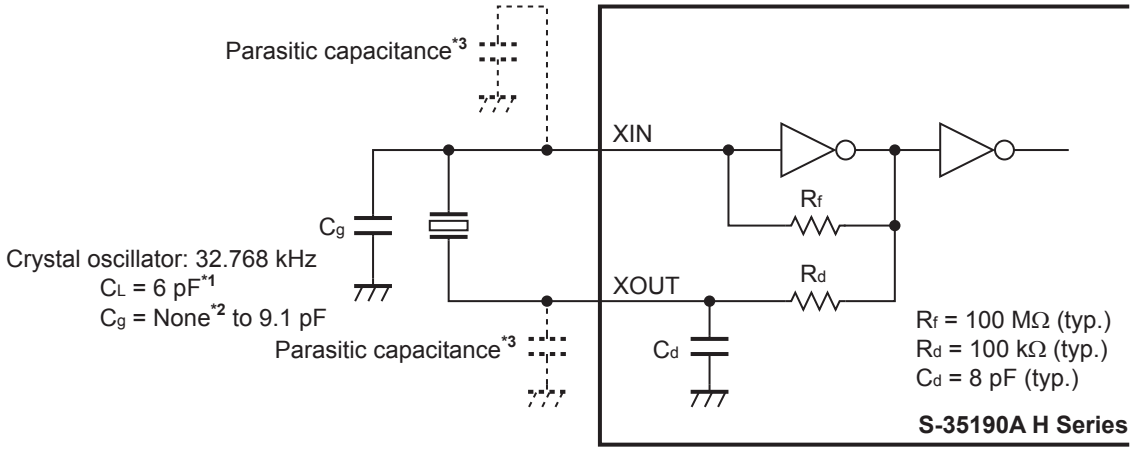
Caution The above connection diagrams do not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

■ Adjustment of Oscillation Frequency

1. Configuration of crystal oscillation circuit

Since the crystal oscillation circuit is sensitive to external noise (the clock accuracy is affected), the following measures are essential for optimizing the configuration.

- Place the S-35190A H Series, crystal oscillator, and external capacitor (C_g) as close to each other as possible.
- Increase the insulation resistance between pins and the substrate wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locating the GND layer immediately below the crystal oscillation circuit is recommended.
- Locate the bypass capacitor adjacent to the power supply pin of the S-35190A H Series.



***1.** When setting the value for the crystal oscillator's C_L as 7 pF, connect C_d externally if necessary.
***2.** The crystal oscillation circuit operates even when C_g is not connected. Note that the oscillation frequency is in the direction that it advances.
***3.** Design the board so that the parasitic capacitance is within 5 pF.

Figure 44 Connection Diagram 1

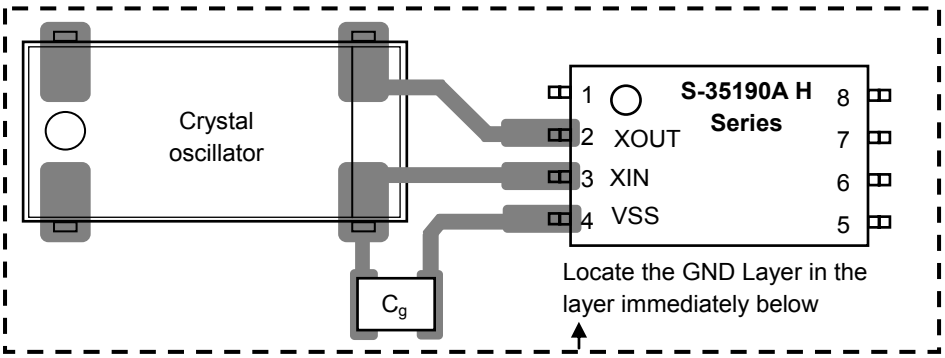


Figure 45 Connection Diagram 2

Caution 1. When using the crystal oscillator with a C_L exceeding the rated value (7 pF) (e.g: C_L = 12.5 pF), oscillation operation may become unstable. Use a crystal oscillator with a C_L value of 6 pF or 7 pF.
2. Oscillation characteristics are subject to the variation of each component such as substrate parasitic capacitance, parasitic resistance, crystal oscillator, and C_g. When configuring a crystal oscillation circuit, pay sufficient attention for them.

2. Measurement of oscillation frequency

When the S-35190A H Series is turned on, the internal power-on detection circuit operates and a signal of 1 Hz is output from the $\overline{INT}$ pin to select the crystal oscillator and optimize the C_g value. Turn the power on and measure the signal with a frequency counter following the circuit configuration shown in **Figure 46**.
If 1 Hz signal is not output, the power-on detection circuit does not operate normally. Turn off the power and then turn it on again. For how to apply power, refer to "**■ Power-on Detection Circuit and Register Status**".

Remark If the error range is ±1 ppm in relation to 1 Hz, the time is shifted by approximately 2.6 seconds per month (calculated using the following expression).
10^{-6} (1 ppm) × 60 seconds × 60 minutes × 24 hours × 30 days = 2.592 seconds

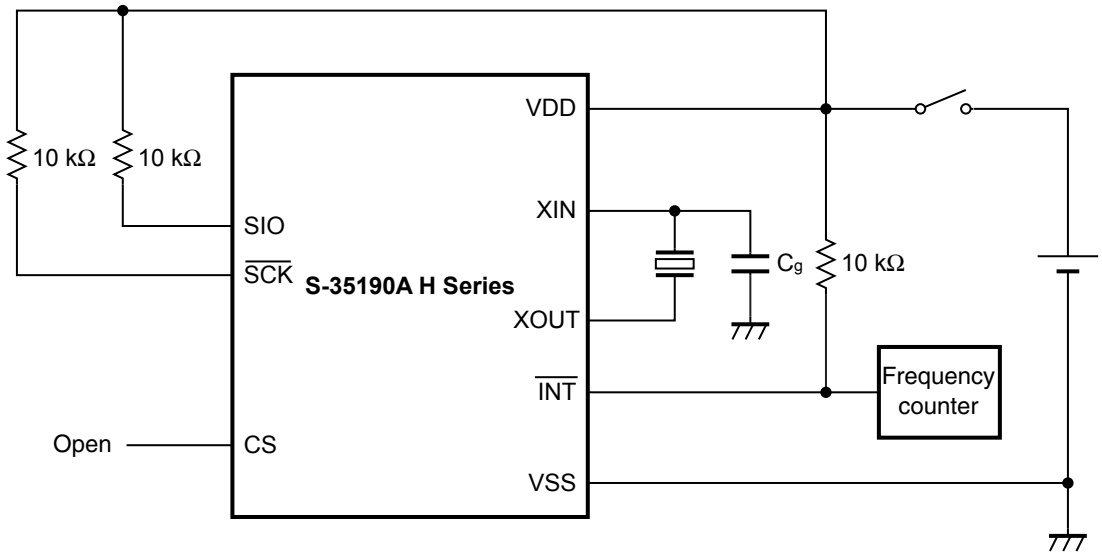


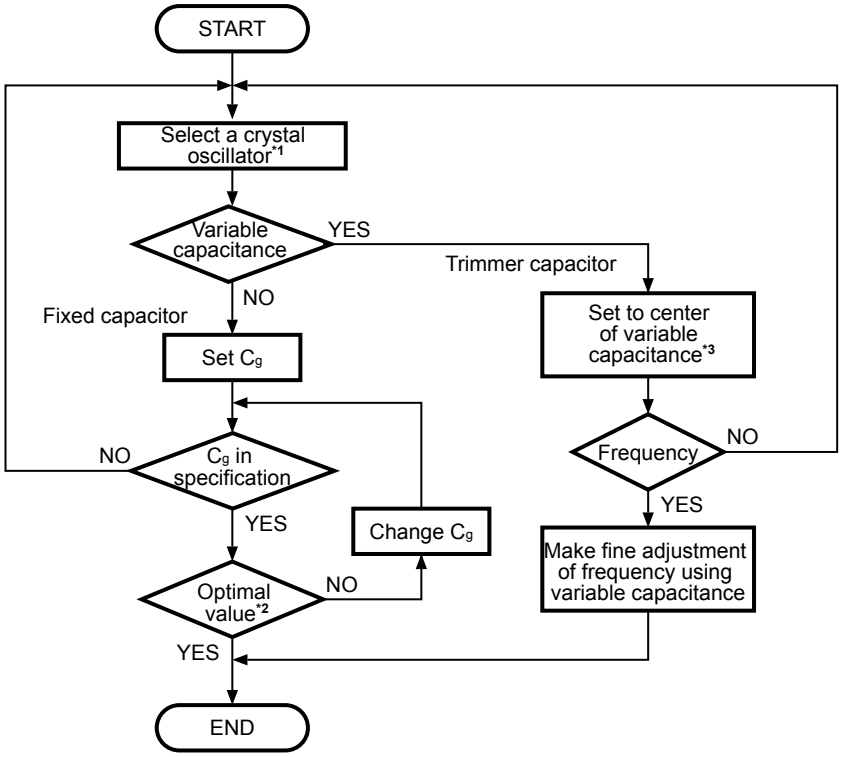
Figure 46 Configuration of Oscillation Frequency Measurement Circuit

Caution
1. **Use a high-accuracy frequency counter of 7 digits or more.**
2. **Measure the oscillation frequency under the usage conditions.**
3. **Since the 1 Hz signal continues to be output, initialization must be executed during normal operation.**

3. Adjustment of oscillation frequency

3. 1 Adjustment by setting C_g

Matching of the crystal oscillator with the nominal frequency must be performed with the parasitic capacitance on the board included. Select a crystal oscillator and optimize the C_g value in accordance with the flowchart below.



***1.** Request a crystal manufacturer for a matching evaluation between the IC and the crystal oscillator. The recommended crystal characteristic value is C_L value (load capacitance) = 6 pF. When using the S-35190A H Series and a crystal oscillator in the environment exceeding Ta = +85°C, it is recommended to ensure that the oscillation allowance is at least seven times at normal temperature.

***2.** The C_g value must be selected on the actual PCB since it is affected by parasitic capacitance. Select the external C_g value in a range of 0 pF to 9.1 pF.

***3.** Adjust the rotation angle of the variable capacitance so that the capacitance value is slightly smaller than the center, and confirm the oscillation frequency and the center value of the variable capacitance. This is done in order to make the capacitance of the center value smaller than one half of the actual capacitance value because a smaller capacitance value increases the frequency variation

Figure 47 Crystal Oscillator Setting Flow

Caution 1. The oscillation frequency varies depending on the ambient temperature and power supply voltage. Refer to "■ Characteristics (Typical Data)".

2. The 32.768 kHz crystal oscillator operates more slowly at an operating temperature higher or lower than +20°C to +25°C. Therefore, it is recommended to set the oscillator to operate slightly faster at normal temperature.

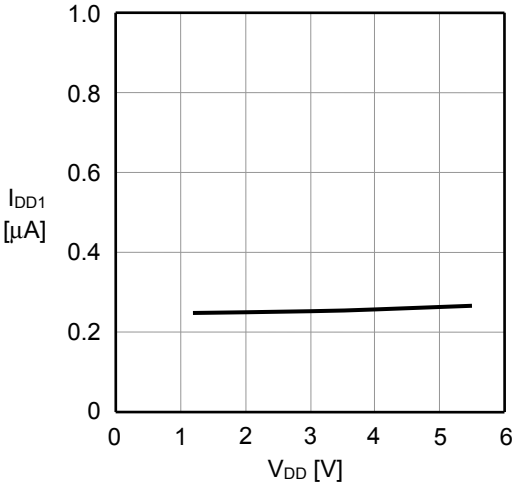
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

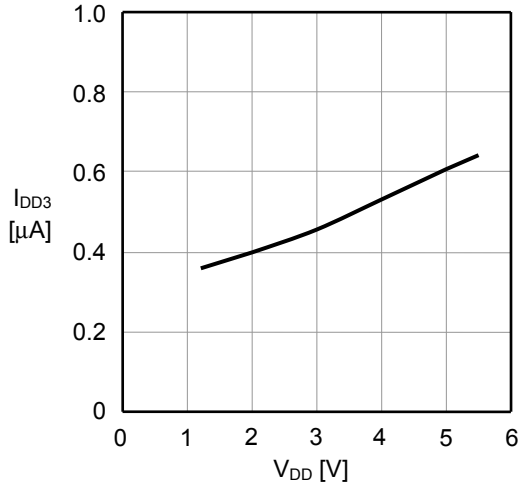
1. Standby current vs. V_{DD} characteristics

Ta = +25°C, C_L = 6 pF



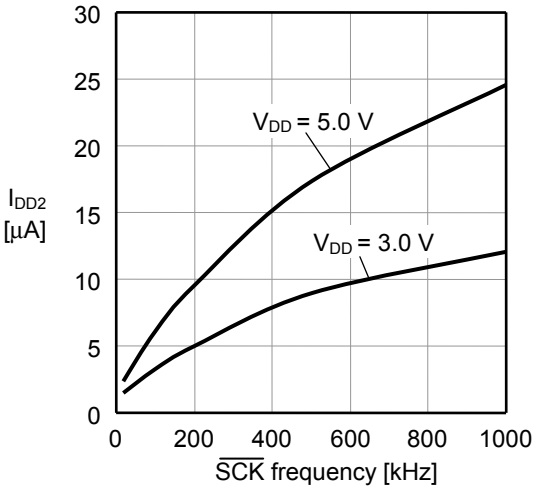
2. Current consumption when 32.768 kHz is output vs. V_{DD} characteristics

Ta = +25°C, C_L = 6 pF



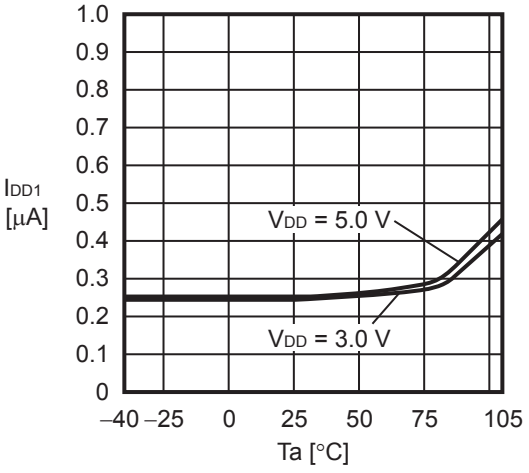
3. Current consumption during operation vs. Input clock characteristics

Ta = +25°C, C_L = 6 pF



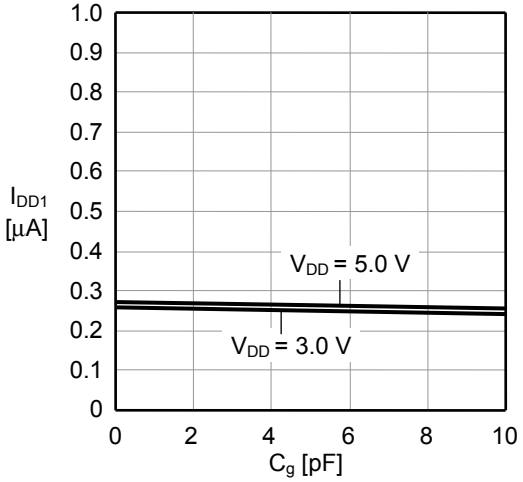
4. Standby current vs. Temperature characteristics

C_L = 6 pF



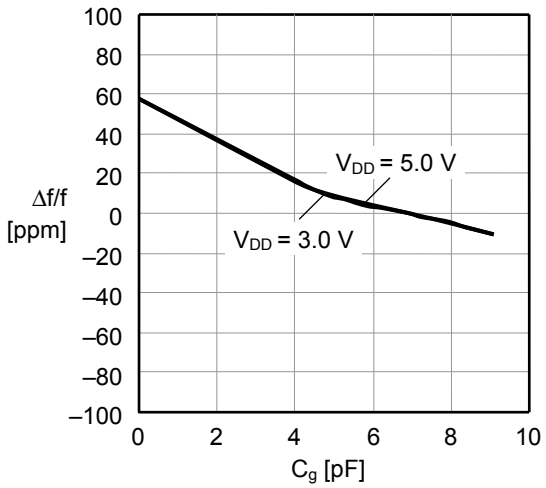
5. Standby current vs. C_g characteristics

Ta = +25°C, C_L = 6 pF

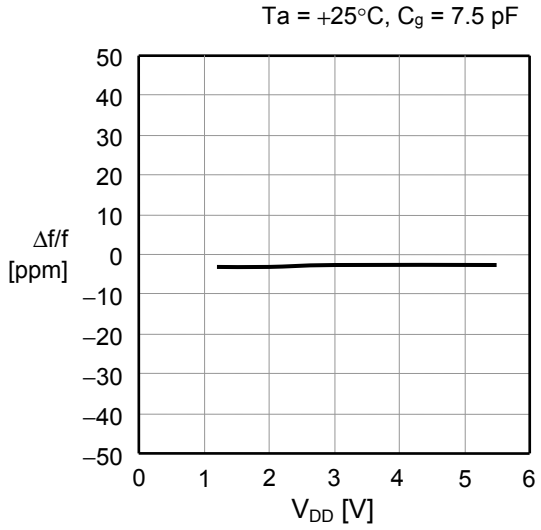


6. Oscillation frequency vs. C_g characteristics

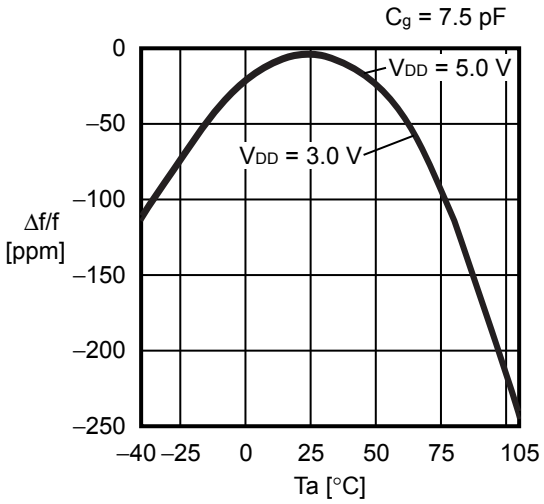
Ta = +25°C, C_L = 6 pF



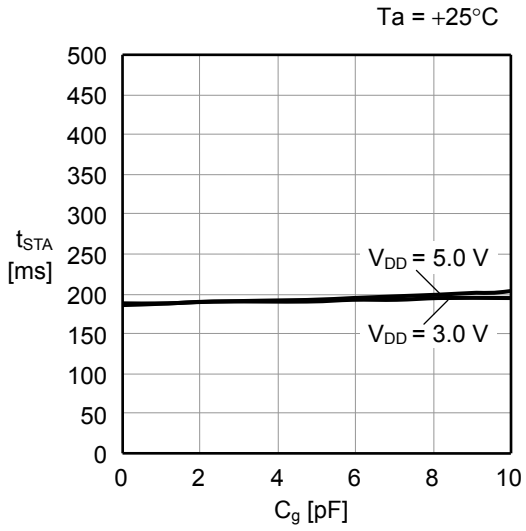
7. Oscillation frequency vs. V_{DD} characteristics



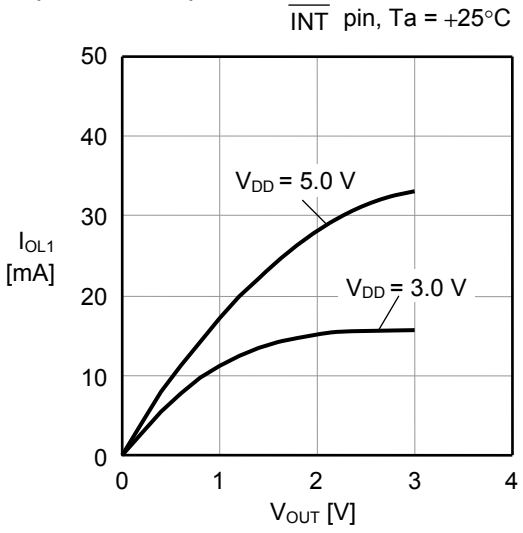
8. Oscillation frequency vs. Temperature characteristics



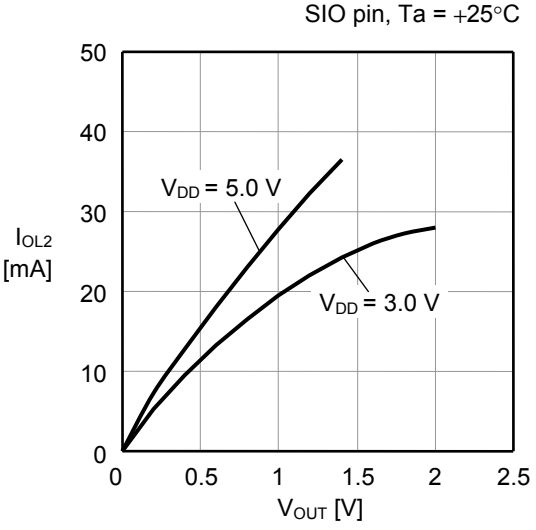
9. Oscillation start time vs. C_g characteristics



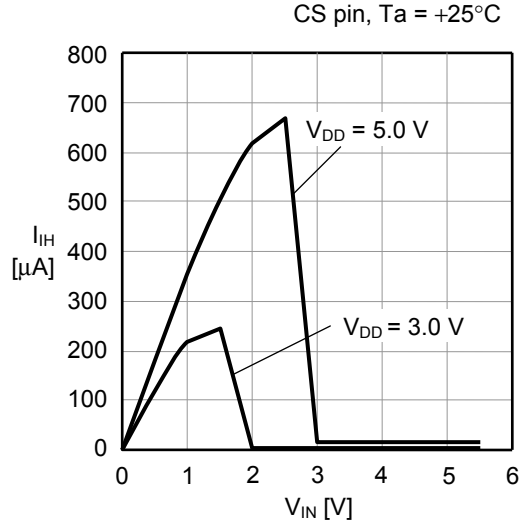
10. Output current characteristics 1 (V_{OUT} vs. I_{OL1})



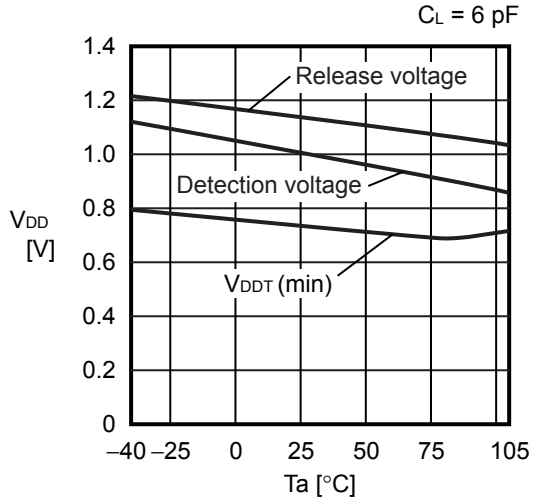
11. Output current characteristics 2 (V_{OUT} vs. I_{OL2})

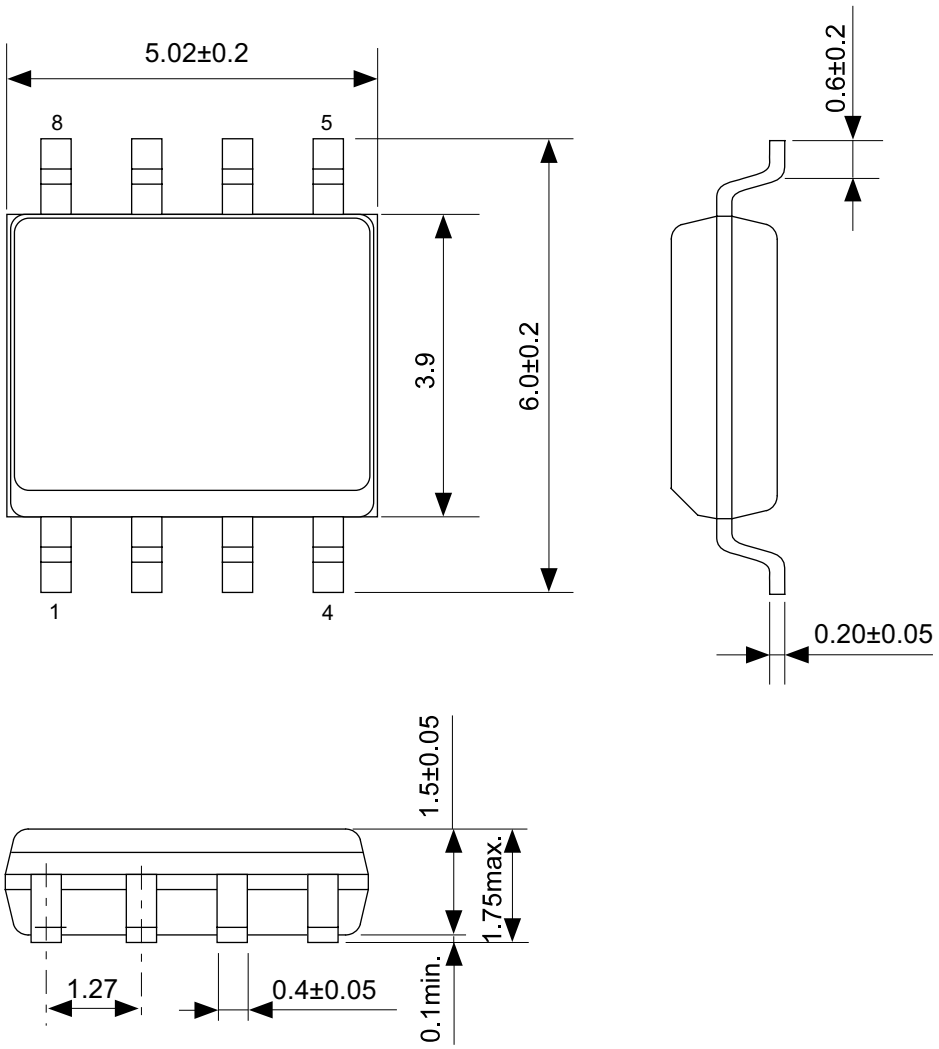


12. CS pin input current characteristics



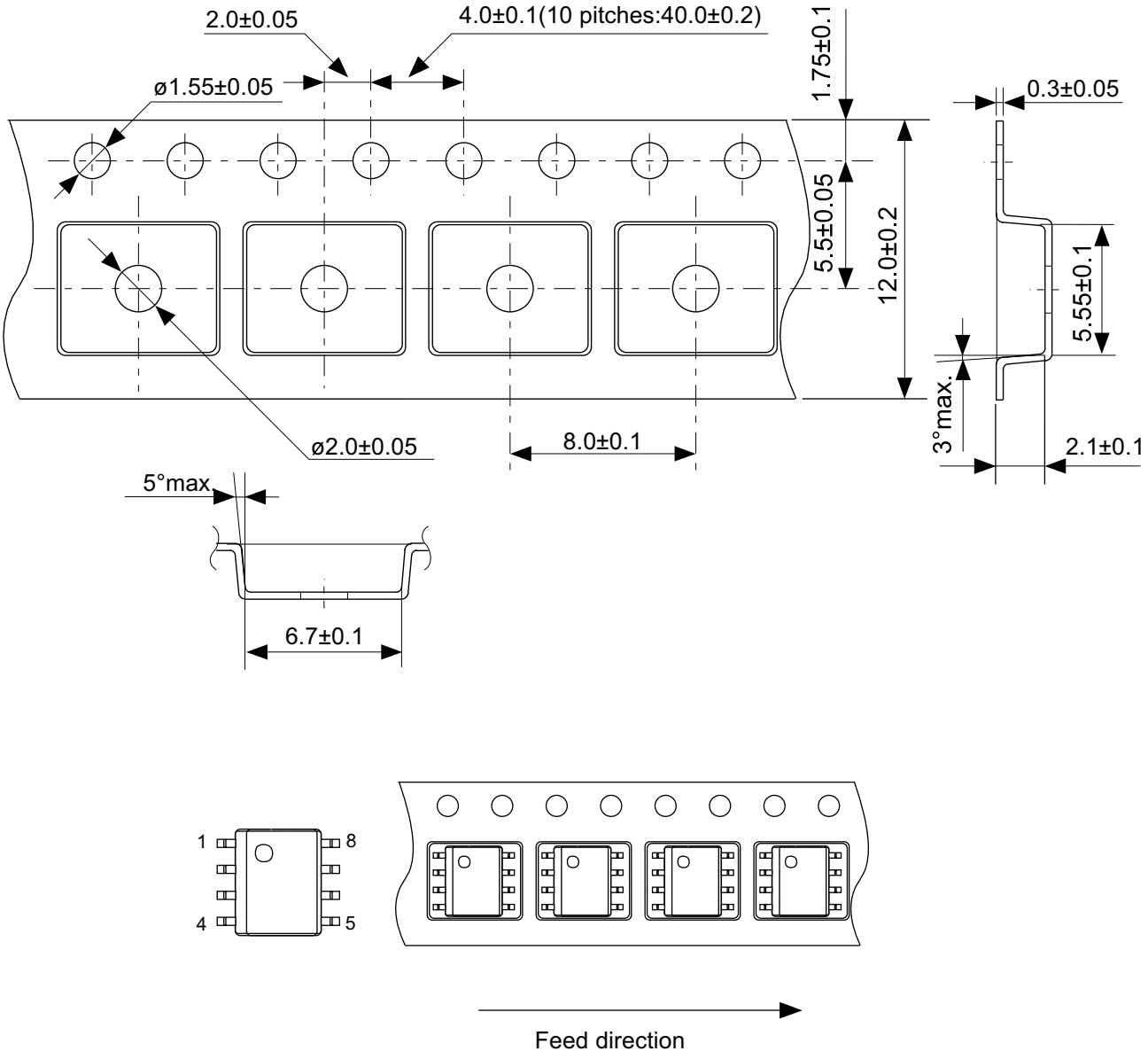
13. BLD detection, release voltage, V_{DDT} (min.) vs. Temperature characteristics





No. FJ008-A-P-SD-2.1

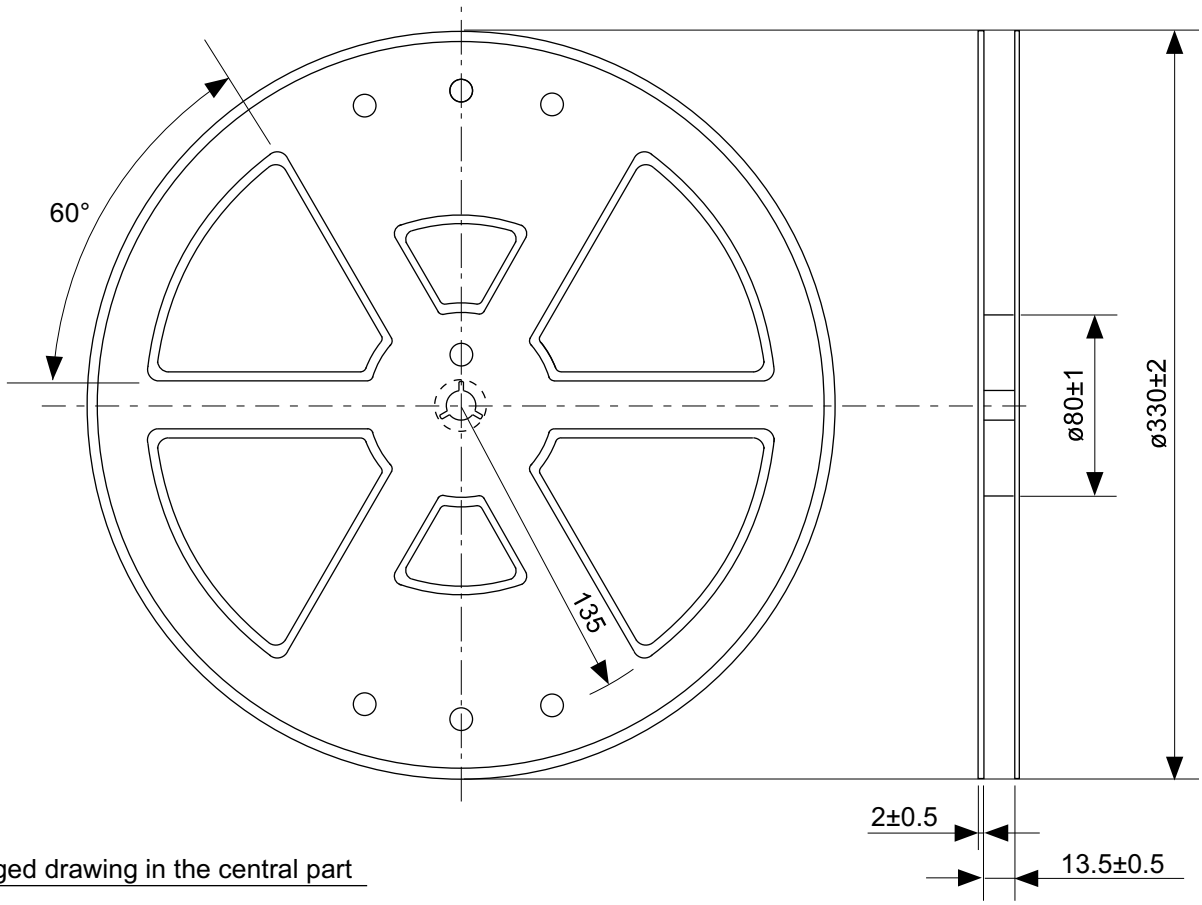
TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	



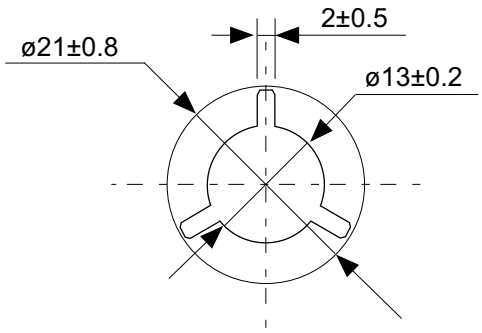
Feed direction

No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	

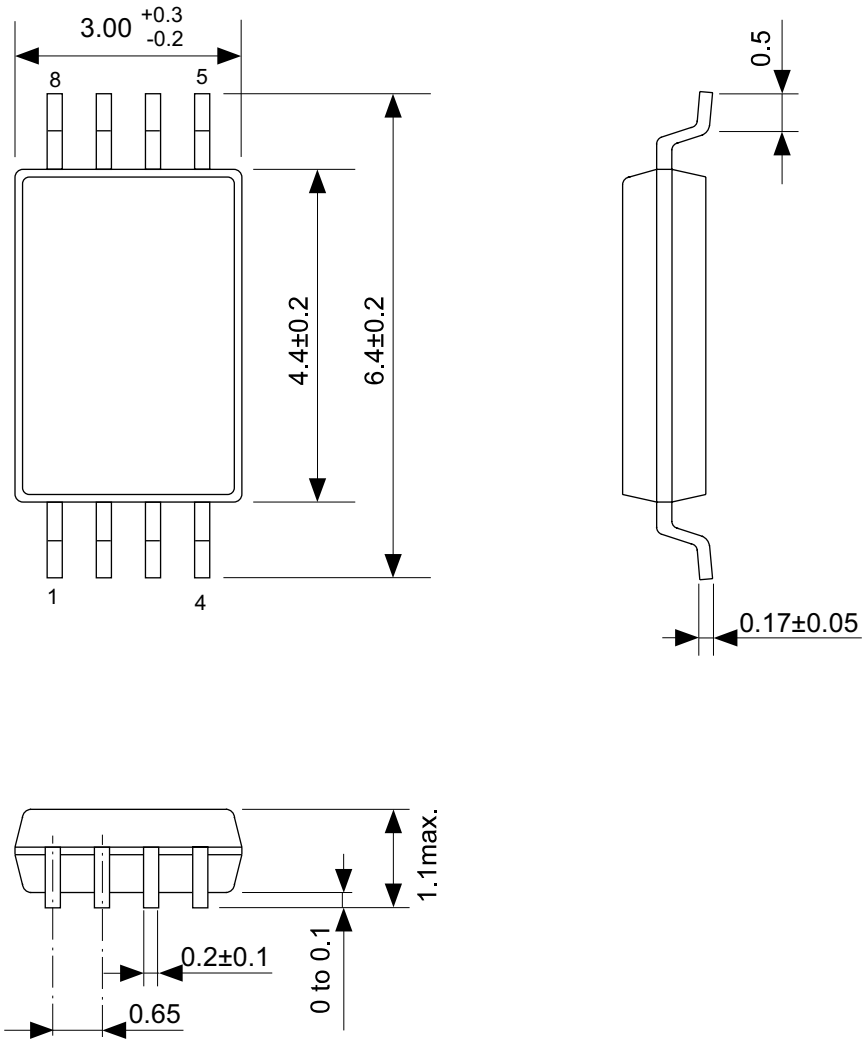


Enlarged drawing in the central part



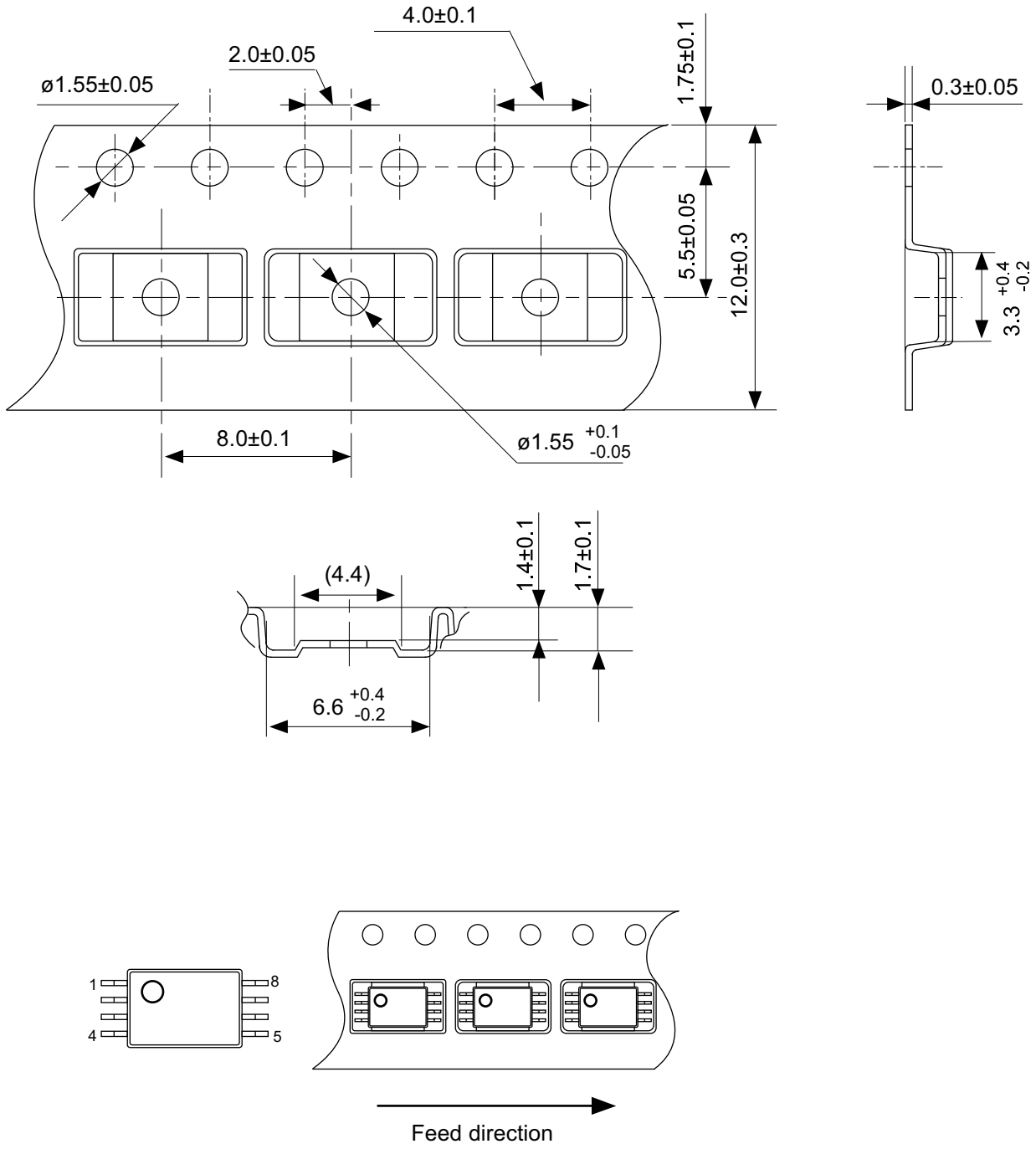
No. FJ008-D-R-S1-1.0

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-S1-1.0		
SCALE		QTY.	4,000
UNIT	mm		
SII Semiconductor Corporation			



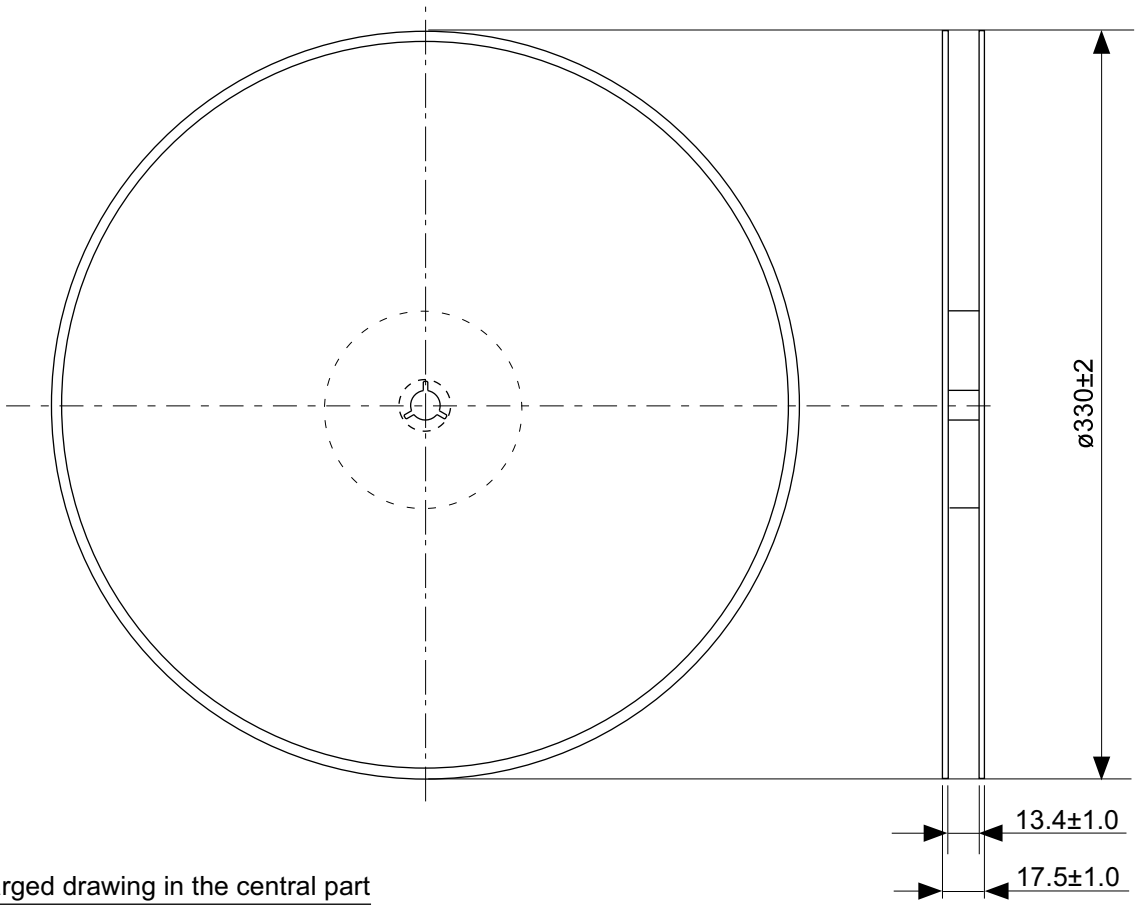
No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	

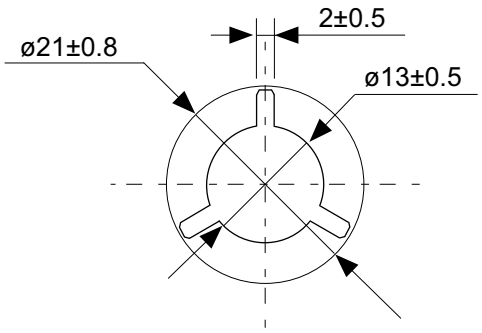


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
SII Semiconductor Corporation	



Enlarged drawing in the central part



No. FT008-E-R-S1-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-1.0		
SCALE		QTY.	4,000
UNIT	mm		
SII Semiconductor Corporation			

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