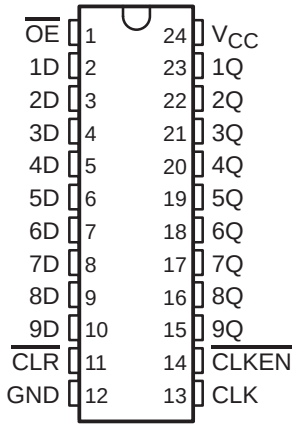
- **Functionally Equivalent to AMD's AM29823**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Outputs Have Undershoot-Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs Reduce dc Loading Effects**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54ALS29823 . . . JT PACKAGE
SN74ALS29823 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 9-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing, and working registers.

With the clock-enable ($\overline{CLKEN}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock (CLK) input. Taking $\overline{CLKEN}$ high disables the clock buffer, latching the outputs. The ′ALS29823 have noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input places the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS29823 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS29823 is characterized for operation from 0°C to 70°C.

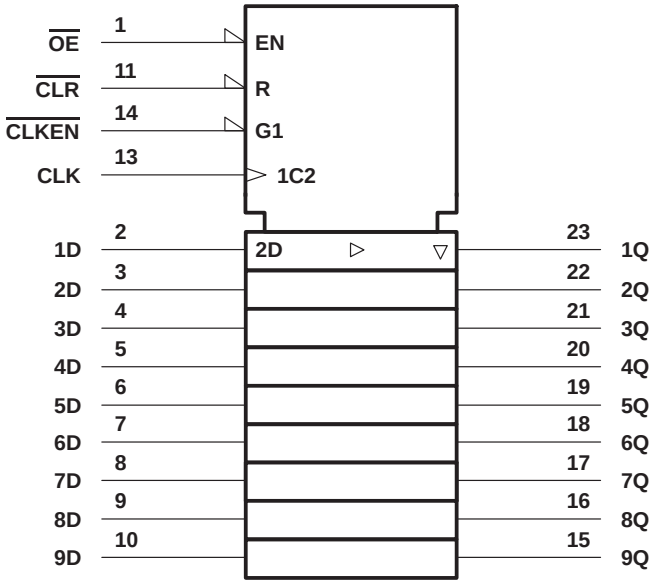
FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUT
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

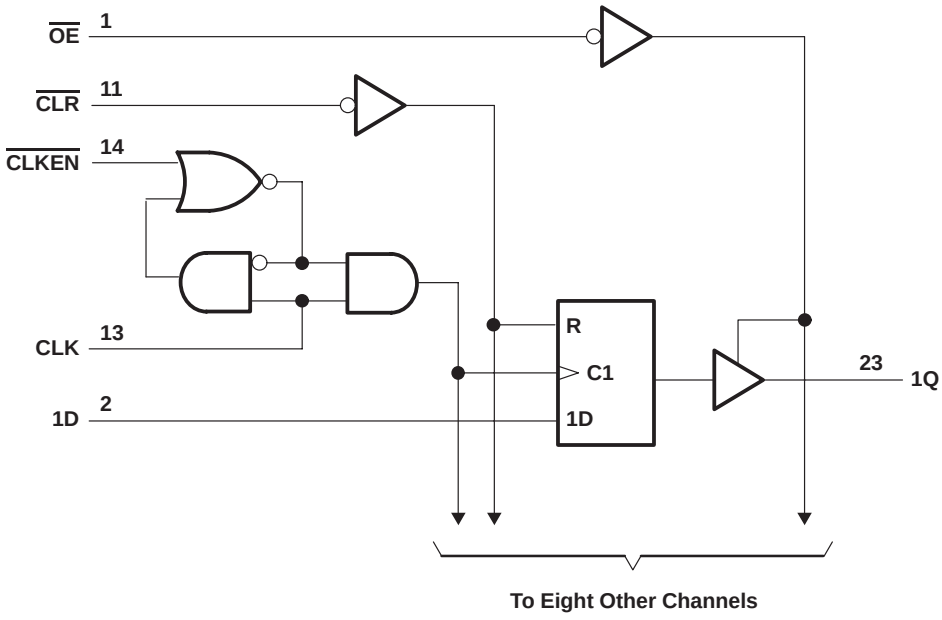
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Voltage applied to a disabled high-impedance output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS29823 . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS29823			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–18	mA
I_{OL}	Low-level output current				32	mA
t_w	Pulse duration	$\overline{CLR}$ low	7			ns
		CLK high or low	8			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	7			ns
		Data	4			
		$\overline{CLKEN}$ high or low	8			
t_h	Hold time after CLK↑	$\overline{CLKEN}$	2			ns
		Data	4			
T_A	Operating free-air temperature		–55	25	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS29823			UNIT
			MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –12 mA	2.4	3.3		V
		I_{OH} = –18 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.4 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.5	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	–75		–250	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high			90	mA
		Outputs low			105	
		Outputs open			115	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = MIN to MAX†, T_A = MIN to MAX†		UNIT
				SN54ALS29823		
				MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2	11.5	ns
t_{PHL}				2	11.5	
t_{PLH}	CLK	Any Q	C_L = 300 pF	2	21	ns
t_{PHL}				2	21	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF	1	17.5	ns
t_{PZH}	$\overline{OE}$	Any Q	C_L = 50 pF	1	17	ns
t_{PZL}				1	17	
t_{PZH}	$\overline{OE}$	Any Q	C_L = 300 pF	1	25	ns
t_{PZL}				1	29.5	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 50 pF	1	16	ns
t_{PLZ}				1	14	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 5 pF	1	12	ns
t_{PLZ}				1	11	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74ALS29823 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN74ALS29823			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			ns
		CLK high or low	5			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	5			ns
		Data	2			
		$\overline{CLKEN}$ high or low	6			
t_h	Hold time after CLK↑	$\overline{CLKEN}$	0			ns
		Data	2			
T_A	Operating free-air temperature		0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS29823			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.75 V	I_{OH} = –15 mA	2.4	3.3		V
		I_{OH} = –24 mA	2	3.1		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.4 V			20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.2	mA
I_{OS}‡	V_{CC} = 5.25 V,	V_O = 0	–75		–250	mA
I_{CC}	V_{CC} = 5.25 V,	Outputs open		80	115	mA

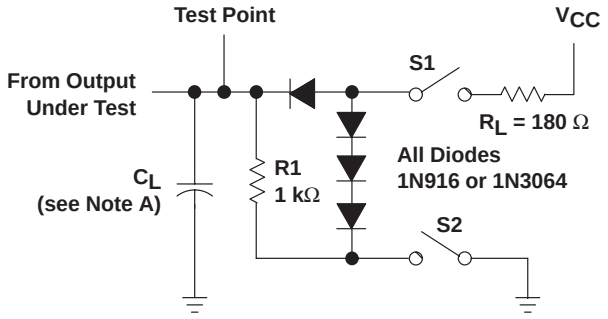
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = MIN to MAX§, T_A = MIN to MAX§		UNIT
				SN74ALS29823		
				MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2	10	ns
t_{PHL}				2	10	
t_{PLH}	CLK	Any Q	C_L = 300 pF		16	ns
t_{PHL}					16	
t_{PHL}	$\overline{CLR}$	Any Q	C_L = 50 pF		12	ns
t_{PZH}	$\overline{OE}$	Any Q	C_L = 50 pF		14	ns
t_{PZL}					14	
t_{PZH}	$\overline{OE}$	Any Q	C_L = 300 pF		20	ns
t_{PZL}					23	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 50 pF		14	ns
t_{PLZ}					12	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 5 pF		9	ns
t_{PLZ}					9	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

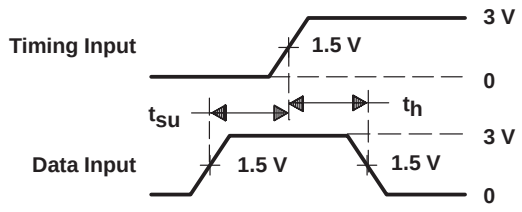
PARAMETER MEASUREMENT INFORMATION



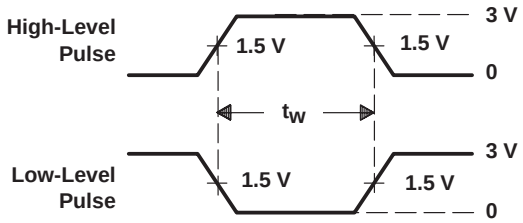
LOAD CIRCUIT

SWITCH POSITION TABLE

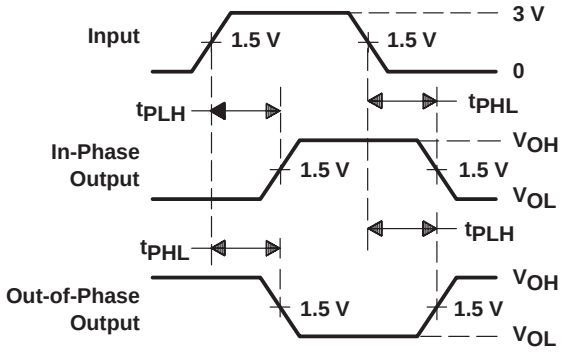
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



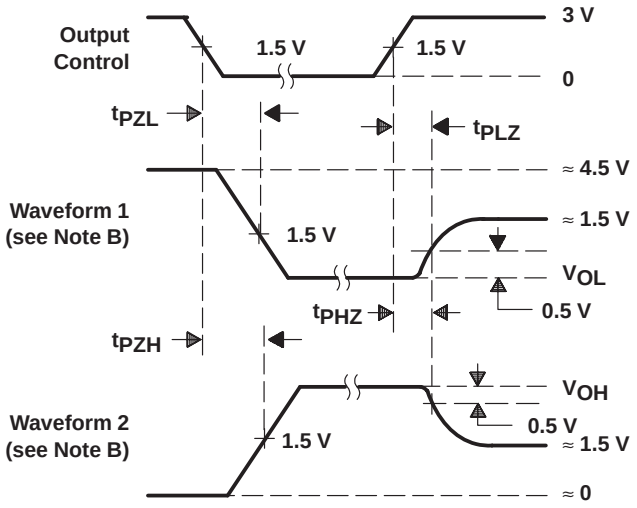
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS29823DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74ALS29823DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70		
SN74ALS29823NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS29823, SN74ALS29823 :

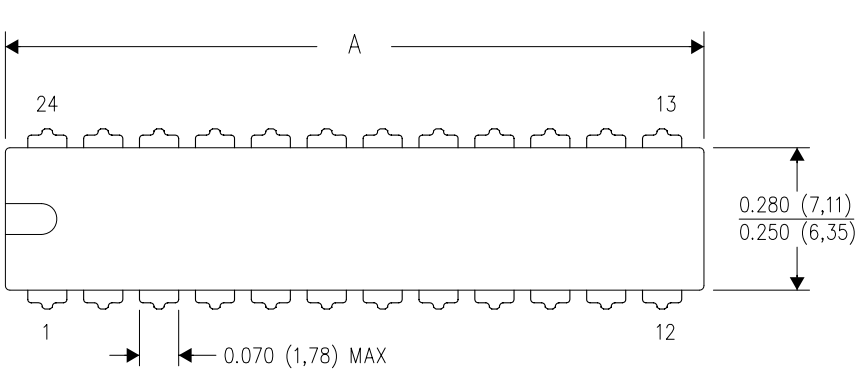
- Catalog: SN74ALS29823
- Military: SN54ALS29823

NOTE: Qualified Version Definitions:

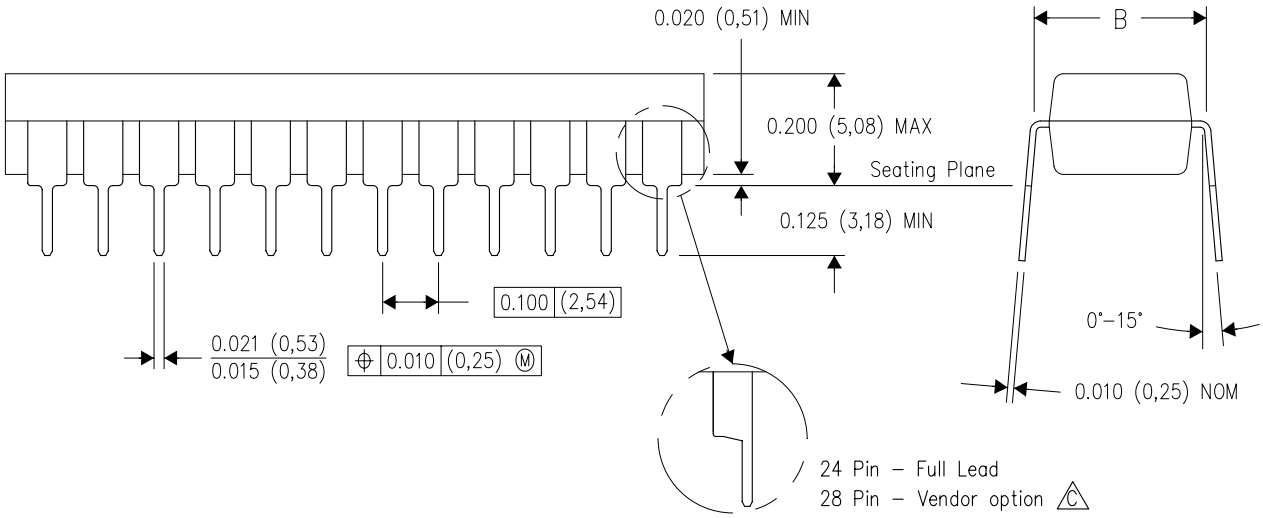
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

24 PINS SHOWN



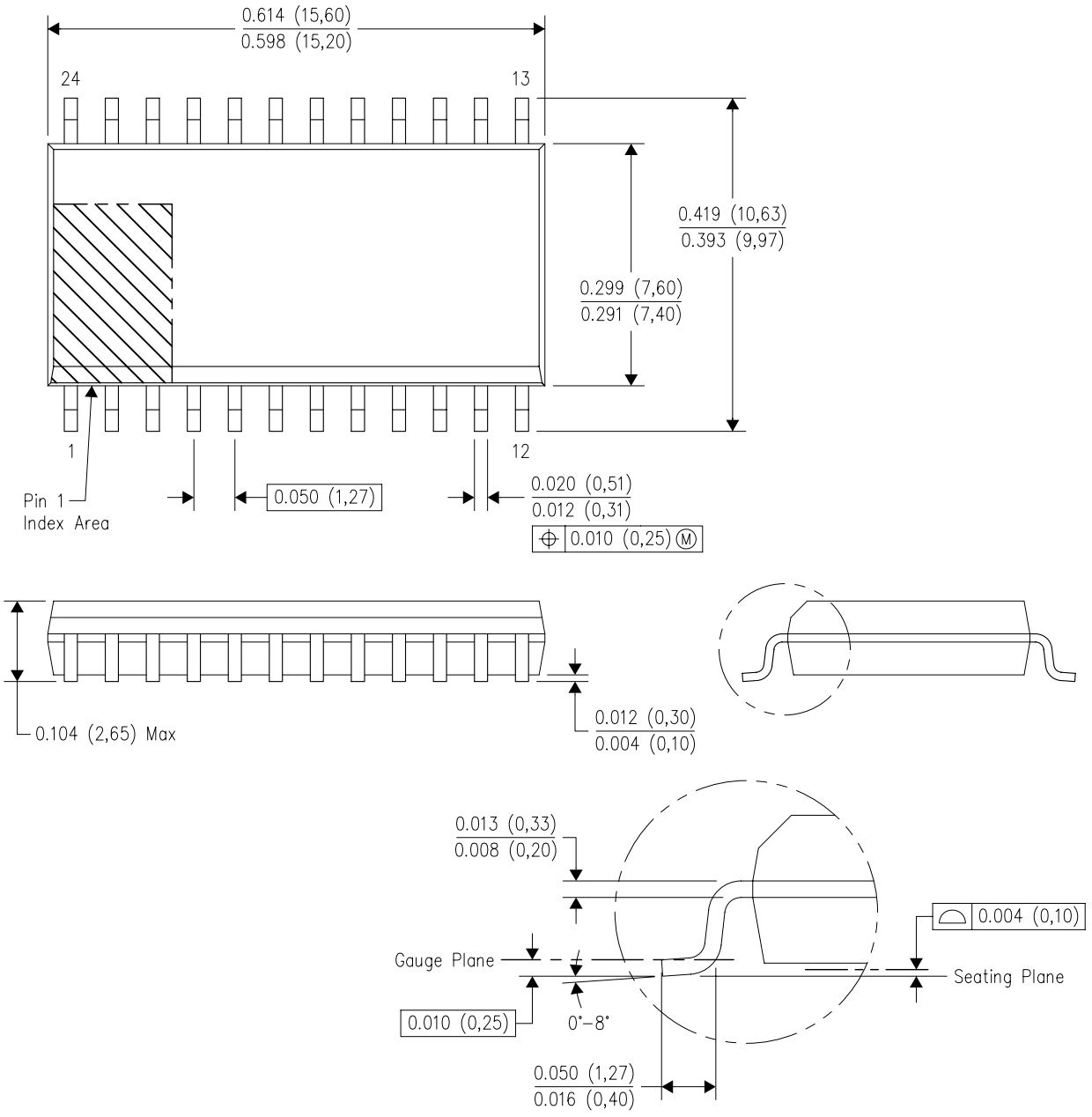
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/C 04/09

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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