

GENERAL DESCRIPTION

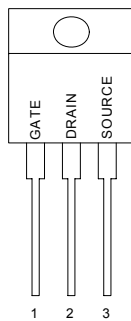
This Power MOSFET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

FEATURES

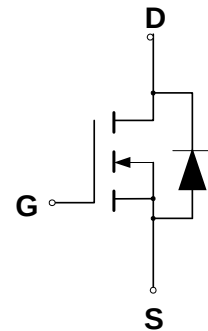
- ◆ Higher Current Rating
- ◆ Lower $r_{DS(ON)}$, Lower Capacitances
- ◆ Lower Total Gate Charge
- ◆ Tighter VSD Specifications
- ◆ Avalanche Energy Specified

PIN CONFIGURATION

TO-220/TO-220FP
Top View



SYMBOL



N-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT05N50N220	TO-220
CMT05N50N220FP	TO-220FP

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current — Continuous	I_D	5.0	A
— Pulsed (Note 1)	I_{DM}	18	
Gate-to-Source Voltage — Continue	V_{GS}	± 20	V
Total Power Dissipation	P_D	96	W
Derate above 25°C		0.77	W/°C
Single Pulse Avalanche Energy (Note 2)	E_{AS}	125	mJ
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Thermal Resistance — Junction to Case	θ_{JC}	1.70	°C/W
— Junction to Ambient	θ_{JA}	62	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_J = 25^\circ\text{C}$.

Characteristic		Symbol	CMT05N50			Units
			Min	Typ	Max	
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$)		$V_{(BR)DSS}$	500			V
Drain-Source Leakage Current ($V_{DS} = 500\text{V}$, $V_{GS} = 0\text{ V}$)		I_{DSS}			25	μA
Gate-Source Leakage Current-Forward ($V_{gsf} = 20\text{ V}$, $V_{DS} = 0\text{ V}$)		I_{GSSF}			100	nA
Gate-Source Leakage Current-Reverse ($V_{gsr} = -20\text{ V}$, $V_{DS} = 0\text{ V}$)		I_{GSSR}			-100	nA
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$)		$V_{GS(th)}$	2.0		4.0	V
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ V}$, $I_D = 2.7\text{A}$) (Note 4)		$R_{DS(on)}$			1.5	Ω
Forward Transconductance ($V_{DS} = 15\text{V}$, $I_D = 2.5\text{ A}$) (Note 4)		g_{FS}	2.8			mhos
Input Capacitance	$(V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$)	C_{iss}		520	730	pF
Output Capacitance		C_{oss}		170	240	pF
Reverse Transfer Capacitance		C_{rss}		11	20	pF
Turn-On Delay Time	$(V_{DD} = 250\text{ V}$, $I_D = 5\text{ A}$, $R_G = 9.1\Omega$, $V_{GS} = 10\text{ V}$) (Note 4)	$t_{d(on)}$		7.0	10	ns
Rise Time		t_r		9.0	20	ns
Turn-Off Delay Time		$t_{d(off)}$		20	40	ns
Fall Time		t_f		10	20	ns
Total Gate Charge	$(V_{DS} = 400\text{V}$, $I_D = 5\text{ A}$, $V_{GS} = 10\text{ V}$) (Note 4)	Q_g		10		nC
Gate-Source Charge		Q_{gs}		2		nC
Gate-Drain Charge		Q_{gd}		3		nC
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)		L_D		4.5		nH
Internal Drain Inductance (Measured from the source lead 0.25" from package to source bond pad)		L_S		7.5		nH
SOURCE-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Charge	$I_F = 5\text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	Q_{rr}		1.8		μC
Forward Turn-On Time		t_{on}		**		
Reverse Recovery Time		t_{rr}		415		ns
Diode Forward Voltage	$I_S = 5\text{ A}$, $V_{GS} = 0\text{ V}$	V_{SD}			1.5	V

Note

- (1) Repetitive rating; pulse width limited by max. junction temperature
 - (2) $V_{DD} = 100\text{V}$, $V_{GS} = 10\text{V}$, $L = 10\text{mH}$, $I_{AS} = 5\text{A}$, $R_G = 25\Omega$
 - (3) $I_{SD} \leq 4.5\text{A}$, $di/dt \leq 75\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ** Negligible, Dominated by circuit inductance

TYPICAL ELECTRICAL CHARACTERISTICS

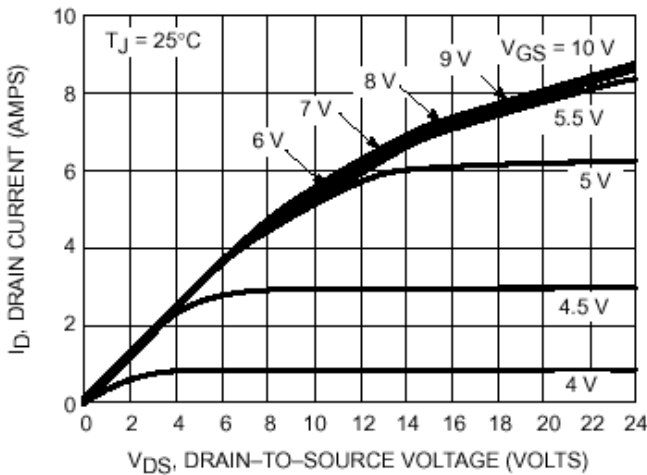


Figure 1. On-Region Characteristics

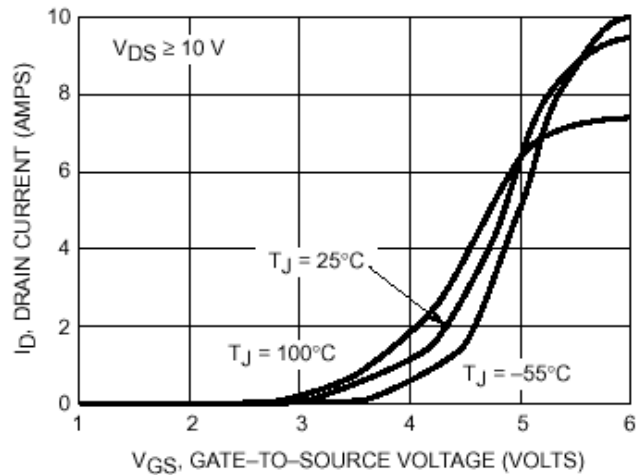


Figure 2. Transfer Characteristics

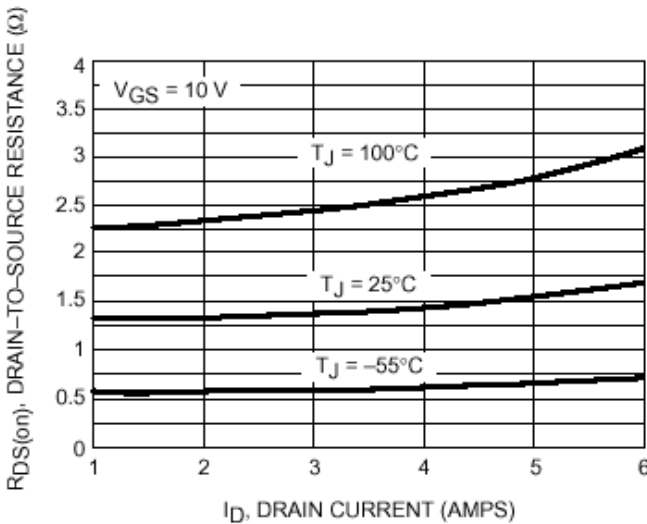


Figure 3. On-Resistance versus Drain Current and Temperature

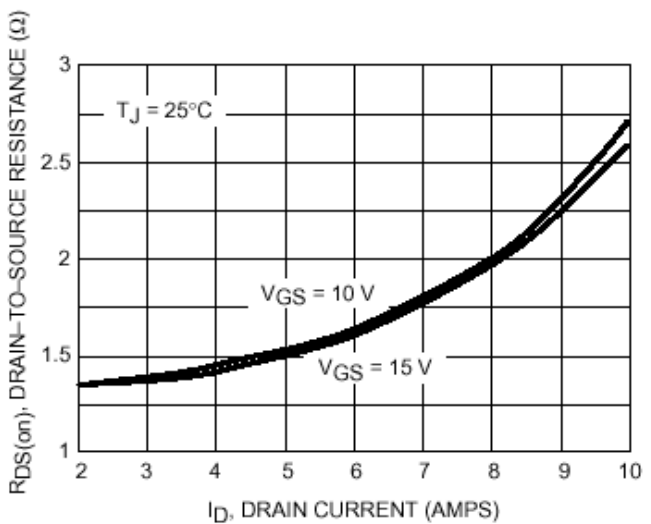


Figure 4. On-Resistance versus Drain Current and Gate Voltage

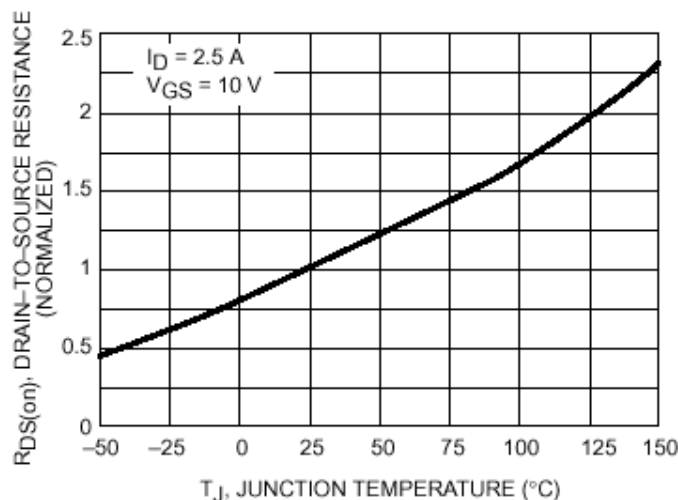


Figure 5. On-Resistance Variation with Temperature

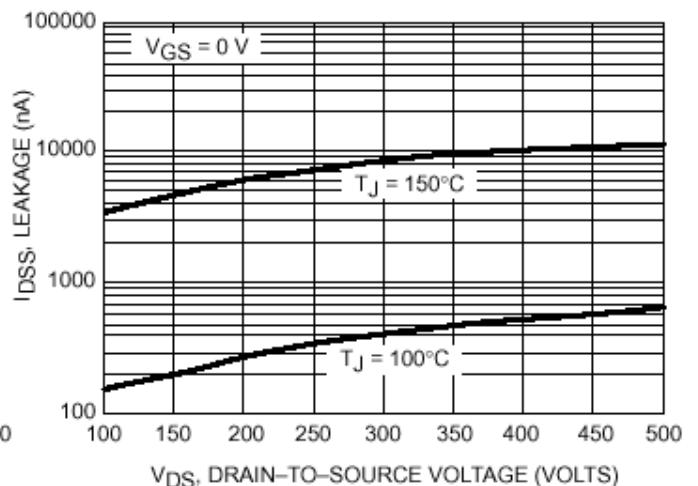
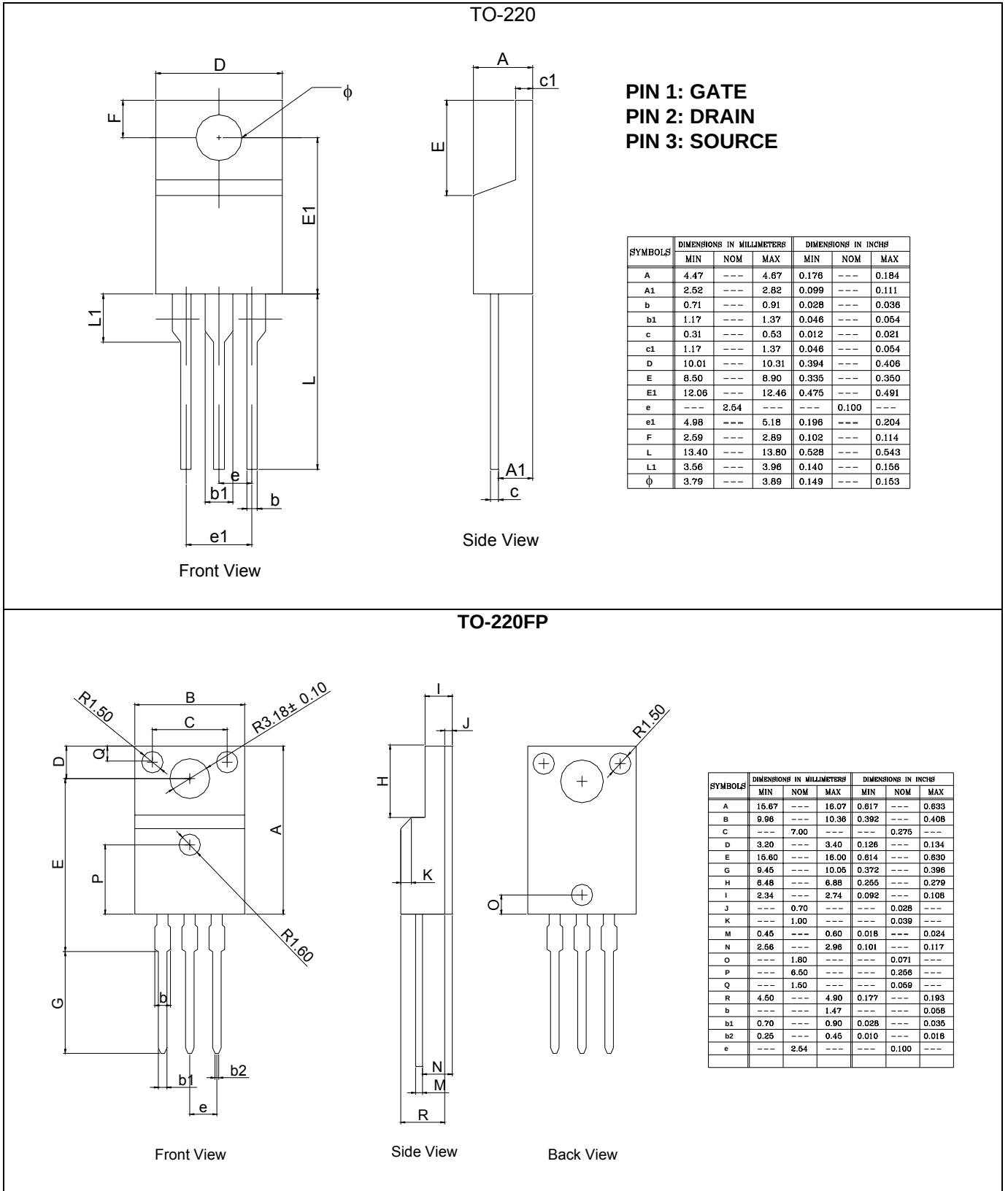


Figure 6. Drain-to-Source Leakage Current versus Voltage

PACKAGE DIMENSION



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