LF156JAN

LF156JAN JFET Input Operational Amplifiers



Literature Number: SNOSAQ0

National Semiconductor

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LF156JAN
JFET Input Operational Amplifiers

General Description

This is the first monolithic JFET input operational amplifier to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). This amplifier features low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The device is also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/*f* noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: $0.01\ pA/\sqrt{Hz}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

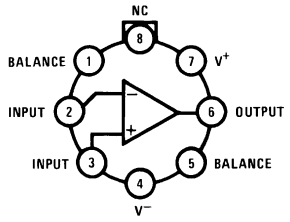
- Extremely fast settling time to 0.01%: 1.5µs
- Fast slew rate: 12V/µs
- Wide gain bandwidth: 5MHz
- Low input noise voltage: $12\ nV/\sqrt{Hz}$

Ordering Information

NS PART NUMBER	SMD PART NUMBER	NS PACKAGE NUMBER	PACKAGE DISCRIPTION
JL156BGA	JM38510/11402	H08C	8LD Metal Can
JL156SGA	JM38510/11402	H08C	8LD Metal Can

Connection Diagrams

Metal Can Package (H)



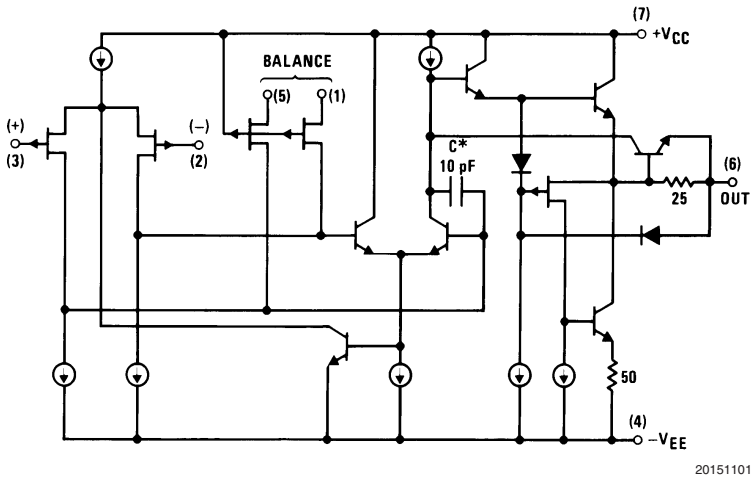
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Top View
See NS Package Number H08C

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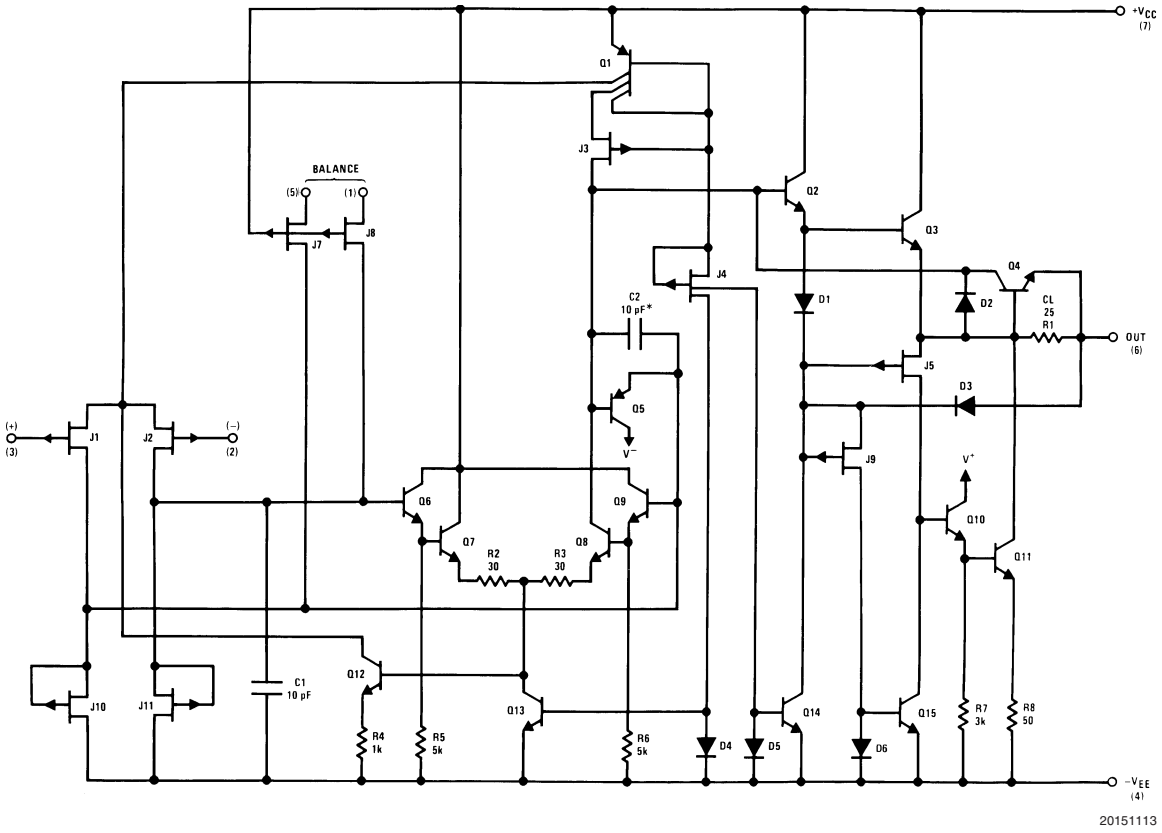
Simplified Schematic



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*3pF in LF357 series.

Detailed Schematic



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*C = 3pF in LF357 series.

Absolute Maximum Ratings (Note 1)

Supply Voltage	±22V
Differential Input Voltage	±40V
Input Voltage Range (Note 3)	±20V
Output Short Circuit Duration (Note 4)	Continuous
T_{JMAX}	175˚C
Power Dissipation at T_A = 25˚C (Note 2)	
Still Air	560 mW
500 LF/Min Air Flow	1200 mW
Thermal Resistance	
θ_{JA}	
Still Air	160˚C/W
400 LF/Min Air Flow	65˚C/W
θ_{JC}	23˚C/W
Storage Temperature Range	−65˚C ≤ T_A ≤ +150˚C
Lead Temperature (Soldering 10 sec.)	300˚C
ESD tolerance (Note 5)	1200V

Recommended Operating Conditions

Supply voltage range	±5 to ±20 V_{DC}
Ambient temperature range	−55˚C ≤ T_A ≤ +125˚C

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25

LF156 Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified.

DC: V_{CC} = ±20V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	+V_{CC} = 15V, -V_{CC} = -15V			7.0	mA	1
					6.0	mA	2
					11	mA	3
V_{IO}	Input Offset Voltage	+V_{CC} = 5V, -V_{CC} = -35V, V_{CM} = 15V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 35V, -V_{CC} = -5V, V_{CM} = -15V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
				-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 5V, -V_{CC} = -5V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
±I_{IB}	Input Bias Current	+V_{CC} = 5V, -V_{CC} = -35V, V_{CM} = 15V		-0.1	3.5	nA	1
				-10	60	nA	2
		+V_{CC} = 35V, -V_{CC} = -5V, V_{CM} = -15V		-0.1	0.1	nA	1
				-10	50	nA	2
				-0.1	0.1	nA	1
				-10	50	nA	2
		+V_{CC} = 5V, -V_{CC} = -25V, V_{CM} = 10V		-0.1	0.3	nA	1
				-10	50	nA	2
I_{IO}	Input Offset Current			-0.02	0.02	nA	1
				-20	+20	nA	2
+PSRR	Power Supply Rejection Ratio	+V_{CC} = 10V, -V_{CC} = -20V		85		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+V_{CC} = 20V, -V_{CC} = -10V		85		dB	1, 2, 3
CMR	Input Voltage Common Mode Rejection	V_{CM} = -15V to 15V		85		dB	1, 2, 3
$V_{IO\ Adj}$(+)	Adjustment for Input Offset Voltage			8.0		mV	1, 2, 3
$V_{IO\ Adj}$(-)	Adjustment for Input Offset Voltage				-8.0	mV	1, 2, 3
+I_{OS}	Output Short Circuit Current (For Positive Output)	+V_{CC} = 15V, -V_{CC} = -15V, t ≤ 25mS		-50		mA	1, 2, 3
-I_{OS}	Output Short Circuit Current (For Negative Output)	+V_{CC} = 15V, -V_{CC} = -15V, t ≤ 25mS			50	mA	1, 2, 3
Δ V_{IO}/ΔT	Temperature Coefficient of Input Offset Voltage	25˚C ≤ T_A ≤ +125˚C	(Note 7)	-30	30	µV/˚C	2
		-55˚C ≤ T_A ≤ 25˚C	(Note 7)	-30	30	µV/˚C	3
-A_{VS}	Open Loop Voltage Gain (Single Ended)	V_O = -15V, R_L = 2KΩ	(Note 6)	50		V/mV	4
			(Note 6)	25		V/mV	5, 6
+A_{VS}	Open Loop Voltage Gain (Single Ended)	V_O = +15V, R_L = 2KΩ	(Note 6)	50		V/mV	4
			(Note 6)	25		V/mV	5, 6
A_{VS}	Open Loop Voltage Gain (Single Ended)	V_{CC} = ±5V, V_O = ±2V, R_L = 2KΩ	(Note 6)	10		V/mV	4, 5, 6
-V_{OP}	Output Voltage Swing	V_{CM} = 20V, R_L = 10KΩ			-16	V	4, 5, 6
		V_{CM} = 20V, R_L = 2KΩ			-15	V	4, 5, 6
+V_{OP}	Output Voltage Swing	V_{CM} = -20V, R_L = 10KΩ		16		V	4, 5, 6
		V_{CM} = -20V, R_L = 2KΩ		15		V	4, 5, 6

LF156 Electrical Characteristics (Continued)

AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
-SR	Slew Rate Fall	V_I = 5V to -5V, A_V = 1		7.5		V/µS	7
				5		V/µS	8A, 8B
+SR	Slew Rate Rise	V_I = -5V to 5V, A_V = 1		7.5		V/µS	7
				5		V/µS	8A, 8B
TR_{TR}	Transient Response Rise Time	R_L = 2KΩ, C_L= 100pF, V_I = 50mV, A_V = 1			100	nS	7, 8A, 8B
TR_{OS}	Transient Response Overshoot	R_L = 2KΩ, C_L = 100pF, V_I = 50mV, A_V = 1			40	%	7, 8A, 8B
NI_{BB}	Noise Broad Band	BW = 5KHz, V_{CC} = ±20V			10	μV_{RMS}	7
NI_{PC}	Noise Popcorn	BW = 5KHz, V_{CC} = ±20V			40	μV_{PK}	7
tS (+)	Settling Time	A_V = -1			1500	nS	12
tS (-)	Settling Time	A_V = -1			1500	nS	12

Drift Values

The following conditions apply, unless otherwise specified.

AC: V_{CC} = ±20V, V_{CM} = 0V

Delta calculations performed on JAN S devices at group B, subgroup 5 only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current			-0.05	0.05	nA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate condition for which the device is functional, but do not guarantee specific performance limits . For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}(maximum junction temperature), θ_{JA}(package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_D=(T_{Jmax}-T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Short circuit may be to ground or either supply. Rating applies to +125˚C case temperature or +75˚C ambient temperature.

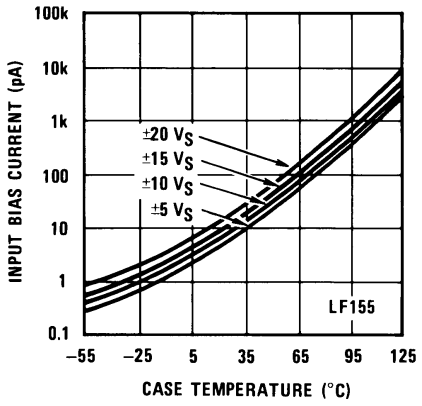
Note 5: Human body model, 100pF discharged through 1.5KΩ.

Note 6: Datalog Reading in K = V/mV.

Note 7: Calculated parameter.

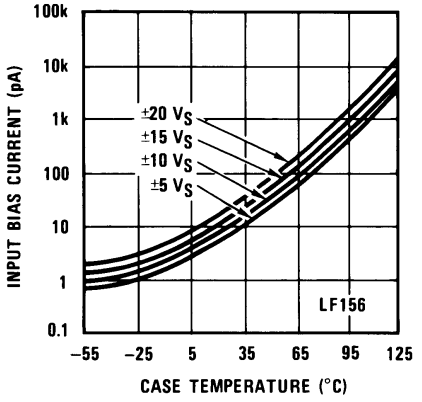
Typical DC Performance Characteristics

Input Bias Current



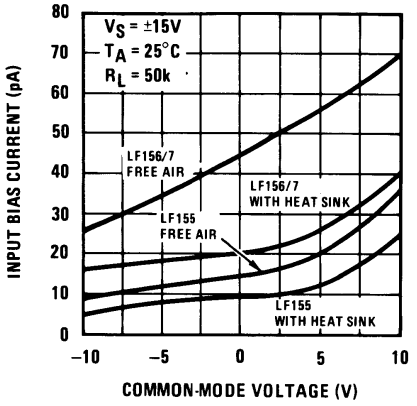
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Input Bias Current



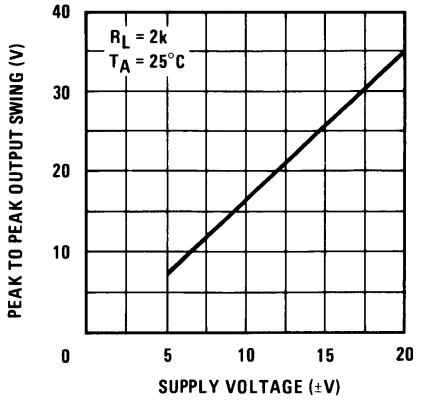
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Input Bias Current



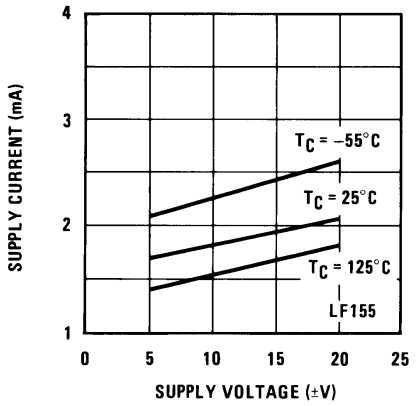
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Voltage Swing



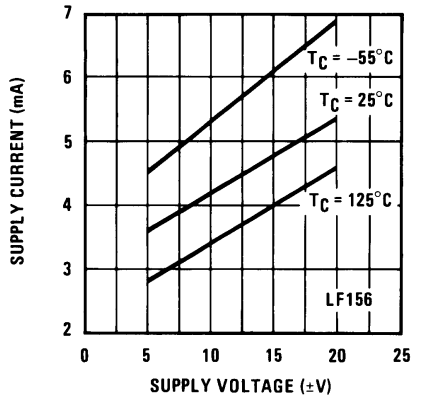
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Supply Current



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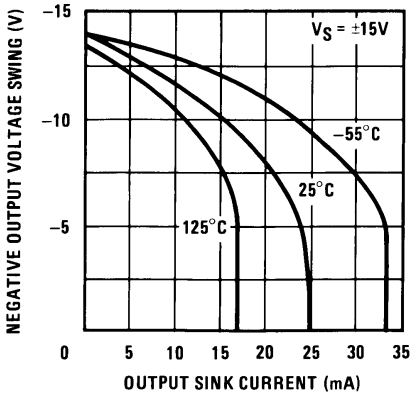
Supply Current



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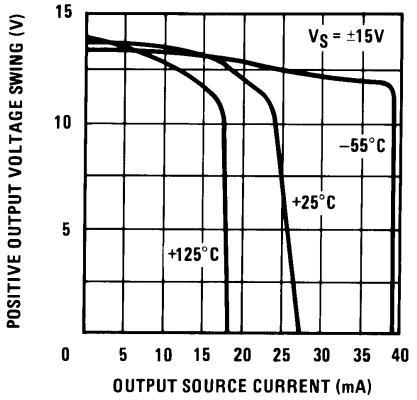
Typical DC Performance Characteristics (Continued)

Negative Current Limit



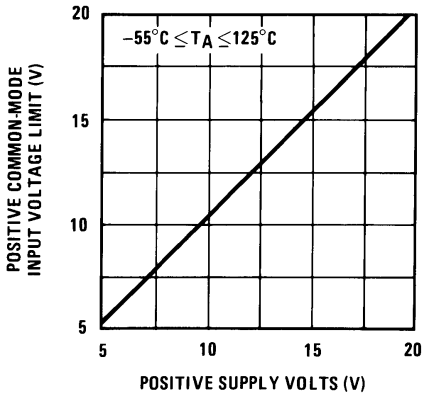
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Positive Current Limit



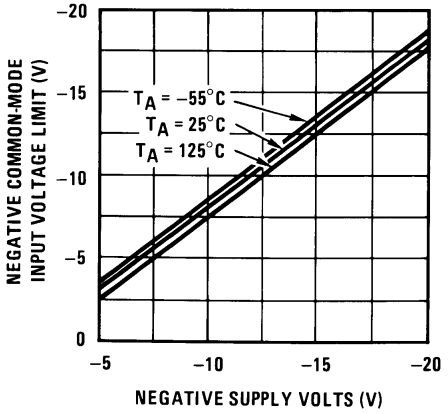
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Positive Common-Mode Input Voltage Limit



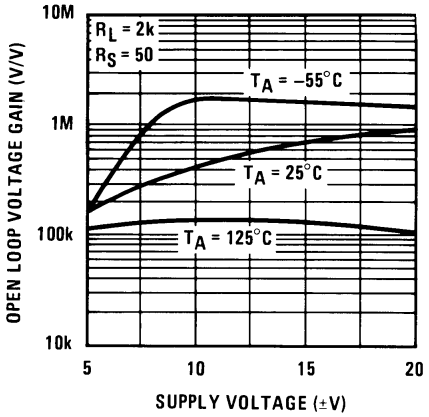
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Negative Common-Mode Input Voltage Limit



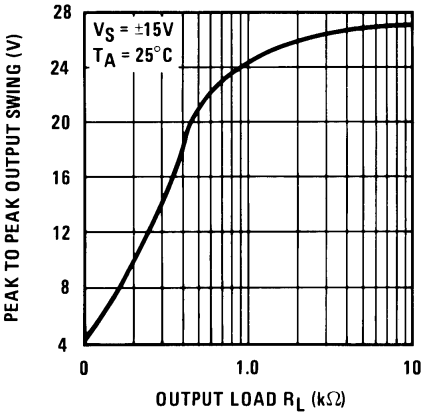
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Open Loop Voltage Gain



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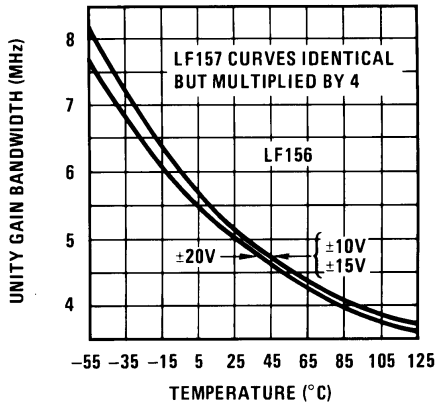
Output Voltage Swing



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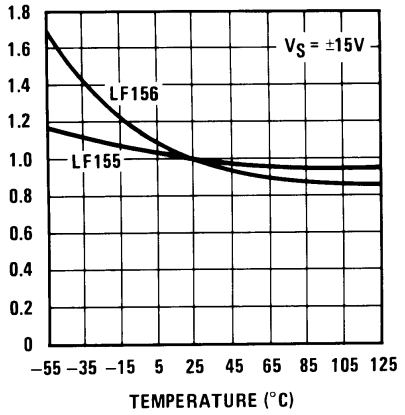
Typical AC Performance Characteristics

Gain Bandwidth



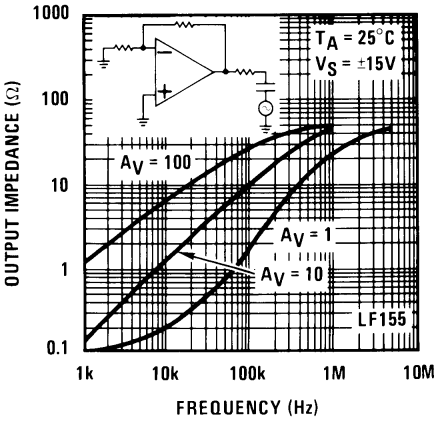
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Normalized Slew Rate



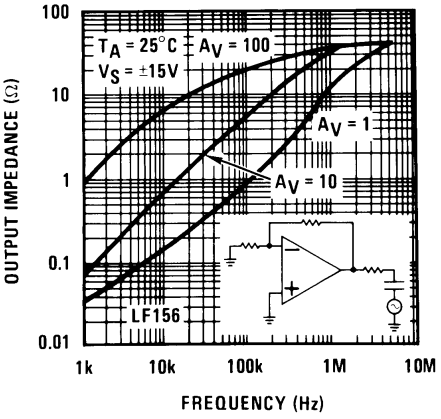
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Output Impedance



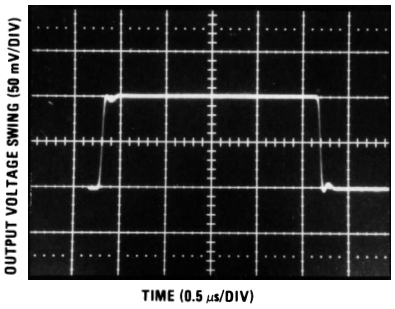
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Output Impedance



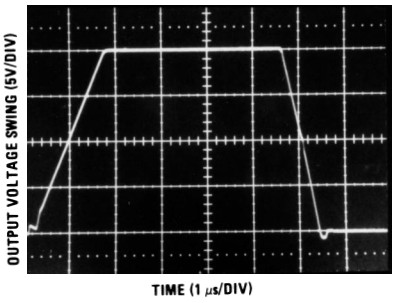
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LF156 Small Signal Pulse Response, A_V = +1



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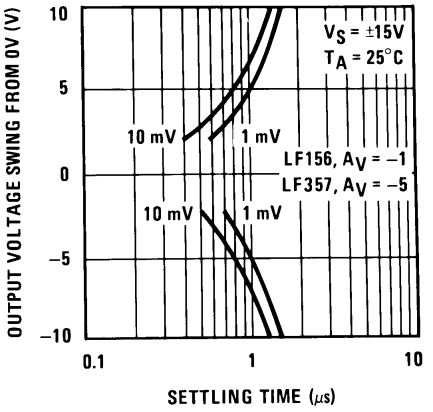
LF156 Large Signal Puls Response, A_V = +1



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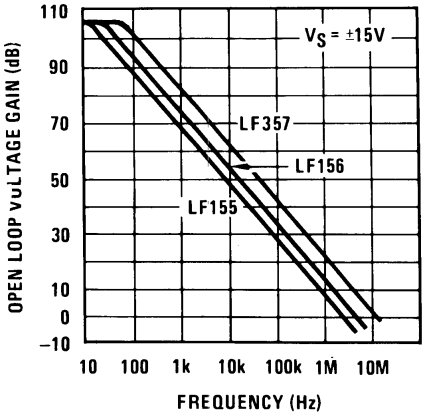
Typical AC Performance Characteristics (Continued)

Inverter Settling Time



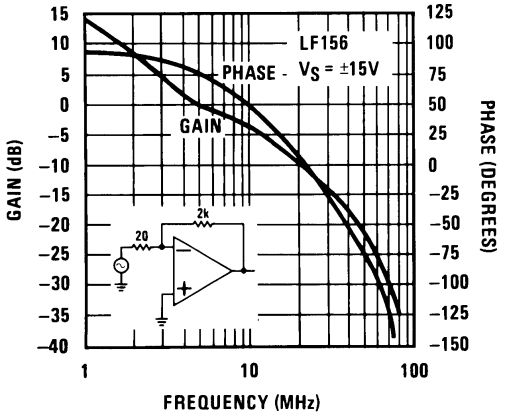
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Open Loop Frequency Response



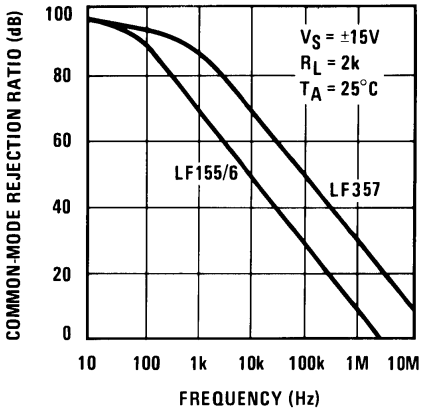
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Bode Plot



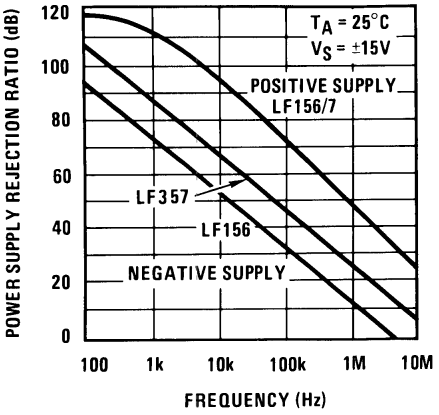
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Common-Mode Rejection Ratio



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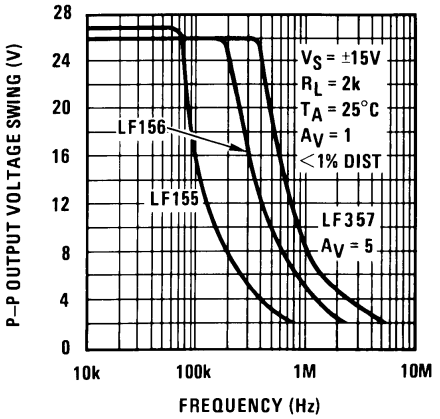
Power Supply Rejection Ratio



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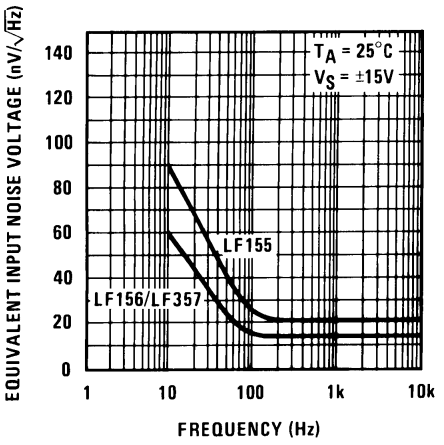
Typical AC Performance Characteristics (Continued)

Undistorted Output Voltage Swing



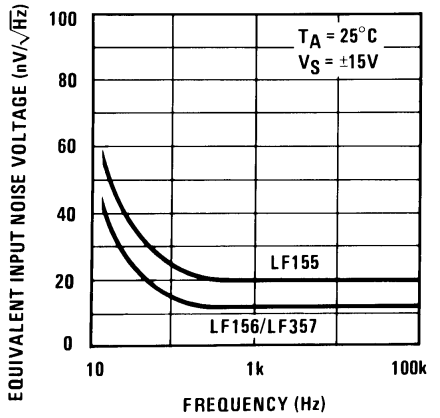
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Equivalent Input Noise Voltage



20151165

Equivalent Input Noise Voltage (Expanded Scale)



20151166

Application Hints

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

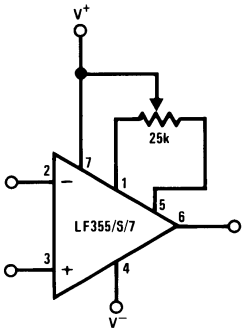
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Circuit Connections

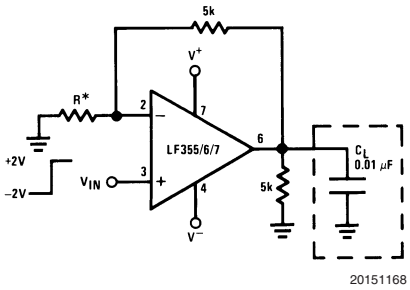
V_{OS} Adjustment



20151167

- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/˚C or less the additional drift with adjust is ≈ 0.5µV/˚C/mV of adjustment
- Typical overall drift: 5µV/˚C ±(0.5µV/˚C/mV of adj.)

Driving Capacitive Loads



20151168

* LF156 R = 5k

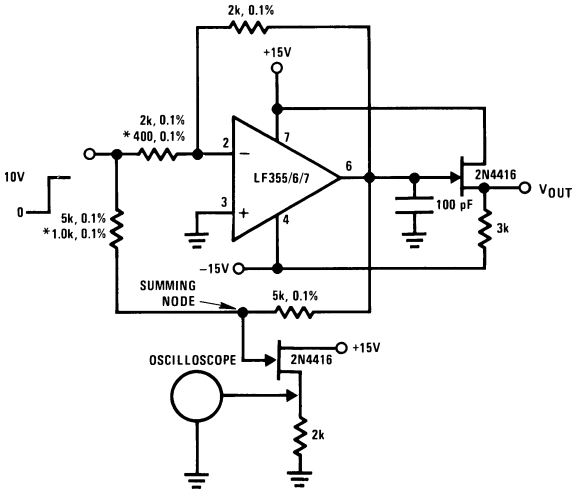
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \simeq 0.01\mu F$.

Overshoot ≤ 20%

Settling time (t_s) ≃ 5µs

Typical Applications

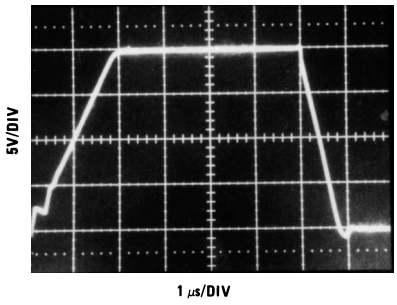
Settling Time Test Circuit



20151116

- Settling time is tested with the LF156 connected as unity gain inverter.
- FET used to isolate the probe capacitance
- Output = 10V step

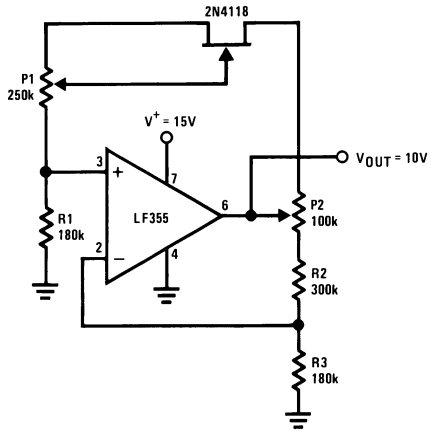
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)
LF356



20151118

Typical Applications (Continued)

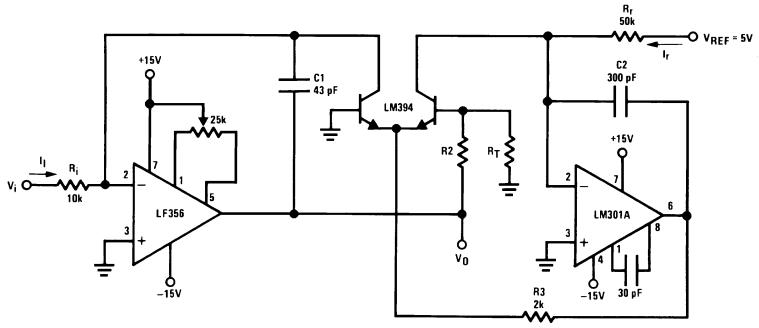
Low Drift Adjustable Voltage Reference



20151120

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust

Fast Logarithmic Converter



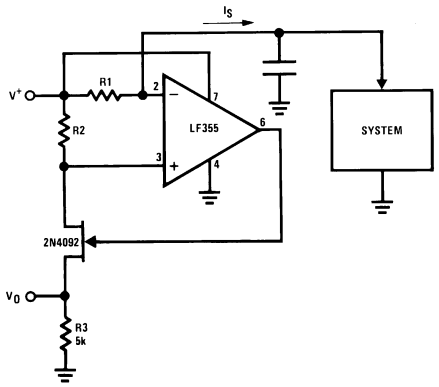
20151121

- Dynamic range: $100\mu A \leq I_i \leq 1mA$ (5 decades), $|V_O| = 1V$/decade
- Transient response: 3µs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\ Ri}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/^{\circ}C \text{ (for temperature compensation)}$$

Typical Applications (Continued)

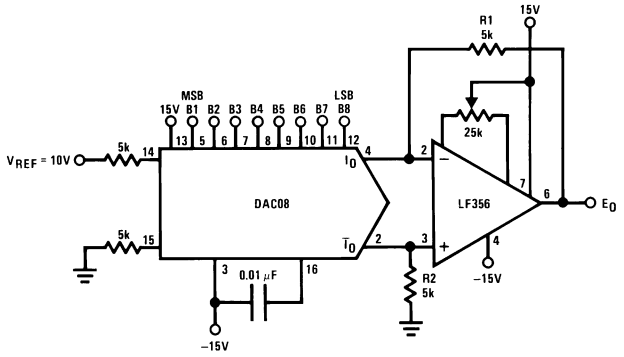
Precision Current Monitor



20151131

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors

8-Bit D/A Converter with Symmetrical Offset Binary Operation



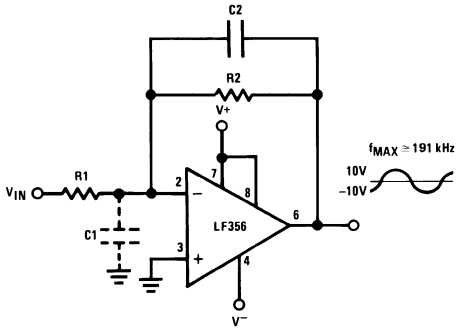
20151132

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier

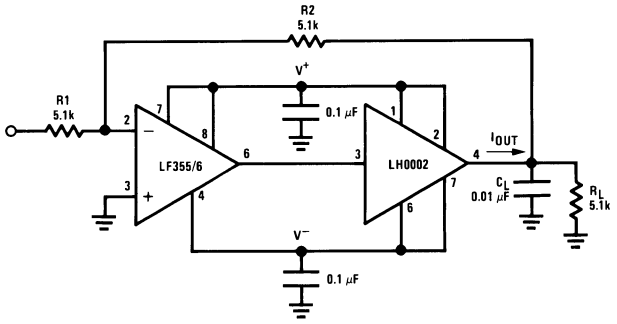


20151170

- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191\,kHz$

- Parasitic input capacitance C1 ≃ 3pF interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

Boosting the LF156 with a Current Amplifier



20151173

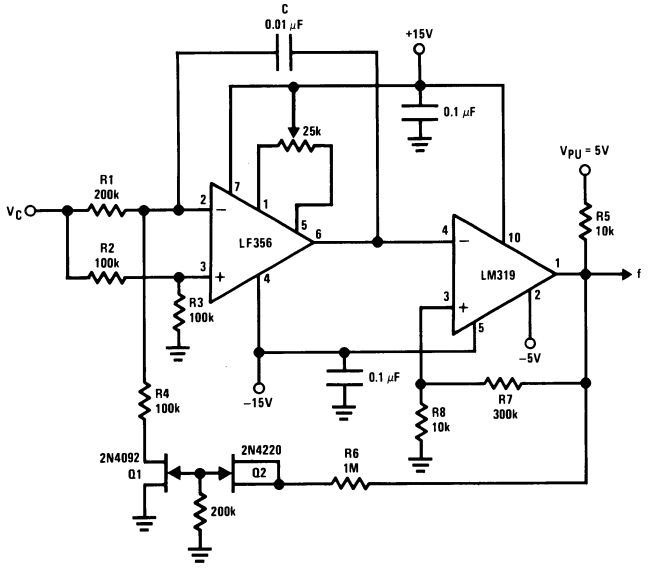
- $I_{OUT(MAX)} \simeq 150mA$ (will drive $R_L \geq 100\Omega$)
-

- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}\ V/\mu s$ (with C_L shown)

- No additional phase shift added by the current amplifier

Typical Applications (Continued)

3 Decades VCO

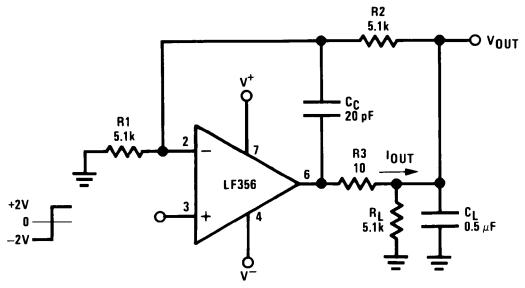


20151124

$$f = \frac{V_C\,(R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \leq V_C \leq 30V,\ 10\,Hz \leq f \leq 10\,kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

Isolating Large Capacitive Loads



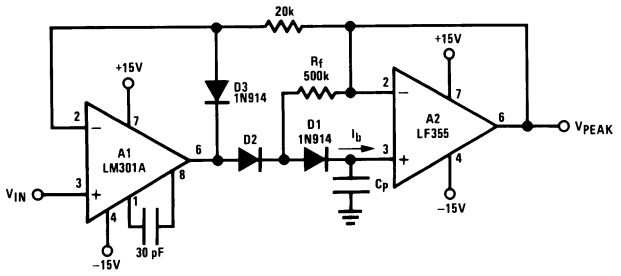
20151122

- Overshoot 6%
- t_s 10µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s\ (\text{with } C_L \text{ shown})$$

Typical Applications (Continued)

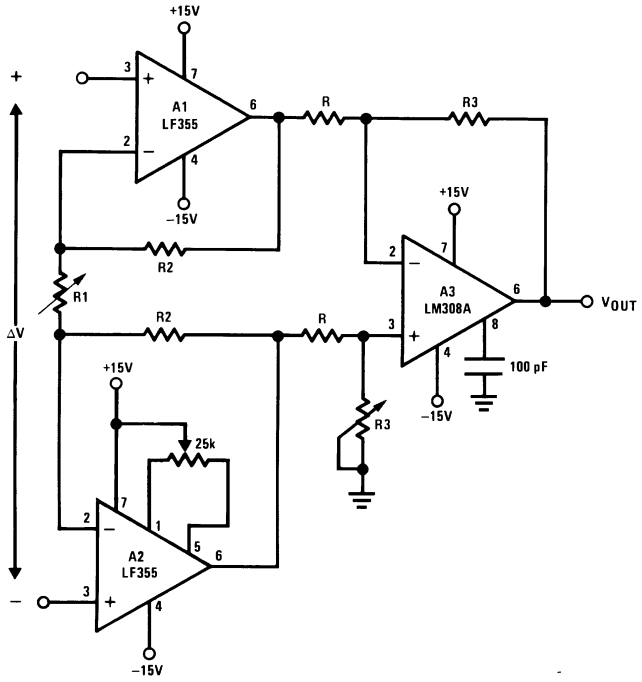
Low Drift Peak Detector



20151123

- By adding D1 and R_f, V_{D1}=0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN}-V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << $\frac{1}{2}\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

High Impedance, Low Drift Instrumentation Amplifier



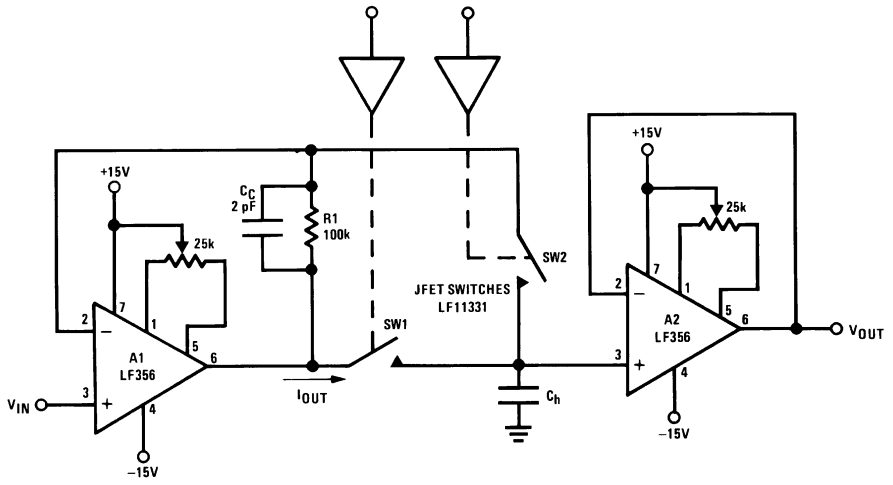
20151126

$$\bullet\ V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V,\ V^- + 2V \leq V_{IN}\ \text{common-mode} \leq V^+$$

- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Typical Applications (Continued)

Fast Sample and Hold



20151133

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON},\ V_{IN},\ C_h}{S_r}\right] 1/2 \text{ provided that:}$$

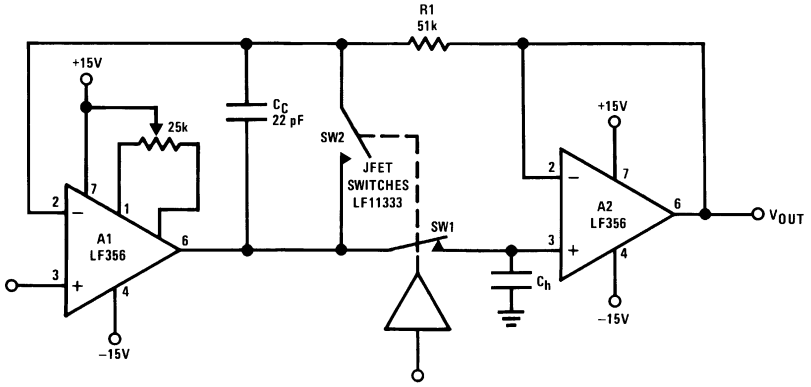
$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}},\ R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

Typical Applications (Continued)

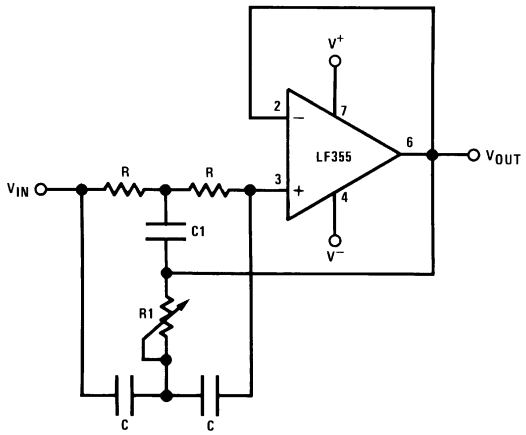
High Accuracy Sample and Hold



20151127

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ■ Fast settling time
  - ■ Low V_{OS}

High Q Notch Filter



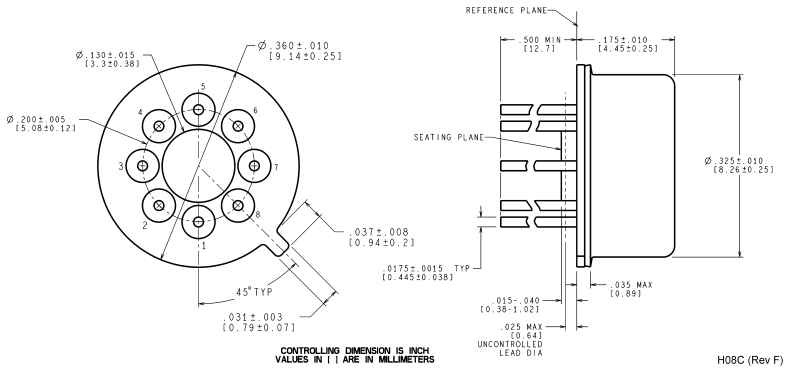
20151134

- 2R1 = R = 10MΩ
  2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = –55 dB, Q > 100
- Use LF155 for
  - ■ Low I_B
  - ■ Low supply current

Revision History

Date Released	Revision	Section	Originator	Changes
03/10/06	A	New Released, Corporate format.	R. Malone	New Release, Corporate format 1 MDS data sheet converted into a Corp. data sheet format. Following MDS data sheet will be Archived MJLF156-X, Rev. 0A0.

Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
NS Package Number H08C

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