ISL91127

High Efficiency Buck-Boost Regulator with 4.5A Switches

FN8418
Rev 4.00
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The ISL91127 is a high-current, buck-boost switching regulator for systems using new battery chemistries. It uses the Renesas proprietary buck-boost algorithm to maintain voltage regulation while providing excellent efficiency and very low output voltage ripple when the input voltage is close to the output voltage.

The ISL91127 can deliver at least 2.1A continuous output current (V_{OUT} = 3.3V) across a battery voltage range of 2.5V to 4.35V. This maximizes the energy utilization of advanced, single-cell Li-ion battery chemistries that have significant capacity left at voltages below the system voltage. Its fully synchronous low ON-resistance 4-switch architecture and a low quiescent current of only 30µA optimize efficiency under all load conditions.

The ISL91127 supports stand-alone applications with a fixed 3.3V or 3.5V output voltage or adjustable output voltage with an external resistor divider. Output voltages as low as 1V or as high as 5.2V are supported.

The ISL91127 is available in a 20 bump, 0.4mm pitch WLCSP (2.15mmx1.74mm) with a 2.5MHz switching frequency, which further reduces the size of external components.

Related Literature

For a full list of related documents, visit our website

- ISL91127 product page

Features

- Accepts input voltages above or below regulated output voltage
- Automatic and seamless transitions between Buck and Boost modes
- Input voltage range: 1.8V to 5.5V
- Continuous output current: up to 2.1A (PVIN = 2.5V, V_{OUT} = 3.3V)
- High efficiency: up to 96%
- 30µA quiescent current maximizes light-load efficiency
- 2.5MHz switching frequency minimizes external component size
- Fully protected for short-circuit, over-temperature, and undervoltage
- Small 2.15mmx1.74mm WLCSP

Applications

- Brownout-free system voltage for smartphones and tablet PCs
- Wireless communication devices
- 2G/3G/4G RF power amplifiers

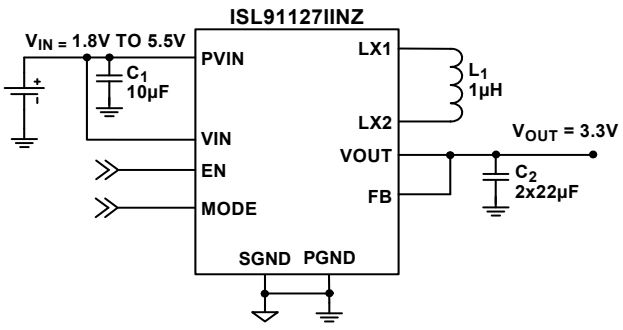


FIGURE 1. TYPICAL APPLICATION: V_{OUT} = 3.3V

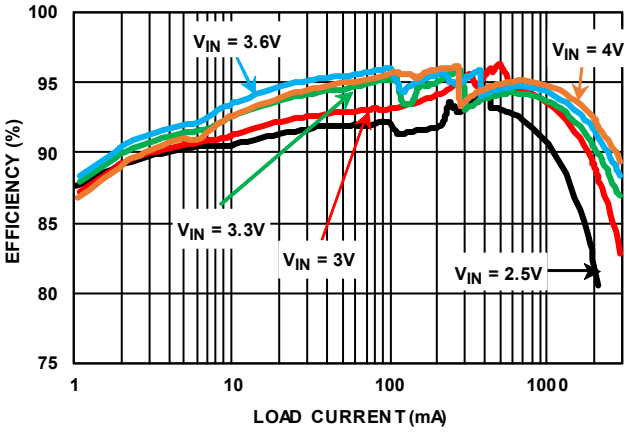


FIGURE 2. EFFICIENCY: V_{OUT} = 3.3V

Block Diagram

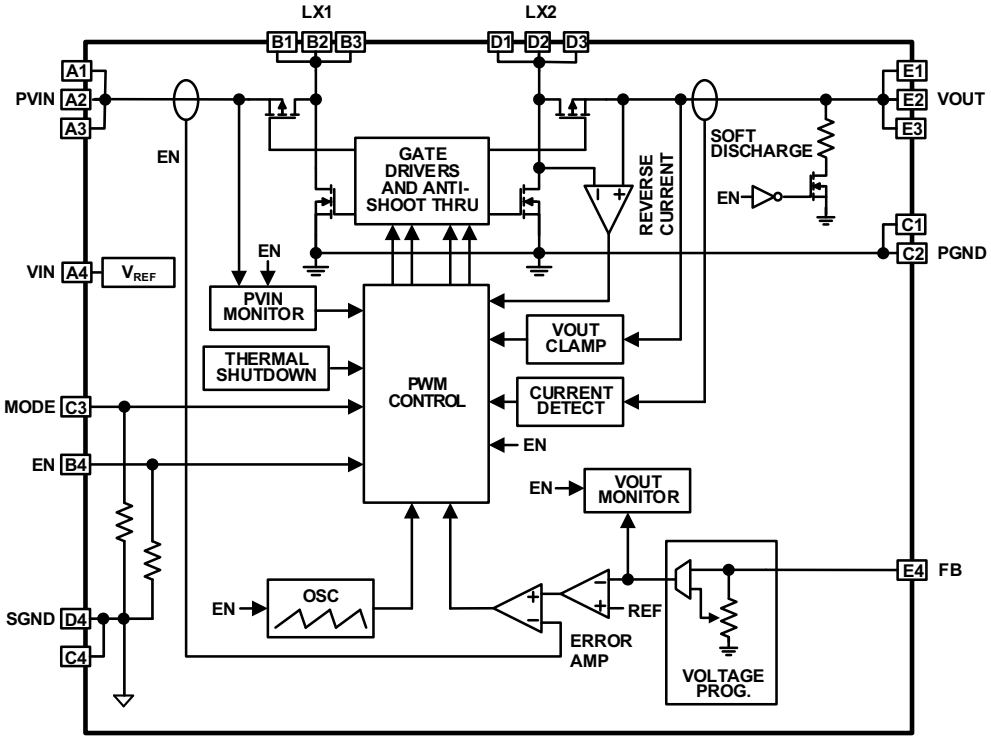
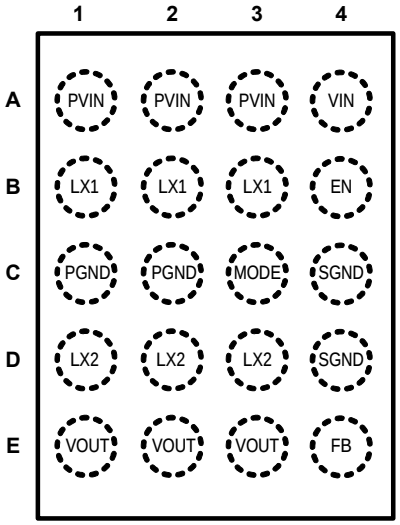


FIGURE 3. BLOCK DIAGRAM

Pin Configuration

ISL91127
(20 BALL WLCSP, 0.4mm PITCH)
TOP VIEW, BUMPS DOWN



Pin Descriptions

PIN #	PIN NAMES	DESCRIPTION
A1, A2, A3	PVIN	Power input. Range: 1.8V to 5.5V. Connect 2x10µF capacitors to PGND.
B1, B2, B3	LX1	Inductor connection, input side
C1, C2	PGND	Power ground for high switching current
D1, D2, D3	LX2	Inductor connection, output side
E1, E2, E3	VOUT	Buck-boost regulator output. Connect 2x22µF capacitors to PGND.
C3	MODE	Logic input, HIGH for auto PFM mode. LOW for forced PWM operation.
A4	VIN	Supply input. Range: 1.8V to 5.5V.
B4	EN	Logic input, drive HIGH to enable device.
C4, D4	SGND	Analog ground pin
E4	FB	Voltage feedback pin

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	OUTPUT VOLTAGE (V)	TEMP RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL91127IINZ-T	GAXU	3.3	-40 to +85	3k	20 Ball WLCSP	W4x5.20M
ISL91127IINZ-T7A	GAXU	3.3	-40 to +85	250	20 Ball WLCSP	W4x5.20M
ISL91127II2AZ-T	GAXV	3.5	-40 to +85	3k	20 Ball WLCSP	W4x5.20M
ISL91127II2AZ-T7A	GAXV	3.5	-40 to +85	250	20 Ball WLCSP	W4x5.20M
ISL91127IIAZ-T	GAXT	ADJ	-40 to +85	3k	20 Ball WLCSP	W4x5.20M
ISL91127IIAZ-T7A	GAXT	ADJ	-40 to +85	250	20 Ball WLCSP	W4x5.20M
ISL91127IIN-EVZ	Evaluation Board for ISL91127IINZ					
ISL91127II2A-EVZ	Evaluation Board for ISL91127II2AZ					
ISL91127IIA-EVZ	Evaluation Board for ISL91127IIAZ					

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL91127 product information page. For more information about MSL, see TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	BUCK-BOOST REGULATION	BYPASS	DYNAMIC VOLTAGE SCALING	I^2C	PACKAGE
ISL91127	Yes	No	No	No	WLCSP
ISL91127IR	Yes	No	No	No	QFN
ISL91128	Yes	Yes	Yes	Yes	WLCSP

NOTE: For the full family of ISL911xx buck-boost regulators, please visit our website.

Absolute Maximum Ratings

PVIN, VIN . . . . . -0.3V to 6.5V
LX1, LX2. . . . . -0.3V to 6.5VDC, -2V to 7V for 10ns
FB (Adjustable Version) . . . . . -0.3V to 2.7V
FB (Fixed V_{OUT} Versions) . . . . . -0.3V to 6.5V
GND, PGND . . . . . -0.3V to 0.3V
All Other Pins . . . . . -0.3V to 6.5V
ESD Rating
Human Body Model (Tested per JS-001-2010). 2.5kV
Machine Model (Tested per JESD22-A115C) 250V
Charged Device Model (Tested per JS-002-2014) 1kV
Latch-Up (Tested per JESD-78D; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JB} (°C/W)
20 Ball WLCSP Package (Notes 4, 5)	72	16

Maximum Junction Temperature . . . . . .+125°C
Storage Temperature Range. . . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range . . . . . 1.8V to 5.5V
Maximum Load Current
V_{IN} = 2.5V V_{OUT} = 3.3V 2.1ADC

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JB}, the board temp is taken on the board near the edge of the package, on a trace at the middle of one side. See TB379.

Analog Specifications

$V_{IN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, $L_1 = 1\mu H$, $C_1 = 2x10\mu F$, $C_2 = 2x22\mu F$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V) unless specified otherwise.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
POWER SUPPLY						
Input Voltage Range	V_{IN}		**1.8**		**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising		1.725	**1.795**	V
		Falling	**1.550**	1.650		V
V_{IN} Supply Current	I_{VIN}	PFM mode, 1.8V ≤ V_{IN} ≤ 5V, no external load on V_{OUT} (Note 8)		30	**55**	µA
V_{IN} Supply Current, Shutdown	I_{SD}	EN = GND, V_{IN} = 3.6V		0.05	**1.00**	µA
OUTPUT VOLTAGE REGULATION						
Output Voltage Range	V_{OUT}	ISL91127IIAZ, I_{OUT} = 100mA, V_{IN} = 3.6V	**1.00**		**5.20**	V
Output Voltage Accuracy		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 0mA, PWM mode	**-2**		**+2**	%
		V_{IN} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM mode	**-3**		**+4**	%
FB Pin Voltage Regulation	V_{FB}	For adjustable output version, V_{IN} = 3.6V	**0.783**	0.800	**0.813**	V
FB Pin Bias Current	I_{FB}	For adjustable output version			**20**	nA
Line Regulation, PWM Mode	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 500mA, V_{IN} steps from 2.8V to 5.5V		2.2		mV/V
Line Regulation, PFM Mode	$\Delta V_{OUT}/\Delta V_I$	I_{OUT} = 100mA, V_{IN} steps from 2.8V to 5.5V		2.7		mV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = 3.7V, I_{OUT} steps from 0A to 1A		0.021		mV/mA
Output Voltage Clamp	V_{CLAMP}	Rising	**5.25**		**5.95**	V
Output Voltage Clamp Hysteresis				400		mV
DC/DC SWITCHING SPECIFICATIONS						
Oscillator Frequency	f_{SW}		**2.10**	2.50	**2.90**	MHz
Minimum On-Time	$t_{ON(MIN)}$			80		ns
LX1 Pin Leakage Current	$I_{PFETLEAK}$	V_{IN} = 3.6V	**-1**		**1**	µA
LX2 Pin Leakage Current	$I_{NFETLEAK}$	V_{IN} = 3.6V	**-1**		**1**	µA

Analog Specifications $V_{IN} = V_{PVIN} = V_{EN} = 3.6V$, $V_{OUT} = 3.3V$, $L_1 = 1\mu H$, $C_1 = 2x10\mu F$, $C_2 = 2x22\mu F$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C and input voltage range (1.8V to 5.5V) unless specified otherwise. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
SOFT-START AND SOFT DISCHARGE						
Soft-Start Time	t_{SS}	Time from when EN signal asserts to when output voltage ramp starts.		1		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Buck mode. $V_{IN} = 4V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		2		ms
		Time from when output voltage ramp starts to when output voltage reaches 95% of its nominal value with device operating in Boost mode. $V_{IN} = 2V$, $V_{OUT} = 3.3V$, $I_O = 200mA$		2		ms
V_{OUT} Soft Discharge ON-Resistance	r_{DISCHG}	$EN < V_{IL}$		120		Ω
POWER MOSFET						
P-Channel MOSFET ON-Resistance	$r_{DS(ON)_P}$	$V_{IN} = 3.6V$, $I_O = 200mA$		28		mΩ
N-Channel MOSFET ON-Resistance	$r_{DS(ON)_N}$	$V_{IN} = 3.6V$, $I_O = 200mA$		26		mΩ
P-Channel MOSFET Peak Current Limit	I_{PK_LMT}	$V_{IN} = 3.6V$	3.8	4.3	5.0	A
PFM/PWM TRANSITION						
Load Current Threshold, PFM to PWM		$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		360		mA
Load Current Threshold, PWM to PFM		$V_{IN} = 3.6V$, $V_{OUT} = 3.3V$		160		mA
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				30		°C
LOGIC INPUTS						
Input Leakage	I_{LEAK}	$V_{IN} = 3.6V$		0.05	**1**	µA
Input HIGH Voltage	V_{IH}	$V_{IN} = 3.6V$	**1.4**			V
Input LOW Voltage	V_{IL}	$V_{IN} = 3.6V$			**0.4**	V

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for $T_A = +25°C$ and $V_{IN} = 3.6V$.
8. Quiescent current measurements are taken when the output is not switching.

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L_1 = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A.

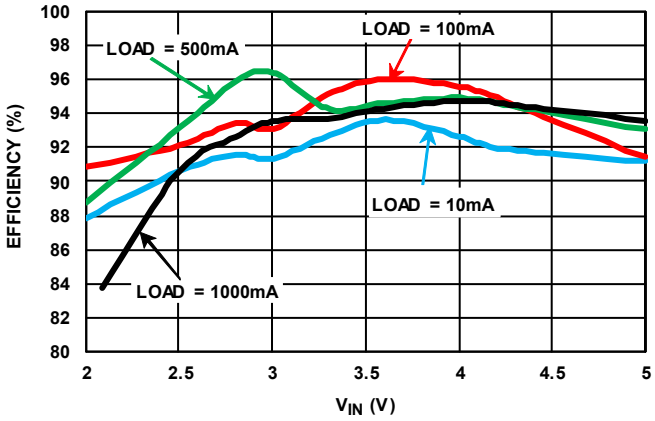


FIGURE 4. EFFICIENCY vs INPUT VOLTAGE

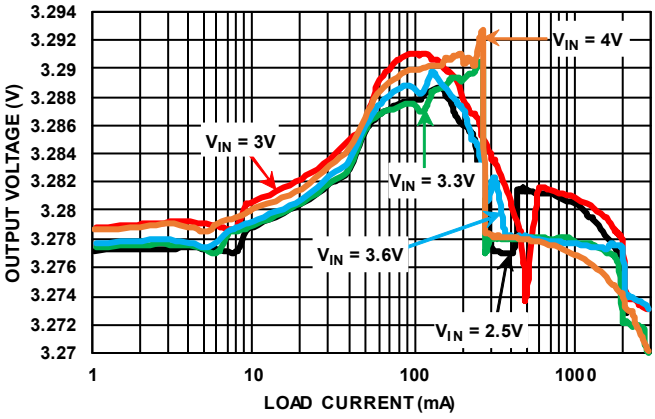


FIGURE 5. OUTPUT VOLTAGE vs LOAD CURRENT

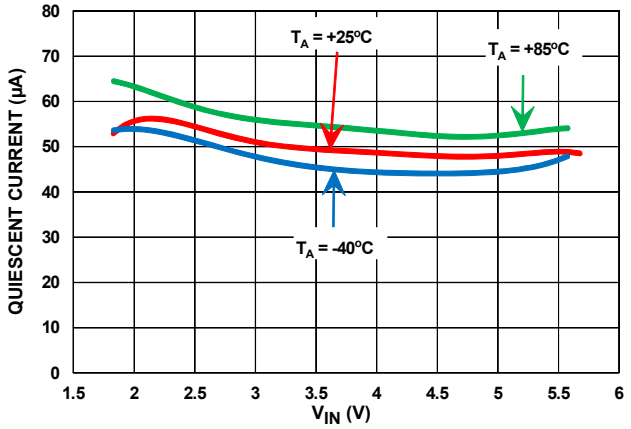


FIGURE 6. QUIESCENT CURRENT vs INPUT VOLTAGE (V_{OUT} = 3.3V, MODE = HIGH)

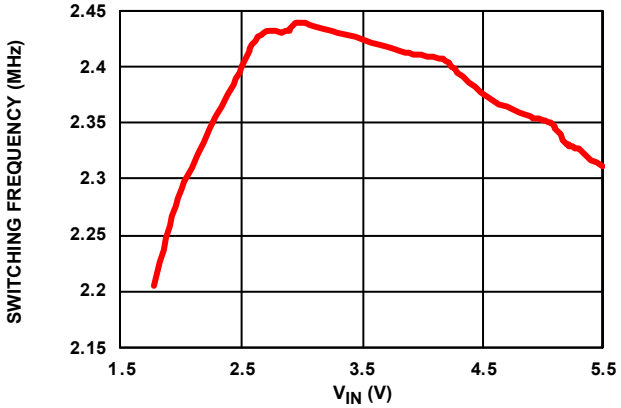


FIGURE 7. SWITCHING FREQUENCY vs INPUT VOLTAGE

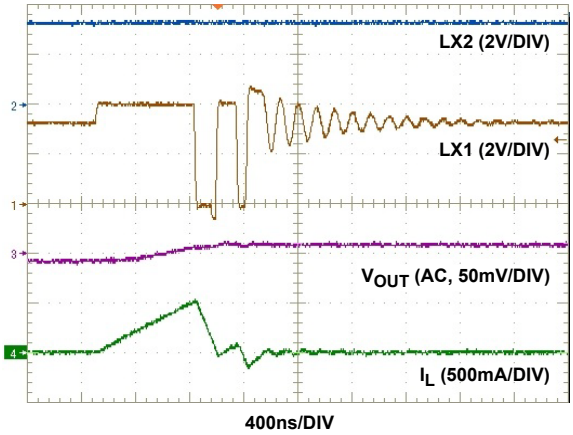


FIGURE 8. STEADY-STATE OPERATION IN PFM (V_{IN} = 4V, V_{OUT} = 3.3V, NO LOAD)

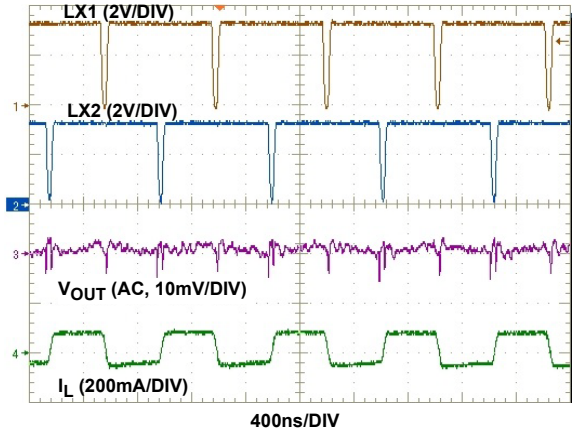


FIGURE 9. STEADY-STATE OPERATION IN PWM (V_{IN} = 3.3V, V_{OUT} = 3.3V, NO LOAD)

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L_1 = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A. **(Continued)**

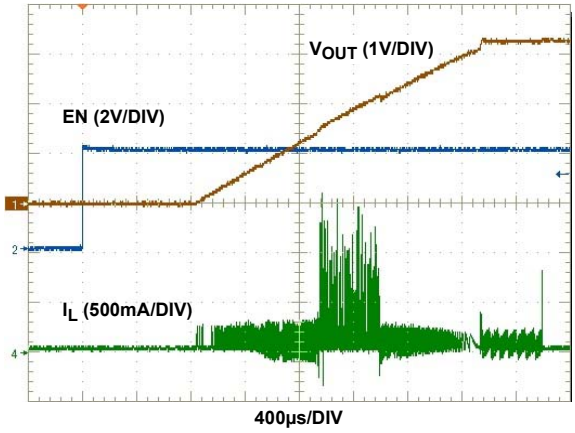


FIGURE 10. SOFT-START (V_{IN} = 3.6V, V_{OUT} = 3.3V, NO LOAD)

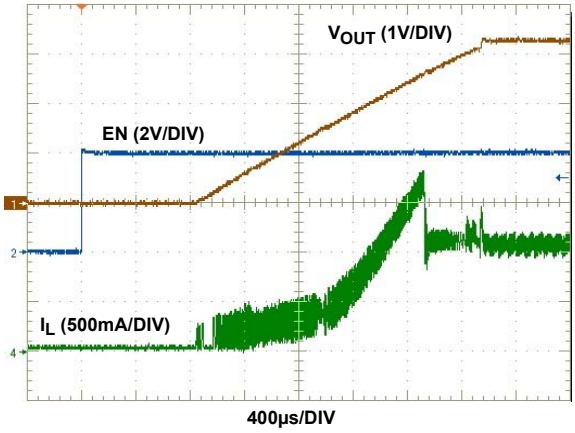


FIGURE 11. SOFT-START (V_{IN} = 3.6V, V_{OUT} = 3.3V, 1A LOAD)

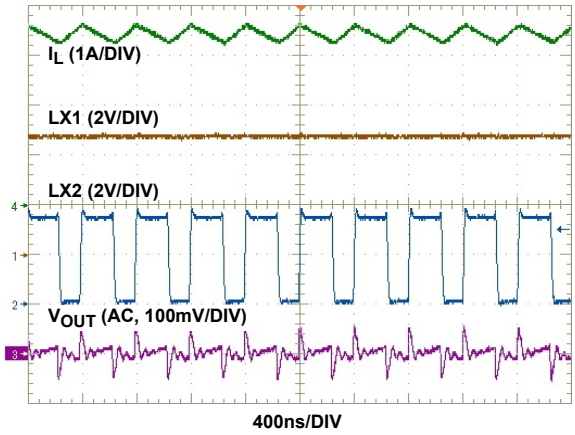


FIGURE 12. STEADY-STATE OPERATION (V_{IN} = 2.5V, V_{OUT} = 3.3V, 2A LOAD)

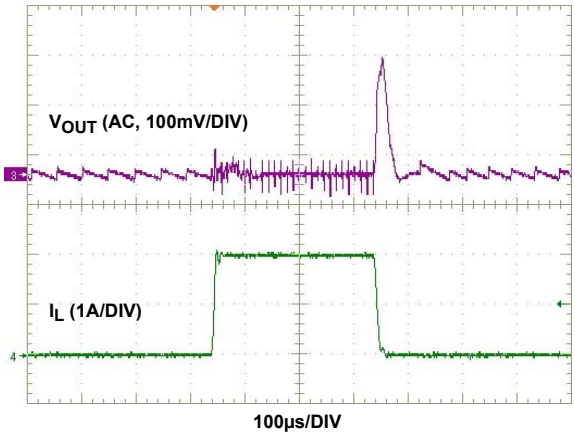


FIGURE 13. 0A TO 2A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

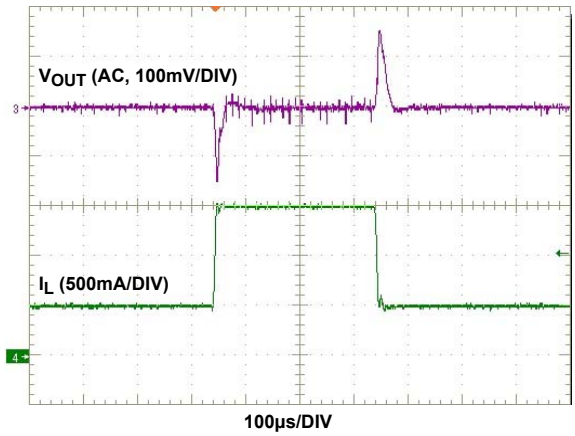


FIGURE 14. 0.5A TO 1.5A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

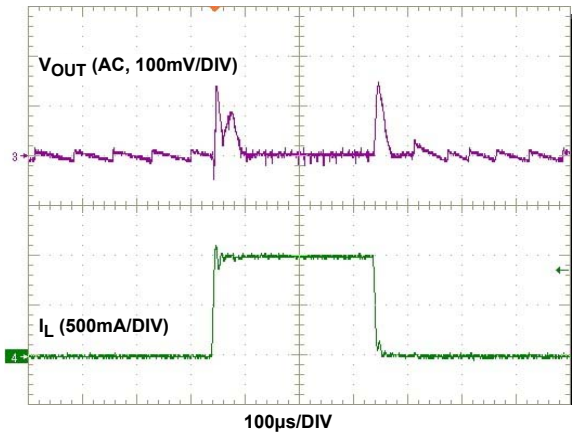


FIGURE 15. 0A TO 1A LOAD TRANSIENT (V_{IN} = 3.6V, V_{OUT} = 3.3V)

Typical Performance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = EN = 3.6V, L_1 = 1µH, C_1 = 2x10µF, C_2 = 2x22µF, V_{OUT} = 3.3V, I_{OUT} = 0A to 3A. **(Continued)**

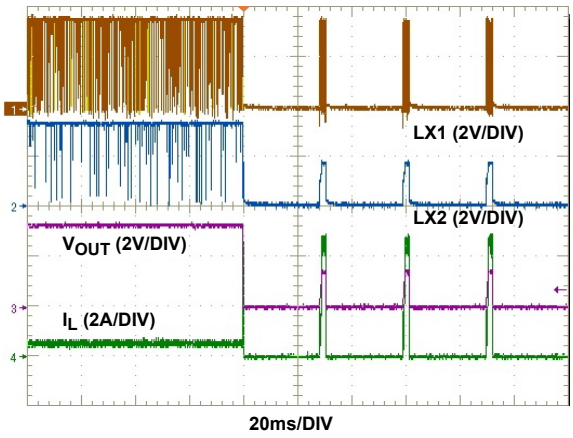


FIGURE 16. OUTPUT SHORT-CIRCUIT BEHAVIOR (V_{IN} = 3.6V, V_{OUT} = 3.3V)

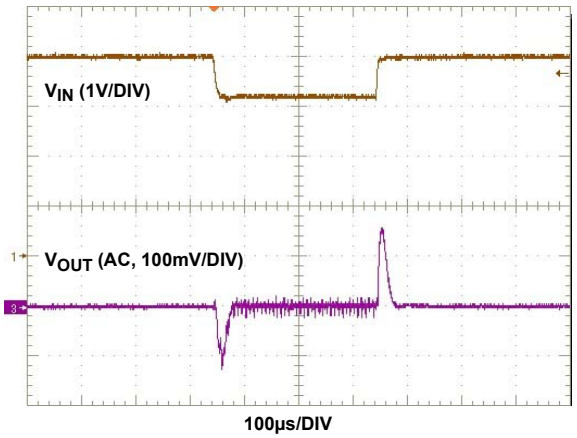


FIGURE 17. 4V TO 3.2V LINE TRANSIENT (V_{OUT} = 3.3V, LOAD = 1A)

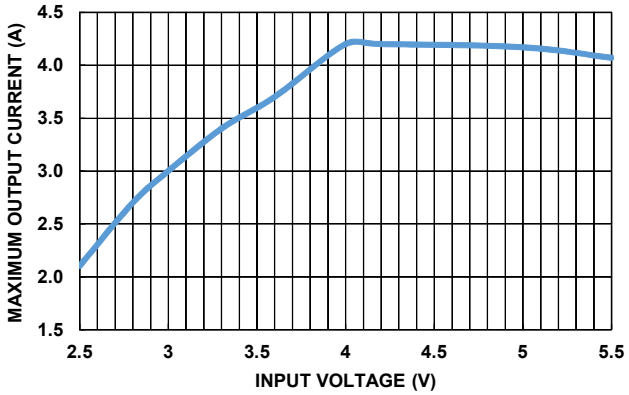


FIGURE 18. OUTPUT CURRENT CAPABILITY: V_{OUT} = 3.3V, T_A = +25°C

Functional Description

Functional Overview

The ISL91127 implements a complete buck-boost switching regulator with PWM controller, internal switches, references, protection circuitry, and control inputs. Refer to the "Block Diagram" on page 2

The PWM controller automatically switches between Buck and Boost modes as necessary to maintain a steady output voltage with changing input voltages and dynamic external loads.

Internal Supply and References

Referring to the "Block Diagram", the ISL91127 provides three PVIN power input pins. The PVIN pins supply input power to the DC/DC converter. An additional VIN pin provides an operating voltage source required for stable V_{REF} generation. Separate ground pins (PGND and SGND) are provided to avoid problems caused by ground shift due to the high switching currents.

Enable Input

Enable the device by asserting the EN pin HIGH. Driving EN LOW invokes a power-down mode, in which most internal device functions are disabled.

Soft Discharge

When the device is disabled by driving EN LOW, an internal resistor between VOUT and GND is activated to slowly discharge the output capacitor. This internal resistor has a typical 120Ω resistance.

POR Sequence and Soft-Start

Asserting the EN pin HIGH allows the device to power up. The following events occur during the start-up sequence: The internal voltage reference powers up and stabilizes. The device then starts operating. There is a typical 1ms delay between assertion of the EN pin and the start of the switching regulator soft-start ramp.

The soft-start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping V_{OUT} voltage. While the output voltage is lower than approximately 20% of the target output

voltage, switching frequency is reduced to a fraction of the normal switching frequency to aid in producing low duty cycles necessary to avoid input inrush current spikes. When the output voltage exceeds 20% of the target voltage, the switching frequency is increased to its nominal value.

When the target output voltage is higher than the input voltage, the device transitions from Buck mode to Boost mode during the soft-start sequence. At the time of this transition, the ramp rate of the reference voltage is decreased, such that the output voltage slew rate is decreased. This provides a slower output voltage slew rate.

The V_{OUT} ramp time is not constant for all operating conditions. Soft-start into Boost mode takes longer than soft-start into Buck mode. The total soft-start time into Buck operating mode is typically 2ms, whereas the typical soft-start time into Boost operating mode is typically 3ms. Increasing the load current increases these typical soft-start times.

Short-Circuit Protection

The ISL91127 provides short-circuit protection by monitoring the feedback voltage. When feedback voltage is sensed to be lower than a certain threshold, the PWM oscillator frequency is reduced in order to protect the device from damage. The P-channel MOSFET peak current limit remains active during this state.

Thermal Shutdown

A built-in thermal protection feature protects the ISL91127 if the die temperature reaches +155°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to +125°C (typical), the device will resume normal operation. When exiting thermal shutdown, the ISL91127 will execute its soft-start sequence.

Buck-Boost Conversion Topology

The ISL91127 operates in either Buck or Boost mode. When operating in conditions where PVIN is close to V_{OUT}, the ISL91127 alternates between Buck and Boost modes as necessary to provide a regulated output voltage.

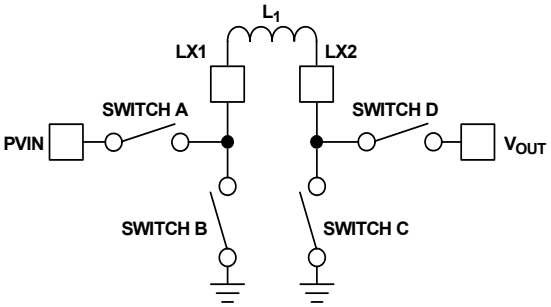


FIGURE 19. BUCK-BOOST TOPOLOGY

Figure 19 shows a simplified diagram of the internal switches and external inductor.

PWM Operation

During PWM operation in Buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate as a synchronous buck converter when in this mode.

During PWM operation in Boost mode, Switch A remains closed and Switch B remains open. Switches C and D operate as a synchronous boost converter when in this mode.

PFM Operation

During PFM operation in Buck mode, Switch D is continuously closed and Switch C is continuously open. Switches A and B operate in discontinuous mode during PFM operation. During PFM operation in Boost mode, the ISL91127 closes Switch A and Switch C to ramp up the current in the inductor. When the inductor current reaches a certain threshold, the device turns off Switches A and C, then turns on Switches B and D. With Switches B and D closed, output voltage increases as the inductor current ramps down.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops, and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.

Operation with V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL91127 rapidly and smoothly switches from Boost to Buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

Output Voltage Programming

The ISL91127 is available in fixed and adjustable output voltage versions. To use the fixed output version, the VOUT pin must be connected directly to FB.

In the adjustable output voltage version (ISL91127IIAZ), an external resistor divider is required to program the output voltage. The FB pin has very low input leakage current, so it is possible to use large value resistors (for example, R_1 = 1MΩ and R_2 = 324kΩ for V_{OUT} = 3.3V) in the resistor divider connected to the FB input.

Applications Information

Component Selection

The fixed-output version of the ISL91127 requires only three external power components to implement the buck-boost converter: an inductor, an input capacitor, and an output capacitor.

The adjustable output version of the ISL91127 requires three additional components to program the output voltage, as shown in Figure 19. Two external resistors program the output voltage and a small capacitor is added to improve stability and response.

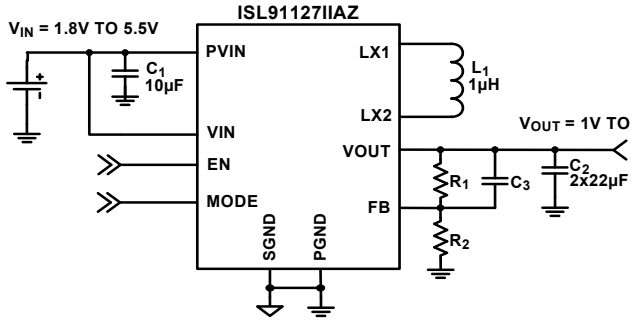


FIGURE 20. ADJUSTABLE OUTPUT APPLICATION

Output Voltage Programming, Adjustable Version

When VREF is connected to GND, select the external resistor values to set and control the output voltage of the ISL91127IIAZ (adjustable output version).

Equation 1 can be used to derive the R_1 and R_2 resistor values:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_1}{R_2}\right) \quad \text{(EQ. 1)}$$

When designing a PCB, include a GND guard band around the feedback resistor network to reduce noise and improve accuracy and stability. Position resistors R_1 and R_2 close to the FB pin.

Feed-Forward Capacitor Selection

A small capacitor (C_3 in Figure 19) in parallel with resistor R_1 is required to provide the specified load and line regulation. The suggested value of this capacitor is 56pF for R_1 = 1MΩ. An NPO type capacitor is recommended.

Inductor Selection

Use an inductor with high frequency core material (for example, ferrite core) to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 1µH inductor with ≥4A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used (refer to Table 3).

PVIN and V_{OUT} Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 10µF. The recommended V_{OUT} capacitor value is 2x22µF.

TABLE 2. CAPACITOR VENDOR INFORMATION

MANUFACTURER	PN	DESCRIPTION
Murata	GRM188R61A226ME15D	22µF, 0603, 10V, X5R
TDK	C1608X5R1A226M080AC	22µF, 0603, 10V, X5R

Recommended PCB Layout

Correct PCB layout is critical for proper operation of the ISL91127. Place the input and output capacitors as close to the IC as possible. The ground connections of the input and output capacitors should be kept as short as possible and should be on the component layer to avoid problems that are caused by high switching currents flowing through PCB vias.

TABLE 3. INDUCTOR VENDOR INFORMATION

MANUFACTURER	MANUFACTURER PART NUMBER	DESCRIPTION	DIMENSION (mm)	WEBSITE
Toko	1277AS-H-1R0M	1µH, 20%, DCR = 34mΩ (typical), I_{SAT} = 4.6A (typical)	3.2x2.5x1.2	www.toko.com
	FDSD0312-H-1R0M	1µH, 20%, DCR = 43mΩ (typical), I_{SAT} = 4.5A (typical)	3.2x3.0x1.2	
Coilcraft	XFL4020-102ME	1µH, 20%, DCR = 11mΩ (typical), I_{SAT} = 5.1A (typical)	4.0x4.0x2.1	www.coilcraft.com

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please visit to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 24, 2018	FN8418.4	Removed About Intersil section. Updated Disclaimer and moved to page 13.
Jan 5, 2017	FN8418.3	Updated Related Literature section on page 1. Updated Table 1 on page 3. - changed “VSEL” column to “Dynamic Voltage Scaling” and made ISL91128 parameter “Yes”. - removed “and DVS” from I2C column.
Aug 9, 2016	FN8418.2	Removed burst current features bullet on page 1. Updated Table 1 on page 3. Removed “V_{IN} = 3.0V V_{OUT} = 3.3V, t_{ON} = 600µs, t = 4.6ms...3A” from the “Recommended Operating Conditions” on page 4.
Jul 15, 2016	FN8418.1	Updated 2 feature bullets to clarify statement. Updated Table 1 on page 3. Updated test conditions for V_{IN} supply current page 4 from “PFM mode, no external load on V_{OUT}” to “PFM mode, 1.8V ≤ V_{IN} ≤ 5V, no external load on”. Updated “P-Channel MOSFET ON-Resistance” typical from 35 to 28 and “N-Channel MOSFET ON-Resistance” typical from 24 to 26 typical. Added Figure 18, “OUTPUT CURRENT CAPABILITY” to typical Performance Curves” on page 8.
Apr 5, 2016	FN8418.0	Initial Release

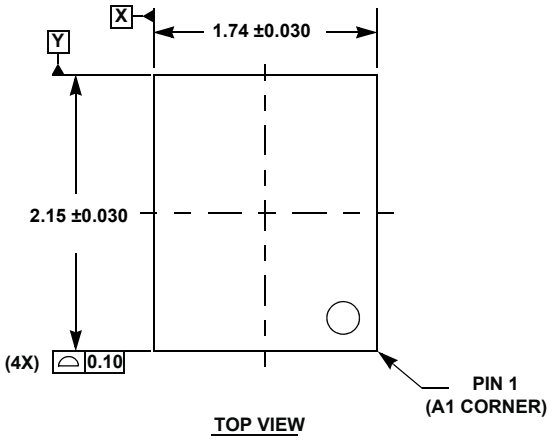
Package Outline Drawing

For the most recent package outline drawing, see W4x5.20M.

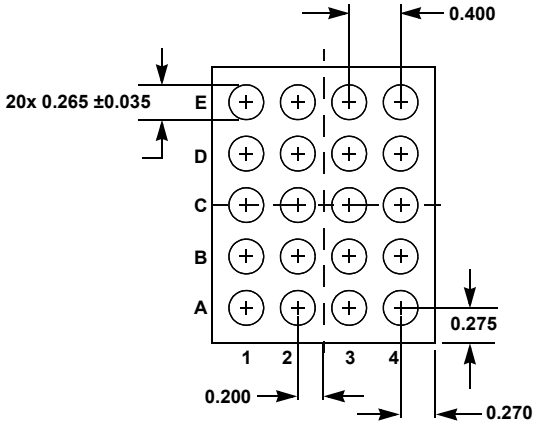
W4x5.20M

20 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP 0.4mm PITCH)

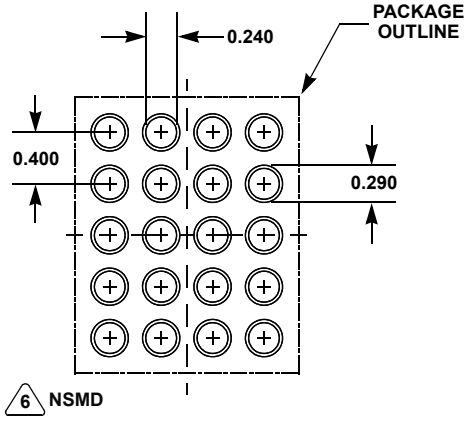
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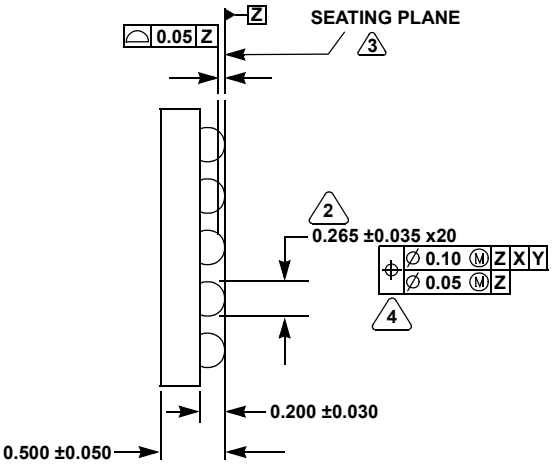
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

NOTES:

1. Dimensions and tolerance per ASMEY 14.5 - 1994.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.
5. All dimensions are in millimeters.
6. NSMD refers to non-solder mask defined pad design per Intersil Techbrief TB451.

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