National Semiconductor

MICROCIRCUIT DATA SHEET

MN54ABT244-X REV 0B0

Original Creation Date: 09/02/94
Last Update Date: 09/24/98
Last Major Revision Date: 03/19/97

OCTAL BUFFER AND LINE DRIVER WITH TRI-STATE OUTPUTS

General Description

The ABT244 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver or bus-oriented transmitter/receiver.

Industry Part Number

54ABT244

Prime Die

NB244

Controlling Document

See Features Page

NS Part Numbers

54ABT244E-QML *
54ABT244E-QMLV**
54ABT244J-QML ***
54ABT244J-QMLV****
54ABT244W-QML *****
54ABT244W-QMLV******

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Non-inverting buffers.
- Output sink capability 48mA, source capability of 24mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- SMD : 5962-9214701Q2A*, V2A**, QRA***, VRA****, QSA*****, VSA******

(Absolute Maximum Ratings)

(Note 1)

Vcc Pin Potential to Ground Potential	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30mA to +5.0mA
Voltage Applies To Any Output	
In the Disabled or Power-Off State	-0.5V to 5.5V
In The High State	-0.5V to Vcc
Current Applies To Output	
In The Low State (Max)	96mA
Junction Temperature (Tj)	
Ceramic	+175C
Thermal Resistance	
Junction-to-Case (Theta JC)	See Mil-Std 1835
Storage Temperature	-65C to +150C
Lead Temperature (Soldering, 10 seconds)	+300C
ESD Classification	Class 1
Maximum Power Dissipation	500 mW

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Supply Voltage (Vcc)	4.5V to 5.5V
Operating Temperature	-55C to +125C
Minimum Input Edge Rate (dV/dt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Maximum Output Current	
High Level (Ioh)	-24 mA
Low Level (Iol)	48 mA

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: 4.5V to 5.5V Temp Range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ICCH	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		250.0	uA	1, 2, 3
ICCL	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		30.0	mA	1, 2, 3
ICCZ	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 4	VCC		250.0	uA	1, 2, 3
ICCT	Supply Current	VCC=5.5V, OE=0.0V Input under test=3.4V Other inputs=5.5V or 0.0V	1, 4	VCC		2.5	mA	1, 2, 3
		VCC=5.5V, OE=3.4V Other inputs=5.5V or 0.0V	1, 4	VCC		2.5	mA	1, 2, 3
		VCC=5.5V, OE=5.5V Input under test=3.4V Other inputs=5.5V or 0.0V	1, 4	VCC		50.0	uA	1, 2, 3
IIH	High Level Input Current	VCC=5.5V, VINH=5.5V	1, 4	IN		2.0	uA	1, 2, 3
IIL	Low Level Input Current	VCC=5.5V, VINL=0.0V	1, 4	IN		-2.0	uA	1, 2, 3
IOZH	Maximum TRI-STATE Leakage Current HIGH	VCC=5.5V, VOUT=2.7V VINL=0.0V, VIH (OE)=2.0V	1, 4	OUT		10.0	uA	1, 2, 3
IOZL	Maximum TRI-STATE Leakage Current LOW	VCC=5.5V, VOUT=0.5V VINH=5.5V, VIH (OE)=2.0V	1, 4	OUT		-10.0	uA	1, 2, 3
ICEX	Output High Leakage Current	VCC=5.5V, VOUT=5.5V VINH=5.5V	1, 4	OUT		50.0	uA	1, 2, 3
IOS	Output Short Circuit Current	VCC=5.5V, VOUT=0.0V VINH=5.5V	1, 4, 10	OUT	-100	-275	mA	1, 2, 3
IOS1	Output Short Circuit Current	VCC=5.5V, VOUT=2.5V VINH=5.5V	1, 4, 10	OUT	-50	-180	mA	1, 2, 3
IBVI	Input High Current Breakdown Test	VCC=5.5V, VINH=7.0V	1, 4	OUT		7.0	uA	1, 2, 3
IZZ	Bus Drainage Test	VCC=0.0V, VOUT=4.5V, VINL=0.0V	1, 4	OUT	-100	100	uA	1, 2, 3
VOL	Low Level Output Voltage	VCC=4.5V, IOL=48.0mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT		0.55	V	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: 4.5V to 5.5V Temp Range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VOH	High Level Output Voltage	VCC=4.5V, IOH=-24.0mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	2.0		V	1, 2, 3
		VCC=4.5V, IOH=-3mA, VINH=4.5V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	2.5		V	1, 2, 3
		VCC=5.0V, IOH=-3mA, VINH=5.0V, VINL=0.0V, VIH=2.0V, VIL=0.8V	1, 4	OUT	3.0		V	1, 2, 3
VID	Input Leakage Test	VCC=0.0V, IID=1.9uA, VINL=0.0V	1, 4	IN	4.75		V	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IKL=-18mA, VINH=4.5V, VINL=0.0V	1, 4	IN		-1.2	V	1, 2, 3
VOLP	Low Level Ground Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	IN		1.2	V	4
VOLV	Low Level Ground Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	IN		-1.8	V	4
VOHP	High Level VCC Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	IN		1.5	V	4
VOHV	High Level VCC Bounce	VCC=5.0V, LOAD : 50pF / 500 OHMS	7, 8	IN		-1.1	V	4
CIN	Input Capacitance	VCC=0.0V	7	IN		11.0	pF	4
COUT	Output Capacitance	VCC=5.5V	7	OUT		16.0	pF	4

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pF RL=500 OHMS TRISE/TFALL = 3.0nS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	In to On	1.0	4.1	ns	9
			2, 5	In to On	1.0	5.3	ns	10, 11
tpHL	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	In to On	1.0	4.2	ns	9
			2, 5	In to On	1.0	5.0	ns	10, 11
tpZL	Output Enable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	$\overline{OE}$ to On	2.1	5.6	ns	9
			2, 5	$\overline{OE}$ to On	1.2	7.9	ns	10, 11
tpZH	Output Enable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	$\overline{OE}$ to On	1.1	5.5	ns	9
			2, 5	$\overline{OE}$ to On	0.8	6.5	ns	10, 11
tpHZ	Output Disable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	$\overline{OE}$ to On	2.1	5.6	ns	9
			2, 5	$\overline{OE}$ to On	1.2	7.6	ns	10, 11
tpLZ	Output Disable Time	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55C/125C	2, 5	$\overline{OE}$ to On	1.5	5.6	ns	9
			2, 5	$\overline{OE}$ to On	1.0	7.9	ns	10, 11

Note 1: SCREEN TESTED 100% ON EACH DEVICE AT -55C, +125C & +25C TEMP., SUBGROUPS 1,2,3,7 & 8.

Note 2: SCREEN TESTED 100% ON EACH DEVICE AT -55C, +25C & +125C TEMP., SUBGROUPS A9, A10 & A11.
Note 3: SCREEN TESTED 100% ON EACH DEVICE AT +25C TEMP. ONLY, SUBGROUP 9.
Note 4: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C, +125C & -55C TEMP., SUBGROUPS A1, 2, 3, 7 & 8.
Note 5: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C, +125C & -55C TEMP., SUBGROUPS A9, 10, & 11.
Note 6: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C TEMP ONLY, SUBGROUP A9.

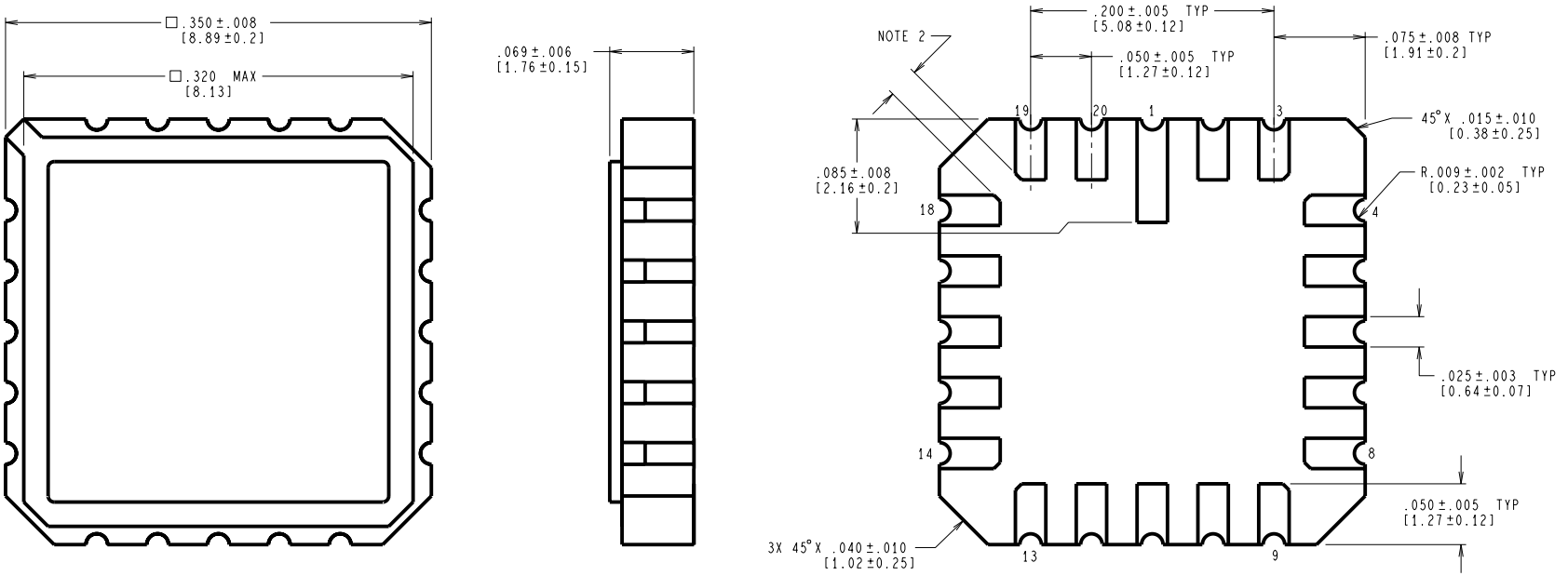
Note 7: NOT TESTED (GUARANTEED BY DESIGN CHARACTERIZATION DATA).
Note 8: MAX NUMBER OF OUTPUTS DEFINED AS (N). N-1 DATA INPUTS ARE DRIVEN 0V TO 3.0V. ONE OUTPUT @ VOL OR @ VOH.
Note 9: MAX NUMBER OF DATA INPUTS (N) SWITCHING. (N-1) INPUTS SWITCHING 0V TO 3.0V. INPUT-UNDERTEST SWITCHING: 3V TO THRESHOLD (VILD), 0V TO THRESHOLD (VIHD), FREQ.= 1 MHZ.
Note 10: MAXIMUM TEST DURATION NOT TO EXCEED ONE SECOND, NOT MORE THAN ONE OUTPUT SHORTED AT ONE TIME.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J20ARM	CERDIP (J), 20 LEAD (P/P DWG)
P000062A	(new)
P000063A	(new)
W20ARF	CERPACK (W), 20 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

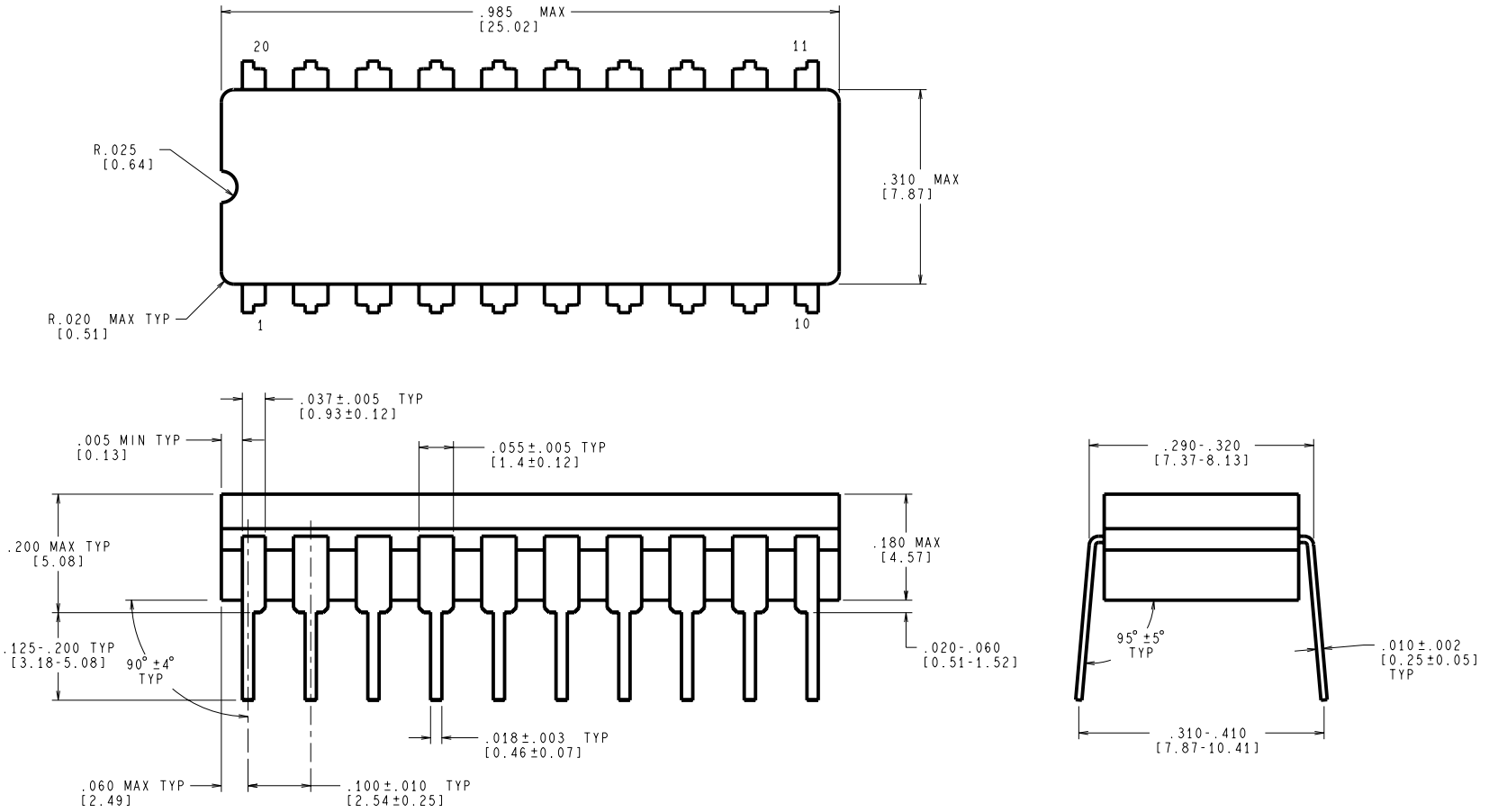
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
N	REVISE AND REDRAW PER CURRENT STANDARD; UPDATE TITLE & MIL/AERO STAMP.	11696	03/27/1997	MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:
   a. 200 MICROINCHES/ 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
   b. 200 TO 800 MICROINCHES/ 5.08 TO 20.32 MICROMETERS TIN PLATE OVER 50 TO 300 MICROINCHES/ 1.27 TO 7.62 MICROMETERS NICKEL UNDERPLATE OR BASIS METAL.
   c. 50 TO 100 MICROINCHES/ 1.27 TO 2.54 MICROMETERS GOLD OVER 50 TO 350 MICROINCHES/ 1.27 TO 8.89 MICROMETERS NICKEL UNDERPLATE.
2. NO JEDEC REGISTRATION AS OF 03/27/1997.

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	03/27/1997
DFTG. CHK.	
ENGR. CHK.	

PROJECTION
INCH [MM]

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2900 Semiconductor dr, Santa Clara, CA 95052-8090

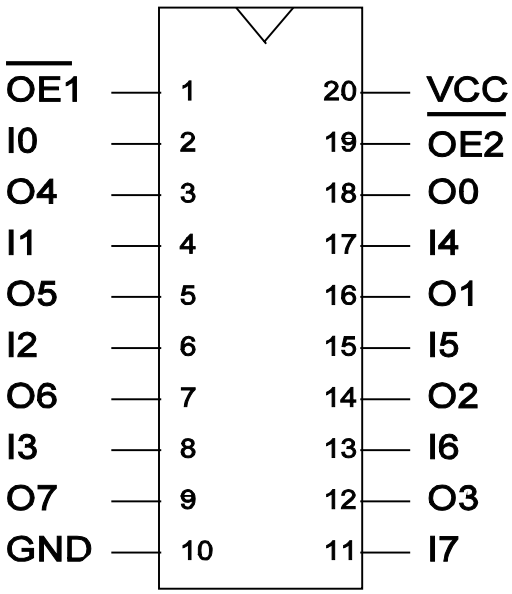
CERDIP, 20 LEAD, .300 CENTERS

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-J20A	N

DO NOT SCALE DRAWING | SHEET 1 of 1

CONNECTION DIAGRAM

54ABT244

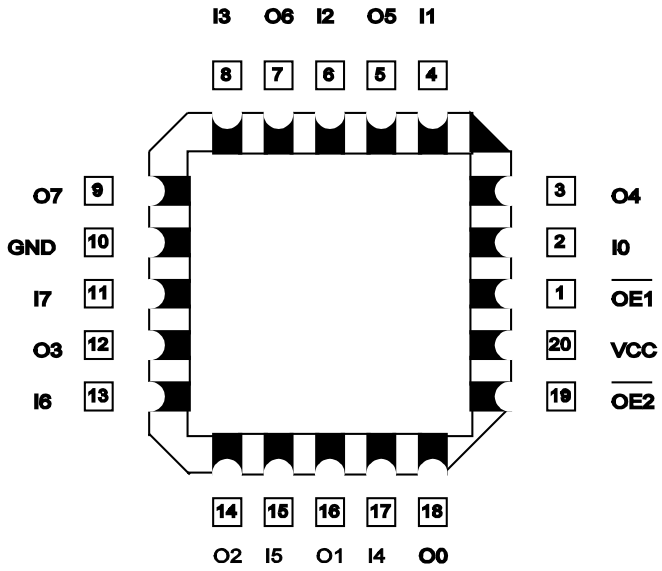


CDIP & FLATPACK PINOUT

(DWG # P000062A)

CONNECTION DIAGRAM

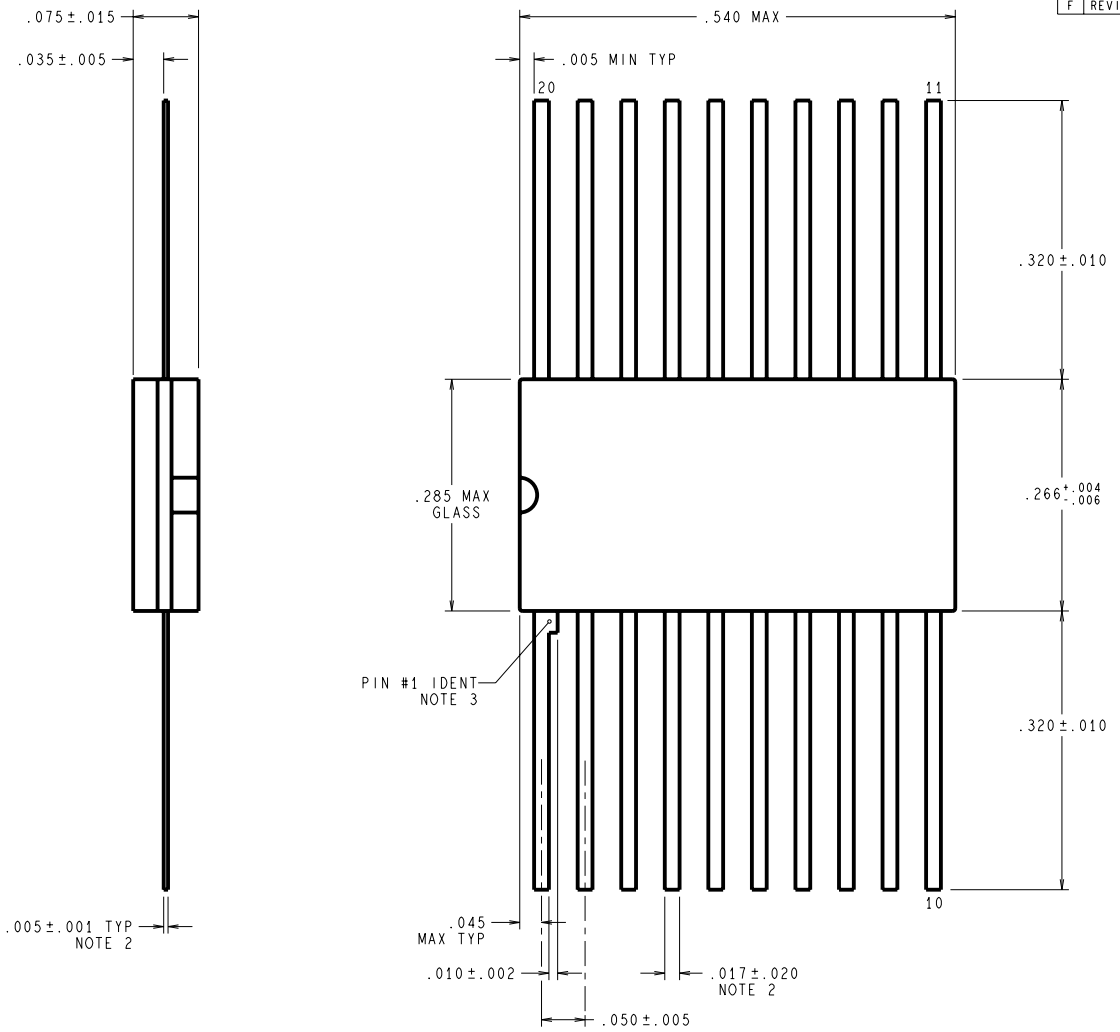
54ABT244



CERAMIC LEADLESS PINOUT

(DWG # P000063A)

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10512	07/28/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. NO JEDEC REGISTRATION AS OF 02/70/94.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 20 LEAD

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W20A	F

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0001565	09/24/98	Bill Petcher	Changed MDS MN54ABT244-X REV 0A0 to MN54ABT244-X REV 0B0