Data Sheet

SSM6515

Ultra Low Power, Class-D Audio Amplifier

FEATURES

- Filterless digital input, mono differential output Class-D amplifier with 3-level Σ-Δ modulation optimized for headphone drive
- Operates from single 1.8 V supply
- 80 mW output power, 16 Ω load at <0.1% THD + N
- 2.57 µV rms noise, 113 dB A weighted signal-to-noise ratio and dynamic range
- 0.003% THD + N at 30 mW, 1 kHz output 32 Ω load
- I^2C control with up to 4 pin selectable addresses or standalone operation
- Multiple serial data formats
  - TDM, I^2S, or left justified slave
  - PDM input operating from 2.8224 MHz to 12.288 MHz
- Support sample rates from 8 kHz to 768 kHz
- 3.9 µs latency with 6 MHz PDM input
- Flexible digital gain adjustment
- DC blocking high-pass filter with programmable corner frequency
- 1.55 mW typical idle power in high performance mode
- Low power modes for reduced power consumption
- Flexible output gain limiter and clipping
- Auto power-down feature with zero digital input
- Short-circuit protection
- Pop and click suppression
- User-selectable ultralow EMI emissions mode
- Power-on reset
- 1.8 V PV_{DD} supply
- 1.2 V to 1.8 V IOV_{DD} supply
- 11-ball, 0.984 mm × 1.444 mm, 0.35 mm pitch WLCSP

APPLICATIONS

- Wireless headphones
- Active noise canceling headphones
- Smartphone earpiece speakers
- Hearing assistance devices
- Portable electronics

GENERAL DESCRIPTION

The SSM6515 is a fully integrated, high efficiency, mono Class-D audio amplifier with digital input that is ideally suited for use in wireless headphones. The application circuit requires few external components and operates from a 1.8 V (PV_{DD}) supply and a 1.2 V to 1.8 V (IOV_{DD}) supply. With 1.8 V signaling, these can be shared. It can deliver 85 mW of continuous output power into a 16 Ω load with <1% total harmonic distortion plus noise (THD + N).

The SSM6515 features a high efficiency, low noise modulation scheme that requires no external inductor/capacitor (LC) output filters. This scheme continues to provide high efficiency even at very low output power resulting in battery life savings compared to conventional headphone amplifiers. The device operates with > 90% efficiency at 55 mW into a 16 Ω load and it has a signal-to-noise ratio (SNR) of 113 dB, A weighted. Spread spectrum, stable common-mode pulse density modulation provides a much lower electromagnetic interference (EMI) radiated emissions compared with other Class-D architectures.

The digital input eliminates the need of an external digital-to-analog converter (DAC). The SSM6515 has a micropower shutdown mode with a typical shutdown current of 6 µA at the 1.8 V PV_{DD} supply and can automatically power down with no input. The device also includes pop and click suppression circuitry that minimizes voltage glitches at the output during turn on and turn off. Inputs support various serial audio formats, including I^2S, time division multiplexing (TDM), and pulse density modulation (PDM).

The SSM6515 is designed to operate with an I^2C control interface or in standalone mode and specified over the temperature range of −40°C to +85°C. The device has built-in output short-circuit protection. The SSM6515 is available in a halide free, 11-ball, 0.984 mm × 1.444 mm, 0.35 mm pitch wafer-level chip scale package (WLCSP).

Note that throughout this data sheet, multifunction pins are referred to by the entire pin name or by a single function of the pin.

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

4/2022—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

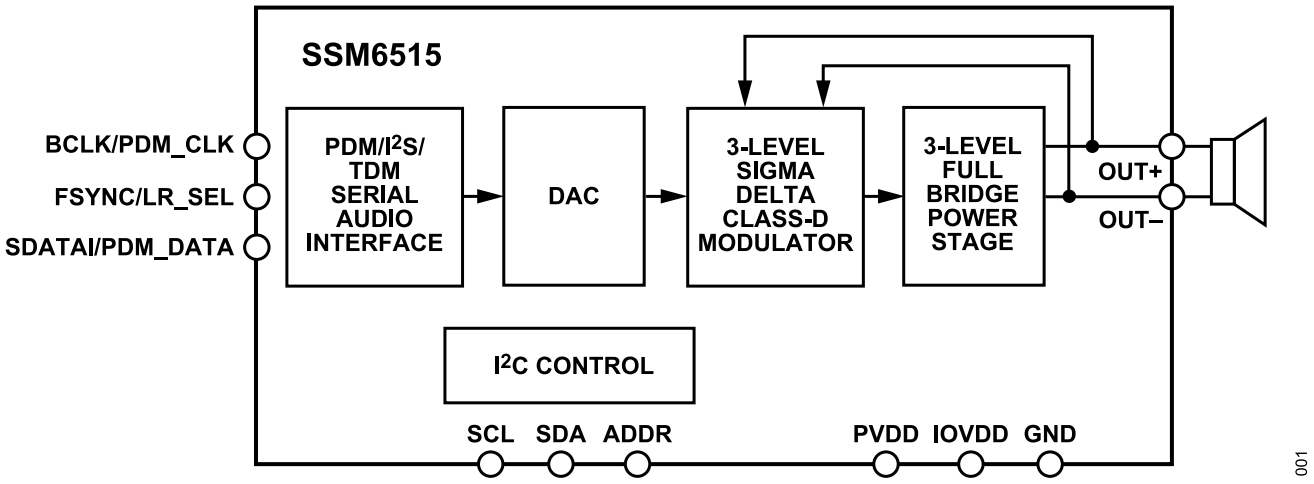

Figure 1.

SPECIFICATIONS

PV_{DD} = 1.8 V, R_L = 16 Ω + 33 µH, BCLK = 3.072 MHz, FSYNC = 48 kHz, −40°C to +85°C, AMP_LPM = 0, and DAC_PWR_MODE = 1, unless otherwise noted. The measurements are taken with a 20 kHz AES17 low-pass filter. The other load impedances used are 8 Ω + 15 µH and 32 Ω + 33 µH.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS		Differential operation				
Full-Scale Output Voltage		0 dBFS to DAC, 16 Ω Load		1.15		V rms
Dynamic Range[1]	DNR	20 Hz to 20 kHz, −60 dB input				
With A Weighted Filter (RMS)				113		dB
With Flat 20 Hz to 20 kHz Filter				110		dB
SNR[2]	SNR	20 Hz to 20 kHz				
With A Weighted Filter (RMS)				113		dB
With Flat 20 Hz to 20 kHz Filter				110		dB
Output Noise		20 Hz to 20 kHz				
With A Weighted Filter (RMS)				2.57		µV rms
THD + N Level		−2 dBFS, AMP_LPM = 0, DAC_PWR_MODE = 1		−90		dBV
		−2 dBFS, AMP_LPM = 1, DAC_PWR_MODE = 2		−81		dBV
THD + N Ratio						
32 Ω Load		P_{OUT} = 30 mW		0.003		%
		P_{OUT} = 1 mW		0.007		%
24 Ω Load		P_{OUT} = 40 mW		0.003		%
16 Ω Load		P_{OUT} = 60 mW		0.003		%
8 Ω Load		P_{OUT} = 120 mW		0.004		%
Headphone Output Power	P_{OUT}					
32 Ω Load		<0.1% THD + N		40		mW
24 Ω Load		<0.1% THD + N		54		mW
16 Ω Load		<0.1% THD + N		80		mW
8 Ω Load		<0.1% THD + N		160		mW
Gain Error				±2.5		%
DC Offset	V_{OOS}			±0.1		mV
Pop-Click Level		A weighted, peak		0.5		mVp
Resistive Load			6			Ω
Load Inductance			5			µH
Common-Mode Output Capacitance		Capacitance from OUTx to GND or PVDD			470	pF
Power Efficiency	η	From PVDD supply into 16 Ω, 60 mW		90		%
Power Supply Rejection Ratio (PSRR)						
		100 mV p-p at 1 kHz		90		dB
		100 mV p-p at 10 kHz		72		dB
Input to Output Delay						
I^2S Mode		f_S = 48 kHz		49.4		µs
		f_S = 96 kHz		22.4		µs
		f_S = 192 kHz		11.9		µs
PDM Mode		f_S = 3.072 MHz, PDM_FILT = 0, DAC_PWR_MODE = 0/1		15.1		µs
		f_S = 3.072 MHz, PDM_FILT = 1, DAC_PWR_MODE = 0/1		8.7		µs
		f_S = 3.072 MHz, PDM_FILT = 2, DAC_PWR_MODE = 0/1		7.5		µs
		f_S = 6.144 MHz, PDM_FILT = 0, DAC_PWR_MODE = 0/1		14.4		µs
		f_S = 6.144 MHz, PDM_FILT = 1, DAC_PWR_MODE = 0/1		4.6		µs
		f_S = 6.144 MHz, PDM_FILT = 2, DAC_PWR_MODE = 0/1		3.9		µs
		f_S = 6.144 MHz, PDM_FILT = 1, DAC_PWR_MODE = 2		5.9		µs
		f_S = 6.144 MHz, PDM_FILT = 2, DAC_PWR_MODE = 2		5.2		µs

SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		f_S = 12.288 MHz, PDM_FILT = 0, DAC_PWR_MODE = 0/1		7.4		µs
		f_S = 12.288 MHz, PDM_FILT = 1, DAC_PWR_MODE = 0/1		4.5		µs
		f_S = 12.288MHz, PDM_FILT = 2, DAC_PWR_MODE = 0/1		2.9		µs
POWER SUPPLIES						
Supply Voltage Range	PV_{DD}		1.7	1.8	1.98	V
Supply Voltage Range	IOV_{DD}		1.1	1.8	1.98	V
PV_{DD} Undervoltage Trip Point		PV_{DD} UVLO		1.55		V
DAC						
Internal Resolution		DAC and all digital processing	24			Bits
Digital Gain						
Step				0.375		dB
Range			−71		+24	dB
Ramp Rate				4.5		dB/ms
POWER CONSUMPTION						
Idle I^2S Mode	I(PVDD)	Dither in		0.85		mA
		Dither in, DAC_PWR_MODE = 2, AMP_LPM = 1		0.72		mA
Idle PDM Mode	I(PVDD)	Dither in, 3.072 MHz,		0.91		mA
	I(PVDD)	Dither in, 3.072 MHz, DAC_PWR_MODE = 2, AMP_LPM = 1		0.82		mA
	I(IOVDD)			0.01		mA
1 mW Output I^2S Mode	I(PVDD)	1 mW into 16 Ω		1.54		mA
		1 mW into 16 Ω , DAC_PWR_MODE = 2, AMP_LPM = 1		1.45		mA
1 mW Output PDM Mode	I(PVDD)	1 mW into 16 Ω, 3.072 MHz		1.58		mA
	I(PVDD)	1 mW into 16 Ω, 3.072 MHz, DAC_PWR_MODE = 2, AMP_LPM = 1		1.49		mA
	I(IOVDD)			0.01		mA
Power-Down	I(PVDD)	Clocks off, SWPDN = 1		6.11		µA
	I(IOVDD)			0.55		µA
	I(PVDD)	Clocks on, SWPDN = 1		8.86		µA
	I(IOVDD)			6.07		µA
INPUT SENSITIVITY		Measured at 1 kHz, no load, full scale output voltage = 1.15 V rms				
I^2S/TDM Mode				0		dBFS
PDM Mode				−6		dBFS
OVERTEMPERATURE						
Overtemperature Warning (OTW)		Overtemperature warning trip point		90		°C
Overtemperature Protection (OTP)		Overtemperature protection trip point		130		°C
Overtemperature Protection Recovery (OTPRCV)		Overtemperature protection recovery		90		°C
SHUTDOWN CONTROL						
Turn On Time	t_{WU}	3.072 MHz BCLK		20.5		ms
Turn On Time	t_{WU}	2.4 MHz BCLK		26		ms
Turn Off Time	t_{SD}	From 0 dB volume setting with ramp down, 3.072 MHz BCLK		24.5		ms
Turn Off Time	t_{SD}	From 24 dB volume setting with ramp down, 2.4 MHz BCLK		30		ms
Turn Off Time	t_{SD}	Output muted, 3.072 MHz BCLK		8.5		ms

[1] Dynamic range is the ratio of the sum of the noise and harmonic power in the band of interest with a −60 dBFS signal present to the full-scale power level in decibels.

[2] SNR is the ratio of the sum of all noise power in the band of interest with no signal present to the full-scale power level in decibels.

SPECIFICATIONS

Table 2. Digital Input/Output

Parameter	Min	Typ	Max	Unit
HIGH INPUT VOLTAGE (V_{IH})				
BCLK, FSYNC, SDATAI	0.7 × IOV_{DD}		1.98	V
SCL and SDA	0.7 × IOV_{DD}		1.98	V
LOW INPUT VOLTAGE (V_{IL})				
BCLK, FSYNC, SDATAI, SDA, SCL	−0.3		+0.3 × IOV_{DD}	V
INPUT LEAKAGE				
BCLK, FSYNC, SDATAI, SDA, SCL, ADDR				
High Input Current (I_{IH})			1	µA
Low Input Current (I_{IL})			1	µA
INPUT CAPACITANCE			5	pF

TIMING SPECIFICATIONS

Table 3. I^2C Port Timing

Parameter	Min	Max	Unit	Description
I^2C PORT				
f_{SCL}		1	MHz	SCL frequency
t_{SCLH}	0.26		µs	SCL high
t_{SCLL}	0.5		µs	SCL low
t_{SCS}	0.26		µs	Setup time, relevant for repeated start condition
t_{SCH}	0.26		µs	Hold time, after this period, the first clock is generated
t_{DS}	50		ns	Data setup time
t_{SCR}		120	ns	SCL rise time
t_{SCF}		120	ns	SCL fall time
t_{SDR}		120	ns	SDA rise time
t_{SDF}		120	ns	SDA fall time
t_{BFT}	0.5		µs	Bus-free time (time between stop and start)

Table 4. Serial Port Digital Input Timing (I^2S/TDM Operation Modes Only)

Parameter	Min	Max	Unit	Description
SERIAL PORT				
t_{BIL}	8		ns	BCLK low pulse width
t_{BIH}	8		ns	BCLK high pulse width
t_{SIS}	4		ns	SDATA setup time to BCLK rising edge
t_{SIH}	4		ns	SDATA hold time from BCLK rising edge
t_{LIS}	5		ns	FSYNC setup time to BCLK rising edge
t_{LIH}	5		ns	FSYNC hold time to BCLK rising edge
t_{BP}	20		ns	Minimum BCLK period
$duty_{BCLK}$	40	60	%	BCLK duty cycle

Table 5. PDM Timing Parameters

	Limit			
Parameter	Min	Max	Unit	Description
PDM Clock Frequency	2.8224	12.4	MHz	
t_{FALL}		10	ns	Clock fall time
t_{RISE}		10	ns	Clock rise time
t_{SETUP}	10		ns	Data setup time
t_{HOLD}	7		ns	Data hold time

SPECIFICATIONS

Digital Timing Diagrams

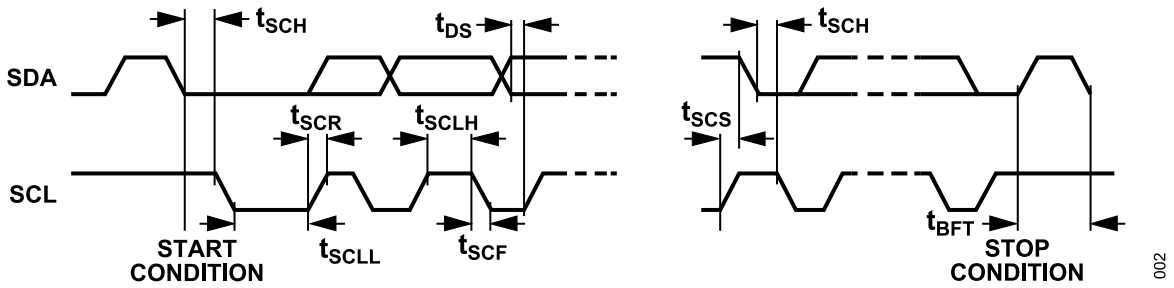

Figure 2. I²C Port Timing

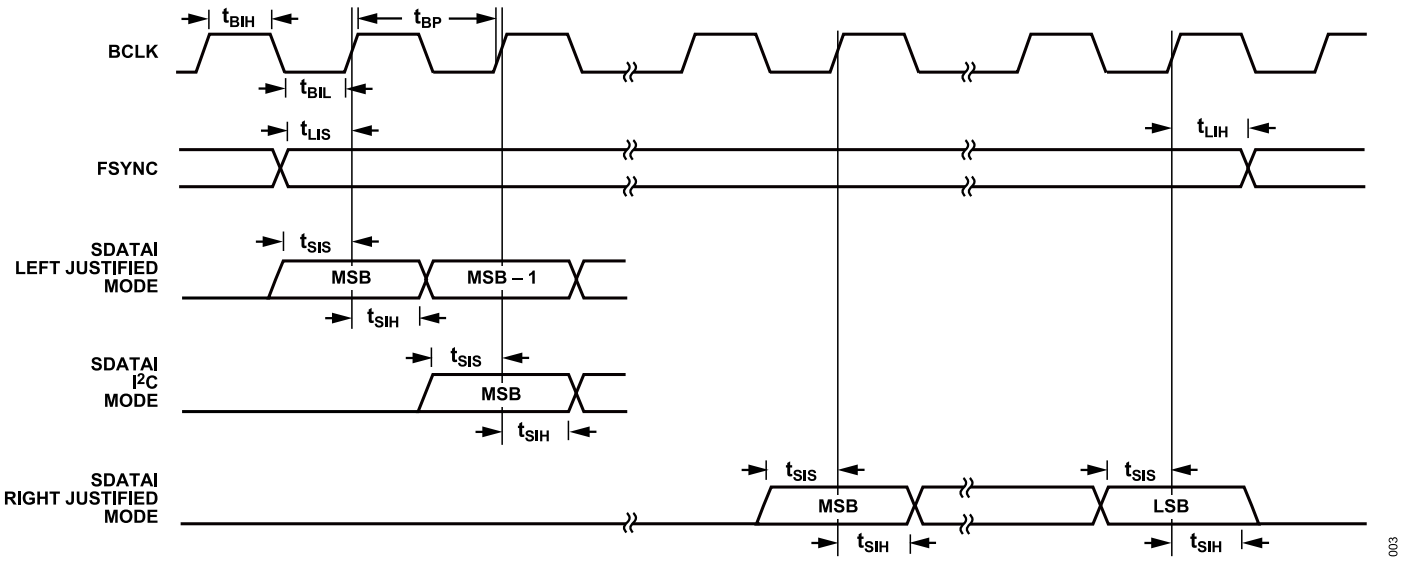

Figure 3. Serial Port SDATAI Timing

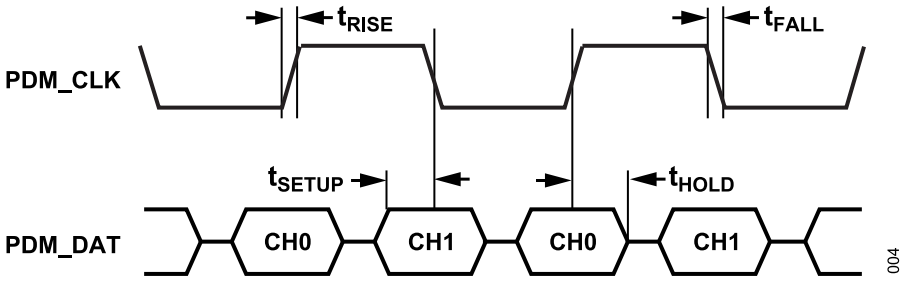

Figure 4. PDM Input/Output Format

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
PV_{DD} Supply Voltage	−0.3 V to +1.98 V
BCLK, FSYNC, ADDR, SDATAI, SCL, SDA, and ADDR Input Voltage	−0.3 V to +1.98 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} and θ_{JB} are determined according to JESD51-9 on a 4-layer PCB with natural convection cooling.

Table 7. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JB}[1]	Unit
CB-11-3	79.87	13.26	°C/W

[1] Thermal impedance simulated values are based on JEDEC2S2P thermal test board with two thermal vias. See JEDEC JESD51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for SSM6515

Table 8. SSM6515, 11-Ball WLCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±1500	1C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. **Charged devices and circuit boards can discharge without detection.** Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

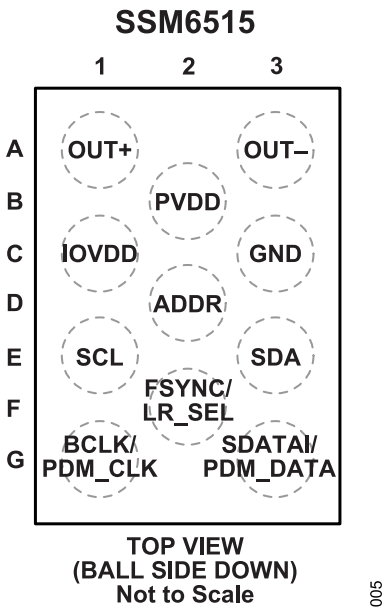

Figure 5. Pin Configuration (Top Side View)

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	OUT+	AOUT	Noninverting Output.
A3	OUT−	AOUT	Inverting Output.
B2	PVDD	PWR	Power and Analog Stage Supply.
C1	IOVDD	PWR	IO Power Supply.
C3	GND	PWR	Power Ground.
D2	ADDR	DIN	Device Address Selection.
E1	SCL	DIN	I^2C Clock.
E3	SDA	DIO	I^2C Data.
F2	FSYNC/LR_SEL	DIN	Frame Sync Input.
G1	BCLK/PDM_CLK	DIN	TDM/I^2S Bit Clock Input, PDM Clock Input.
G3	SDATAI/PDM_DATA	DIN	I^2S/TDM Serial Data Input or PDM Data Input.

[1] AOUT is analog output, PWR is power supply or ground pin, DIN is digital input, and DIO is digital input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

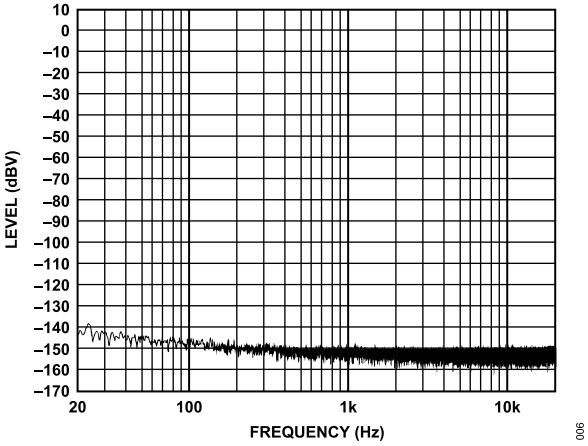

Figure 6. Fast Fourier Transform (FFT), No Signal, R_{LOAD} = 16 Ω

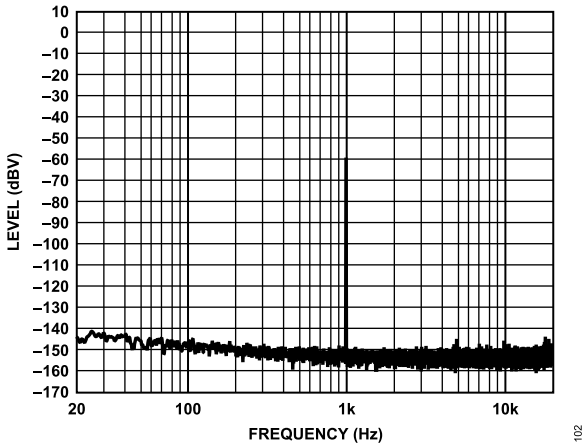

Figure 7. FFT, −60 dBFS Input, R_{LOAD} = 16 Ω

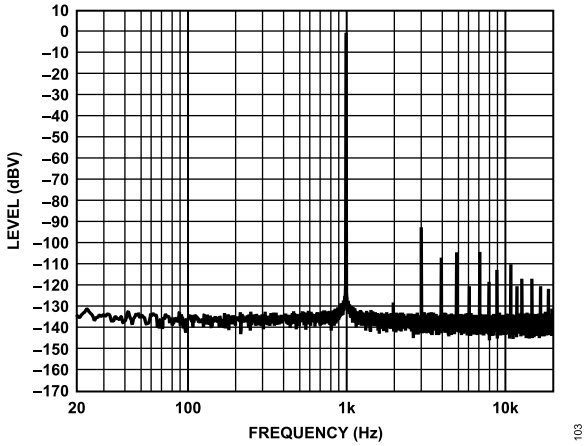

Figure 8. FFT, −2 dBFS Input, R_{LOAD} = 16 Ω

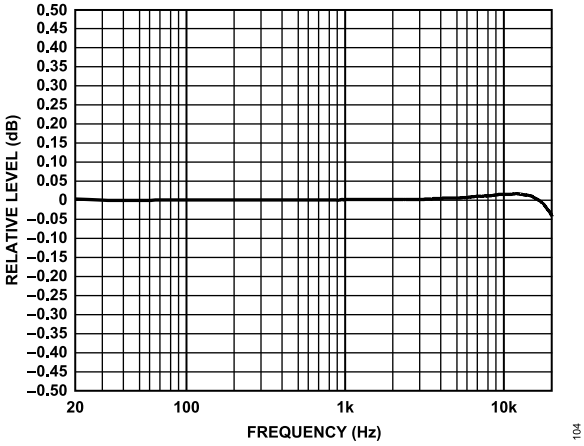

Figure 9. Frequency Response, −20 dBFS Input, I^2S Mode, 16 Ω

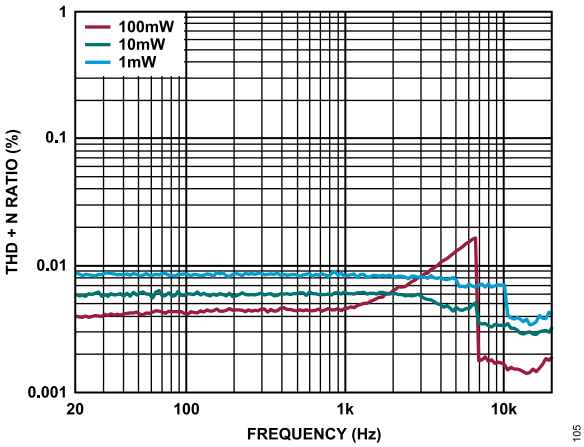

Figure 10. THD + N Ratio vs. Frequency, AMP_LPM = 0, R_{LOAD} = 8 Ω

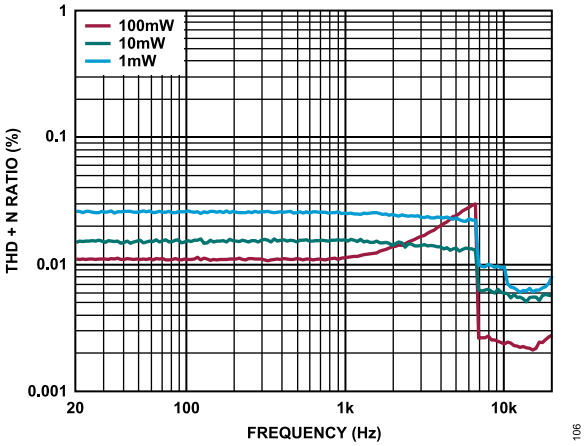

Figure 11. THD + N Ratio vs. Frequency, AMP_LPM = 1, R_{LOAD} = 8 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

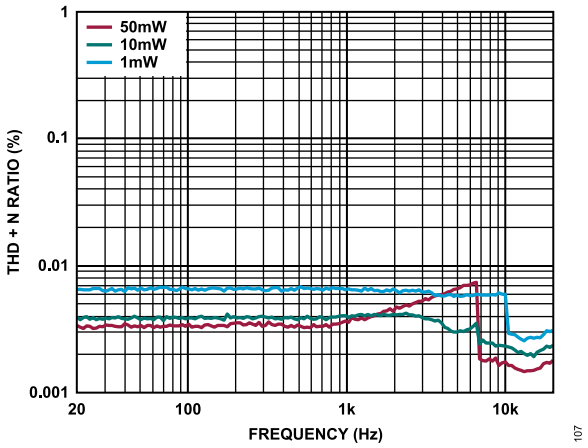

Figure 12. THD + N Ratio vs. Frequency, AMP_LPM = 0, R_{LOAD} = 16 Ω

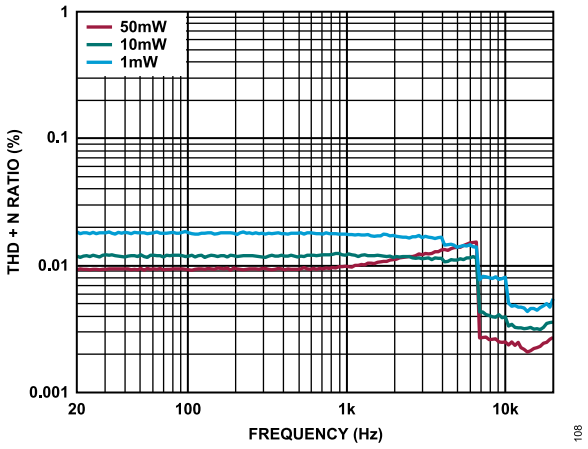

Figure 13. THD + N Ratio vs. Frequency, AMP_LPM = 1, R_{LOAD} = 16 Ω

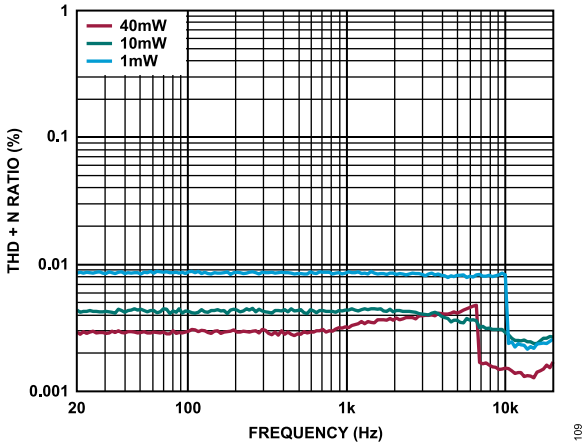

Figure 14. THD + N Ratio vs. Frequency, AMP_LPM = 0, R_{LOAD} = 24 Ω

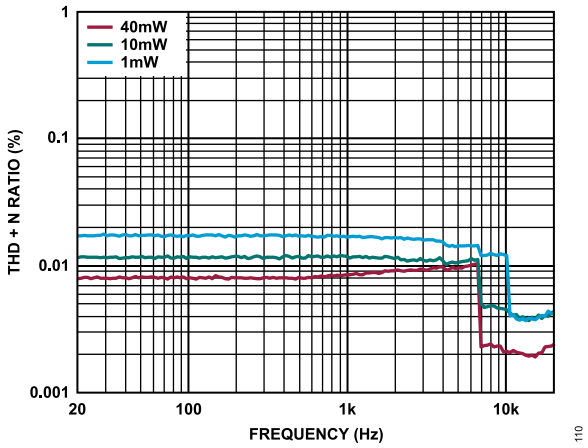

Figure 15. THD + N Ratio vs. Frequency, AMP_LPM = 1, R_{LOAD} = 24 Ω

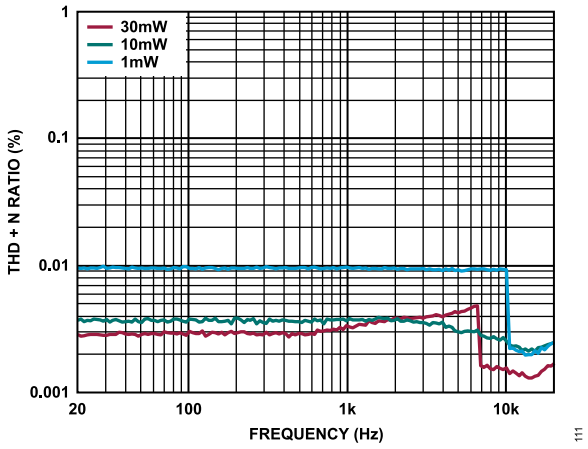

Figure 16. THD + N Ratio vs. Frequency, AMP_LPM = 0, R_{LOAD} = 32 Ω

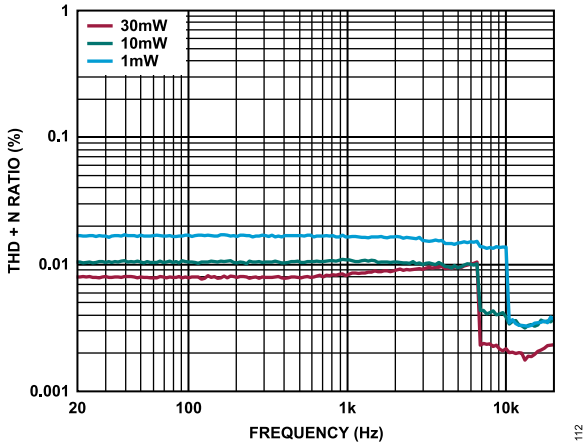

Figure 17. THD + N Ratio vs. Frequency, AMP_LPM = 1, R_{LOAD} = 32 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

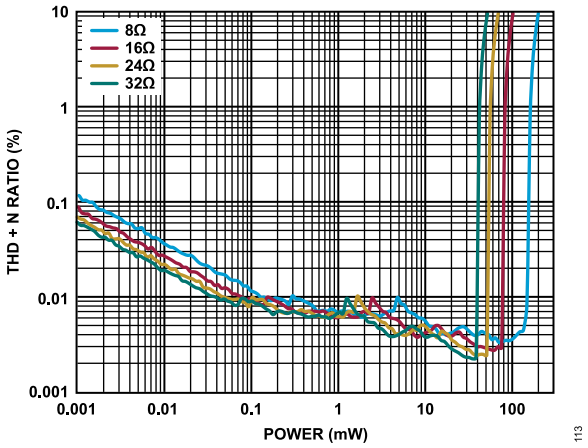

Figure 18. THD + N Ratio vs. Power, AMP_LPM = 0

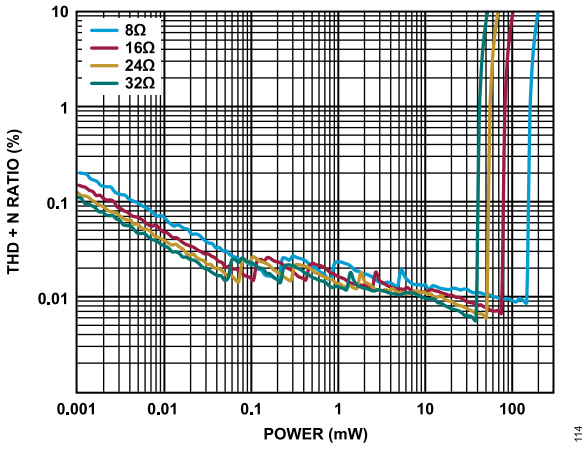

Figure 19. THD + N Ratio vs. Power, AMP_LPM = 1

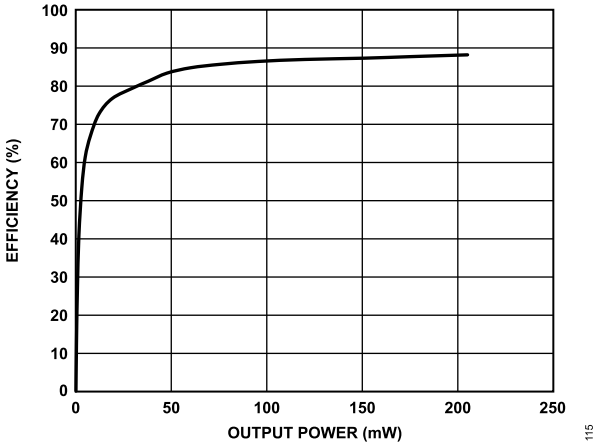

Figure 20. Efficiency, R_{LOAD} = 8 Ω, Low EMI Mode

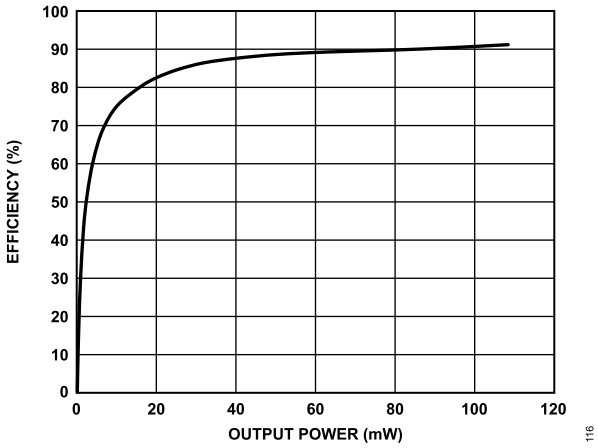

Figure 21. Efficiency, R_{LOAD} = 16 Ω, Low EMI Mode

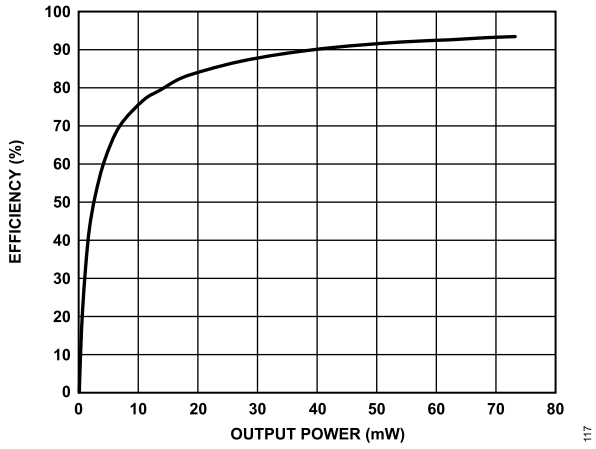

Figure 22. Efficiency, R_{LOAD} = 24 Ω, Low EMI Mode

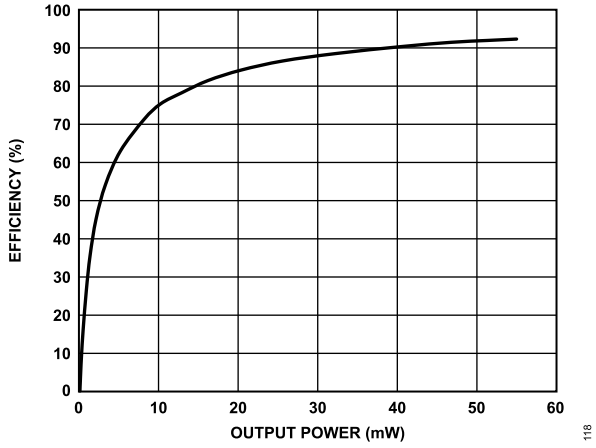

Figure 23. Efficiency, R_{LOAD} = 32 Ω, Low EMI Mode

TYPICAL PERFORMANCE CHARACTERISTICS

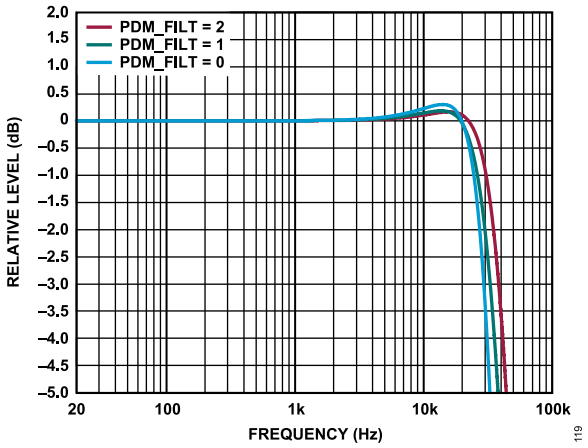

Figure 24. Frequency Response, PDM, 16 Ω, BCLK = 3.072 MHz

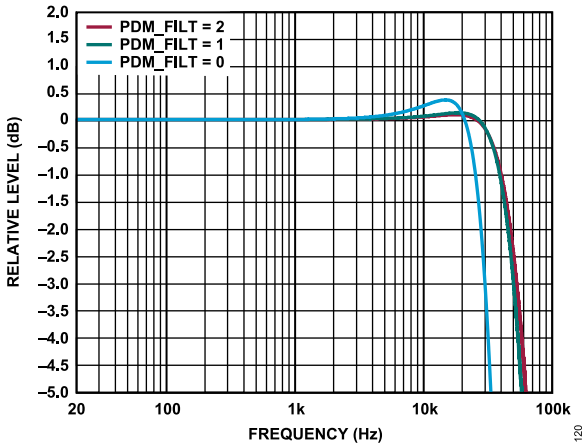

Figure 25. Frequency Response, PDM, 16 Ω, BCLK = 6.144 MHz

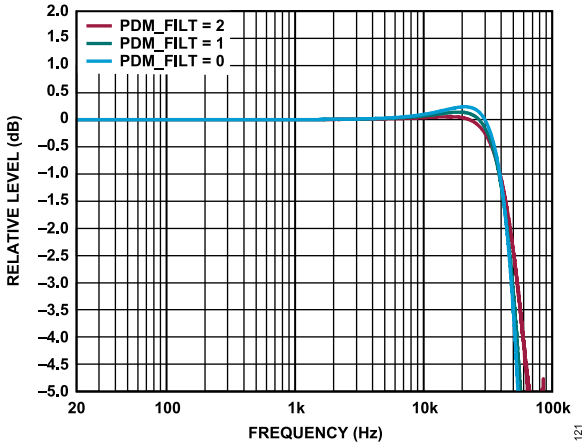

Figure 26. Frequency Response, PDM, 16 Ω, BCLK = 12.288 MHz

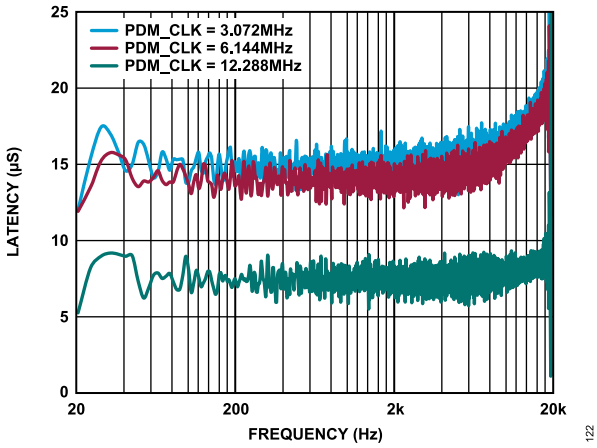

Figure 27. PDM Latency, 16 Ω, PDM_FILT = 0

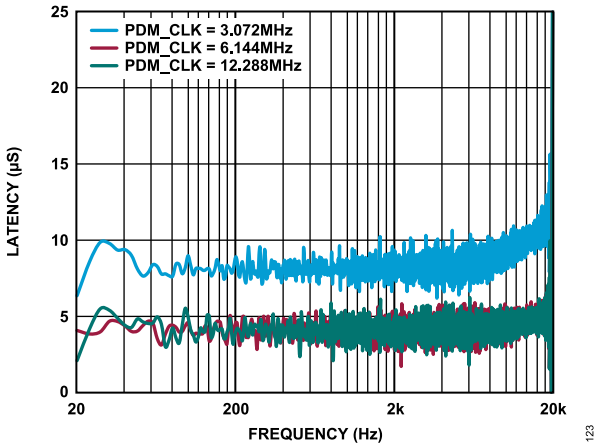

Figure 28. PDM Latency, 16 Ω, PDM_FILT = 1

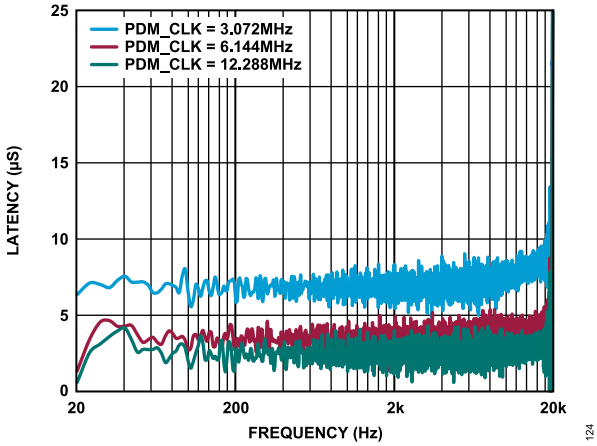

Figure 29. PDM Latency, 16 Ω, PDM_FILT = 2

THEORY OF OPERATION

OVERVIEW

The SSM6515 Class-D audio amplifier features a filterless, common-mode stable modulation scheme that reduces the external component count, conserving board space and reducing system cost. The SSM6515 does not require an output filter. It relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to recover the audio component of the square wave output. Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM6515 uses Σ-Δ pulse-density modulation to determine the switching pattern of the output devices, resulting in a number of important benefits. Σ-Δ modulation reduces the amplitude of spectral components at high frequencies, reducing EMI emission that can otherwise be radiated by speakers and cable traces. In addition, the SSM6515 maintains a stable common-mode output voltage that further reduces power consumption, EMI, and filtering needed compared to other filterless Class-D topologies.

The SSM6515 also integrates overcurrent protection that can be disabled for lower power consumption. Overtemperature warnings and protection are also integrated.

The SSM6515 supports two main modes of operation with control and data supplied through the I^{2}C and TDM/I^{2}S ports (see Table 11) or PDM interface. A standalone mode of operation without I^{2}C control is also supported.

POWER SUPPLIES

PVDD is used for the main output stage, DAC, and Class-D modulator. It is also used to generate a lower voltage purely internal core supply.

IOVDD is used for the input signaling to set the high and low voltage thresholds.

ADDR PIN SETUP AND CONTROL

The SSM6515 supports I^{2}C control. The ADDR pin can be set to four different levels: pulled to GND, pulled up to PV_{DD} via a 47 kΩ resistor, pulled down to ground via a 47 kΩ resistor, or left open. The state of the ADDR pin determines the I^{2}C device address or if the device is in standalone mode. By default, in I^{2}C mode, the device uses the BCLK, FSYNC, and SDATAI pins for TDM/I^{2}S data. Alternatively, the device can be set to receive PDM data by setting the PDM_MODE register bit field. See Table 11 for setting up the desired mode.

Table 10. I^{2}C Address Selection

ADDR Pin Connection	Control Port Mode	I^{2}C Address
GND	I^{2}C	0x34
Pull Down with 47 kΩ to GND	I^{2}C	0x35
Open	I^{2}C	0x36
Pull Up with 47 kΩ to PVDD	I^{2}C	0x37
PVDD	Standalone mode	Not applicable

Table 11. Serial Port Mode Setup for I^{2}S, TDM, and PDM

		Pin Usage		
Serial Port Mode	Description	BCLK Pin	FSYNC Pin	SDATAI Pin
I^{2}S/TDM	Sets the device into default I^{2}S/TDM mode	Bit clock input	Frame clock input	Data input I^{2}S/TDM format
PDM	Set the PDM_MODE bit to 1 in Register 0x06	PDM clock input	Tie to GND	Data input PDM format

THEORY OF OPERATION

STANDALONE OPERATING MODE

The SSM6515 supports a standalone operating mode that is enabled by connecting the ADDR pin to the PVDD supply. In this mode, an I²C interface is not required to operate the device. All registers are set to default in this mode, except for SPWDN = 0 and APWDN_EN = 1. Both I²S and PDM input options are supported by configuring the SCL, SDA, and FSYNC pins, as shown in Table 12.

Table 12. Standalone Mode Options

Mode	f_s	SCL Pin	SDA Pin	FSYNC Pin	Data Slot
I²S	48 kHz	GND	GND	FSYNC	Left
I²S	48 kHz	GND	IOVDD	FSYNC	Right
PDM	3 MHz	IOVDD	GND	GND	Left
PDM	3 MHz	IOVDD	GND	IOVDD	Right
PDM	6 MHz	IOVDD	IOVDD	GND	Left
PDM	6 MHz	IOVDD	IOVDD	IOVDD	Right

POWER-DOWN MODES

The SSM6515 can be powered down over the I²C interface. Setting the SPWDN bit to 1 fully powers down the device except for the I²C interface. By default, the device first ramps down the volume control to mute, then completes its power-down sequence to ensure a pop free power-down.

The SSM6515 also contains a clock loss detection circuit that monitors the BCLK input clock. When no BCLK/PDM_CLK is present, the device automatically powers down most internal circuitry to its lowest power state. When BCLK returns, the device automatically powers up following its usual power sequence.

To ensure the lowest pop and click performance and lowest power shutdown current, the SPWDN bit must be set to 1, and the power-down sequence completed, before removing the BCLK/PDM_CLK signal. See the Specifications section for the length of time of the power-down sequence, from SPWDN to when the clocks can be removed.

There is an optional automatic power-down feature when using I²S/TDM: the device enters a lower power state when 2048 consecutive zero input samples are received. The device automatically powers back up from this state once a single nonzero value sample is received. Only the I²C and digital audio input blocks are active when in auto power-down.

LOW POWER MODES

The SSM6515 has several modes where the power consumption can be lowered from the default settings.

For the various low power modes to take effect, they must be applied over I²C and then the clocks must be re-toggled, meaning they are turned off and then turned on. This ensures that the internal blocks are optimized correctly for a given setting.

DAC_PWR_MODE offers three levels of control, and all levels offer similar performance. The lowest power setting, DAC_PWR_MODE = 2, increases the latency of the audio stream by 1.3 µs.

DAC_PERF_MODE offers two levels of control. By default, it is in its lowest power setting. The higher performance setting can lower THD + N at high signal amplitudes with slightly increased power consumption.

DAC_IBIAS controls the level of bias current to the DAC. The lower power settings can cause an increase in distortion performance.

AMP_LPM = 1 can lower the power consumption used by the Class-D modulator at the expense of increased THD and noise.

PULSE CODE MODULATION (PCM) DIGITAL AUDIO SERIAL INTERFACE

The SSM6515 includes a standard serial audio interface (SAI) that is slave only and used when in I²C mode. The interface is capable of receiving I²S, left justified, right justified, or TDM formatted data.

Provide a BCLK signal to the SSM6515 for proper operation. The BCLK signal must have a minimum frequency of 2.048 MHz. The BCLK signal internally clocks the device. The BCLK rate is automatically detected by default, but the sampling frequency must be known to the device via the DAC_FS. The BCLK rates at 32 kHz to 48 kHz that are supported are 50×, 64×, 100×, 128×, 150×, 192×, 200×, 250×, 256×, 384×, 400×, 500×, 512×, 768×, 800×, and 1024× the sample rate. Note that at different sample rates, these supported ratios scale accordingly. Refer to Table 13 for a full list of ratios and register settings at different sample rates. Alternatively, the BCLK rate can be set manually via the BCLK_RATE register control.

The serial interfaces have three main operating modes. Stereo modes, typically I²S or left justified, are used when there are one or two chips on the interface bus. TDM modes are more flexible and can support up to 16 chips on the bus. These mode selections can be set via the I²C interface with the SPT_SAI_MODE bit.

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Table 13. BCLK_RATE Selection Table[1, 2]

LRCLK (kHz)	BCLK_RATE: Bits[4:0] of Register Address 0x05																
	00001	00010	00011	00100	00101	00110	00111	01000	01001	01010	01011	01100	01101	01110	01111	10000	10001
	BCLK: FSYNC Ratio																
8[3]	N/A	256	400	500	512	600	768	800	1000	1024	1536	1600	2000	2048	3072	4000	4096
12[4]	200	256	400	500	512	600	768	800	1000	1024	1536	1600	2000	2048	3072	4000	4096
16[3]	N/A	128	200	250	256	300	384	400	500	512	768	800	1000	1024	1536	1600	2048
24[4]	100	128	200	250	256	300	384	400	500	512	768	800	1000	1024	1536	1600	2048
32[3]	N/A	64	100	125	128	150	192	200	250	256	384	400	500	512	768	800	1024
44.1[5]	50	64	100	125	128	150	192	200	250	256	384	400	500	512	768	800	1024
48[5]	50	64	100	125	128	150	192	200	250	256	384	400	500	512	768	800	1024
88.2[5]	N/A	32	50	N/A	64	75	96	100	125	128	192	200	250	256	384	400	512
96[4]	N/A	32	50	N/A	64	75	96	100	125	128	192	200	250	256	384	400	512
176.4[5]	N/A	N/A	N/A	N/A	32	N/A	48	50	N/A	64	96	100	125	128	192	200	256
192[4]	N/A	N/A	N/A	N/A	32	N/A	48	50	N/A	64	96	100	125	128	192	200	256
384[4]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	32	48	50	N/A	64	96	N/A	N/A
768[4]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	32	48	N/A	N/A

1 Table 13 assumes a minimum of two channels.

2 N/A means not applicable.

3 32 kHz, 44.1 kHz, and 48 kHz are the sampling rates used to scale the ratio calculations for the SSM6515. 8 kHz and 16 kHz are scaled as 4x and 2x the 32 kHz settings, respectively.

4 32 kHz, 44.1 kHz, and 48 kHz, are the sampling rates used to scale the ratio calculations for the SSM6515. 12 kHz, 24 kHz, 96 kHz, 192 kHz, 384 kHz, and 768 kHz are scaled as 4x, 2x, 1/2, 1/4, 1/8, and 1/16 of the 48 kHz settings, respectively.

5 32 kHz, 44.1 kHz, and 48 kHz are the sampling rates used to scale the ratio calculations for the SSM6515. 88.2 kHz and 176.4 kHz are scaled as 1/2 and 1/4 of the 44.1 kHz settings, respectively.

STEREO (I^2S/LEFT JUSTIFIED) OPERATING MODE

Stereo modes use both edges of the FSYNC signal to determine placement of data. Stereo mode is enabled when SPT_SAI_MODE = 0, and the I^2S or left justified format is determined by the SPT_DATA_FORMAT register.

The I^2S or left justified formats accepts any number of BCLK cycles per FSYNC cycle as long as it is a supported BCLK rate.

Right justified operation can be achieved by using the delay by 8, 12, and 16 BCLK selections in the SPT_DATA_FORMAT register. The amount of delay to achieve this is dependent on the number of BCLK cycles per channel.

The SPT_SLOT_SEL register can select which channel of I^2S is routed to the DAC.

Sample rates from 8 kHz to 768 kHz are accepted.

TDM OPERATING MODE

The TDM operating mode allows more channels to use a single serial interface bus.

The FSYNC signal operates at the desired sample rate. A rising edge of the FSYNC signal indicates the start of a new frame.

Each chip on the TDM bus can occupy 16, 24, or 32 BCLK cycles. This is set with the SPT_SLOT_WIDTH register and all chips on the bus must have the same setting. Up to 32 SSM6515 chips can be used on a single TDM bus, but only four unique I^2C device addresses are available. The SSM6515 automatically determines how many possible chips can be placed on the bus from the BCLK rate. There is no limit to the total number of BCLK cycles per FSYNC pulse, except for the maximum 50 MHz frequency of BCLK.

The TDM slot data the SSM6515 device routes to the DAC is determined by the SPT_SLOT_SEL bits.

PDM OPERATING MODE

By setting the PDM_MODE bit to 1, the DAC can be driven with 1-bit PDM data on SDATAI. In this case, a 2.8224 MHz to 3.072 MHz, 5.6448 MHz to 6.144 MHz, or 11.2896 MHz to 12.288 MHz CLK must be provided on the BCLK pin. The frequency range is selected via the PDM_FS register.

PDM input data is latched on both edges of the clock. The PDM_CHAN_SEL register state determines which channel (CH0/CH1) is sent to the DAC.

The PDM_PHASE_SEL register determines which two edges of PDM_CLK are in phase, either falling then rising or rising then falling.

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The amount of filtering on the PDM signal, and consequently the input to output delay, is adjusted via the PDM_FILT register.

DIGITAL GAIN AND HIGH-PASS FILTER

There is a digital gain volume control in the DAC_VOL register that provides fine control in 0.375 dB steps from −70 dB to +24 dB. The volume control can be bypassed to save additional power. The volume control is bypassed by default. The DAC_VOL_MODE setting is used to bypass the volume control with fixed gain of either 0 dB or 6 dB or can enable the full selectable gain volume control. Note that any DAC_VOL_MODE setting made after this point overrides the fixed gain setting.

By default, the volume control ramps at a rate of 4.5 dB/ms and only updates to a new value after a zero crossing. The soft ramping can be disabled by setting DAC_HARD_VOL to 1. The zero crossing can be disabled such that the volume control change is instantaneous by setting DAC_VOL_ZC to 0.

Optional dc blocking is available and can be enabled via the DAC_HPF_EN register. By default, this filter is disabled for lowest power consumption. The corner frequency of this filter is variable and can be set via the DAC_HPF_FC register.

OUTPUT LIMITER AND CLIPPER

The SSM6515 includes a digital output limiter. The limiter follows the digital volume control in the signal chain. Therefore, the limiter accounts for the gain setting of the volume control. By default, this limiter is disabled to save power. It can be enabled by setting the LIM_EN bit in the power control register to 1.

This is a peak limiter and its threshold to which it limits the output is variable and set via the LIM_THRES register. Both the rate at which the gain is reduced (the attack rate) and the rate at which the gain is increased (the release rate) are determined by the LIM_RRT register and LIM_ATR register, respectively.

For example, the limiter threshold is set to 0 dB by default. This setting corresponds to 0 dB full-scale output, which is typically 1.15 V rms with 0 dBFS input at 1.8 V PVDD. If the volume control is set to 0 dB and the limiter threshold is set to −10 dB, the limiter activates at and above −10 dBFS input. That is, the output is limited to −10 dB full scale (0.363 V rms).

If the volume control is set to 3 dB gain, the limiter activates at and above −13 dBFS input, and the output is limited to −10 dB full scale (0.363 V rms).

The SSM6515 output can also be digitally clipped, if desired, at a level below the full-scale output. Clipping is symmetrical on both the positive and negative output swings. The level at which clipping occurs is determined by the DAC_HF_CLIP register. By default, the clipper is set to 0 dB, which corresponds to no digital clipping.

The limiter block also offers the attack and release rate controls. The attack rate is defined in µs/dB, whereas the release rate is defined in ms/dB. For example, the attack rate determines the attack time required for the limiter to start limiting the output when above a set threshold. If the limiter threshold is set to −10 dB, with an attack rate of 120 µs/dB and a release rate of 1600 ms/dB, and the signal exceeds 5 dB above threshold or −5 dBFS, the limiter takes approximately 120 µs/dB × 5 dB = 600 µs to start limiting the output to −10 dB full scale. Similarly, the release rate determines if the limiter releases the gain reduction when the input level falls below the set threshold, such as −15 dBFS. Therefore, the limiter releases the output in 1600 ms/dB × 5 dB = 8 sec to −15 dB full scale.

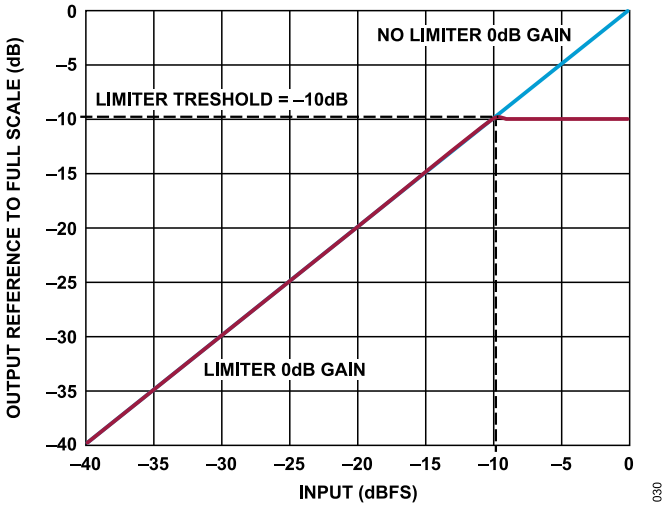


Figure 30. Output Reference to Full Scale vs. Input, 0 dB Gain

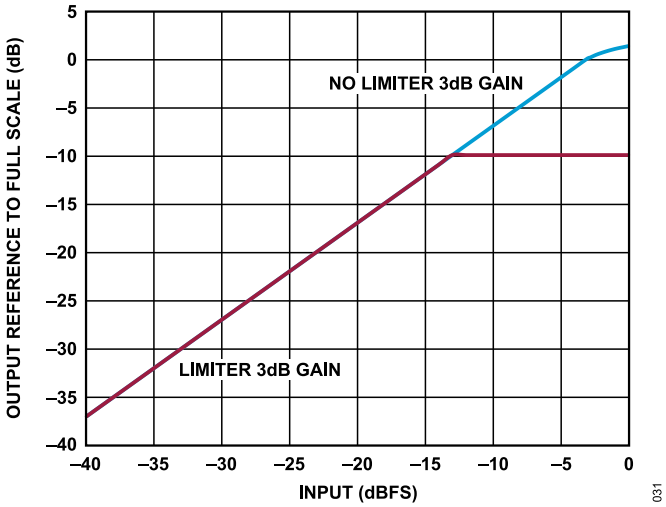


Figure 31. Output Reference to Full Scale vs. Input, 3 dB Gain

FAULTS AND STATUS

The SSM6515 includes fault detection, protection, and status reporting for amplifier over current fault, overtemperature fault, and PVDD undervoltage fault. The device also detects and status reports incorrect clocking ratios, incorrect serial port inputs, and an

THEORY OF OPERATION

overtemperature warning. There is also status reporting for DAC clipping and when the limiter actively reduces the gain.

The SSM6515 short detection detects an output short to GND or PVDD, setting the OCP bit, and turning off the outputs. However, if OUT+ and OUT− are shorted together, there can be instances where OCP is not triggered and significant PVDD current of several hundred mA is consumed. If it is necessary to protect against an OUT+/OUT− short, system level protection is recommended.

The reporting of all of these events are in the read-only STATUS register. When any of these events occur, the respective status bits remain set to 1, even if the event is no longer active. The STATUS bits can be cleared by writing a 1 to the STATUS_CLEAR register.

Note that the only exception is the OTW bit, which self clears when the temperature drops back below the warning threshold.

POP AND CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Clicks and pops are defined as undesirable audible transients, generated by the amplifier system, that do not come from the system input signal.

Such transients can be generated when the amplifier system changes its operating mode. For example, system power-up and power-down can be sources of audible transients.

The SSM6515 has an advanced pop and click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

It is best to power down via the SPWDN control and wait for the power-down sequence to complete before the BCLK signal is removed to ensure the most pop free power-down.

EMI CONTROL

The SSM6515 uses a proprietary common-mode stable output switching, modulation, and spread spectrum technology to minimize EMI emissions from the device. The SSM6515 produces lower emission levels than other filterless Class-D topologies. The SSM6515 includes an extra EMI emissions control mode that significantly reduces the radiated emissions at the Class-D outputs, particularly above 30 MHz. The output slew rate control is provided in Register 0x0E. By default, normal mode is enabled, but to reduce the emissions, this bit can be set to low EMI mode.

The distance of the amplifier to speaker also decides the radiated emissions from the board or cable. For speaker cable lengths <4", no extra filter components are needed. For longer speaker cable lengths, the ferrite bead and 100 pF capacitor filter can be used to reduce the emissions. See Figure 40.

OUTPUT MODULATION DESCRIPTION

The SSM6515 uses common-mode stable, three-level, Σ-Δ output modulation. See Figure 32, Figure 33, and Figure 34.

The waveforms at the OUT+ and OUT− balls, as shown in the figures. The DIFF OUT waveform is a differential voltage measured across the speaker output (that is, OUT+ to OUT−).

Both OUT+ and OUT− stay at PVDD/2 under no signal or idle conditions, but due to the constant presence of noise in the system, a differential pulse is occasionally generated in response to this stimulus (see Figure 32). OUT+ goes to PVDD and OUT− goes to 0 V, or vice versa. This creates the differential voltage across the speaker load either going to PVDD or to −PVDD. See the DIFF OUT waveform. Typically, the output differential pulse is small (40.69 ns). Therefore, only a small amount of current flows into the inductive load when this differential pulse is generated. This feature ensures that the current flowing through the inductive load is small and also reduces the idle current draw from the power supply.

When the user sends an input signal, an output pulse is generated to follow the input voltage. The differential pulse density, as well as pulse width, is increased by raising the input signal level. Figure 33 and Figure 34 depict three-level, Σ-Δ output modulation with an +ve and −ve input stimulus.

The pulse width increases or decreases the differential voltage across the speaker terminal creating positive or negative signals.

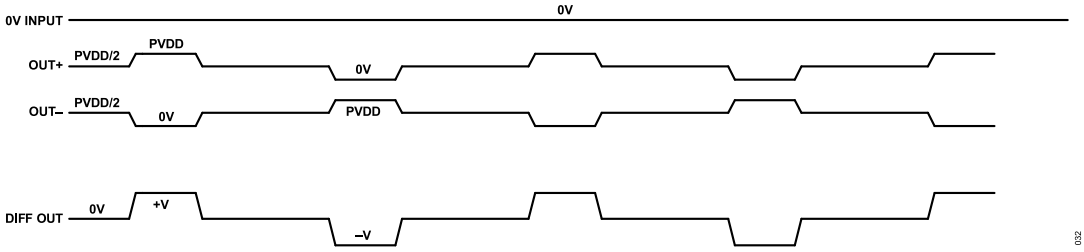


Figure 32. Idle Mode, Three-Level, Σ-Δ Output Modulation

THEORY OF OPERATION

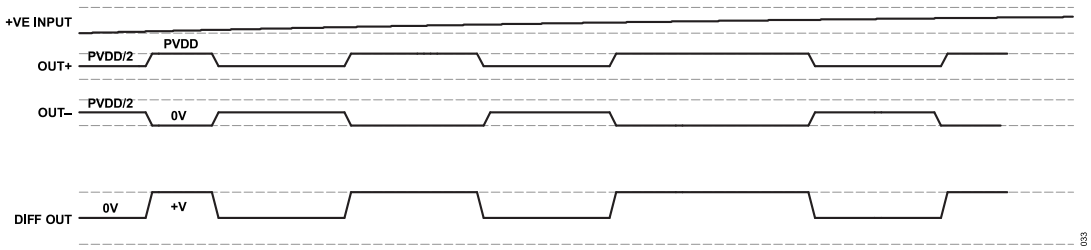


Figure 33. Positive Output, Three-Level, Σ-Δ Output Modulation

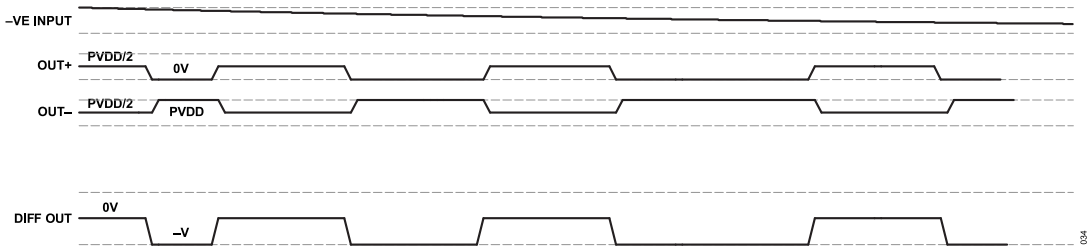


Figure 34. Negative Output, Three-Level, Σ-Δ Output Modulation

OUTPUT LOAD

The load presented to the output pins of the SSM6515 must meet the minimum dc resistance and inductance requirements to ensure that power and performance specifications are met. In addition, the output resistive load can be set via the AMP_RLOAD register. This register setting can optimize the amplifier power stage for the given load.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The PVDD power supply input must be decoupled with a 1 nF, X7R, low equivalent series resistance (ESR), multilayer ceramic capacitor (MLCC) that works as a high frequency decoupling capacitor. Place the capacitor as close as possible to the PVDD and GND pins of the device. The larger bulk bypass capacitor must be available near the 1.8 V output in the system. This bulk capacitor is 10 µF, and electrolytic or MLCC types are acceptable. This capacitor helps provide the current needed at low frequencies.

LAYOUT

PVDD and GND carry the device current and must be properly decoupled with capacitors close to the device power supply and ground pins.

Properly designed multilayer PCBs can reduce electromagnetic emission and improve RF immunity compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal traces.

I²C CONTROL

The SSM6515 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, SDA and SCL, carry information between the SSM6515 and the system I²C master controller. The SSM6515 is always a slave on the bus, meaning it cannot initiate a data transfer. Each slave device is recognized by a unique address. Using the ADDR pin provides the four device addresses, which are listed in Table 14. The address byte format is shown in Table 15. The address resides in the first seven bits of the I²C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Connect 2.2 kΩ pull-up resistors on the lines connected to the SDA and SCL pins. The voltage on these signal lines must not be more than 1.98 V.

Table 14. ADDR Pin to I²C Device Address Mapping

ADDR Pin	I²C Address Bit 2	I²C Address Bit 1
GND	0	0
Pull-Down 47 kΩ Resistor	0	1
Open	1	0
Pull-Up 47 kΩ Resistor	1	1
PVDD	Not applicable	Not applicable

Table 15. I²C Device Address Byte Format Using the ADDR Pin

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	1	ADDR1	ADDR0	R/$\overline{W}$

THEORY OF OPERATION

Addressing

Initially, each device on the I^{2}C bus is in an idle state, monitoring the SDA and SCL lines for a start condition and the proper address. The I^{2}C master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCL remains high. This transition indicates that an address or data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is an acknowledge (ACK) bit. All other devices withdraw from the bus at this point and return to the idle condition. The device address for the SSM6515 is determined by the state of the ADDR pin. See Table 14 for four available addresses.

The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means the master writes information to the peripheral, whereas a Logic 1 means that the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer occurs until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. The timing for the I^{2}C port is shown in Figure 35.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the SSM6515 immediately jumps to the idle condition. During a given SCL high period, the user must issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If the user issues an invalid subaddress, the SSM6515 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken.

In read mode, the SSM6515 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition is when the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the SSM6515, and the device returns to the idle condition.

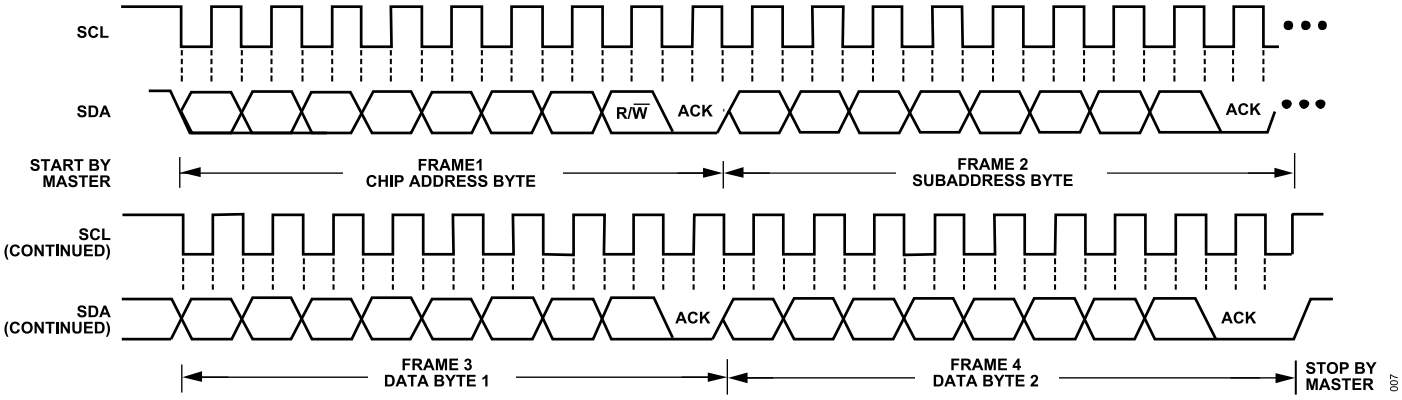


Figure 35. I^{2}C Read/Write Timing

THEORY OF OPERATION

I²C Read and Write Operations

Figure 36 shows the timing of a single-word write operation. Every ninth clock, the SSM6515 issues an acknowledge by pulling SDA low.

Figure 37 shows the timing of a burst mode write sequence. Figure 37 shows an example in which the target destination registers are two bytes. The SSM6515 increments its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

The timing of a single word read operation is shown in Figure 38. The first R/$\overline{W}$ bit is 0, indicating a write operation followed by the subaddress of the register to be read. After the SSM6515 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). The SSM6515 acknowledges and puts 8-bit data on the SDA pin. The master then responds every ninth pulse with an acknowledge pulse to the SSM6515.

Figure 36 through Figure 39 use the following abbreviations:

- S is the start bit
- P is the stop bit
- A_M is the acknowledge by master
- A_S is the acknowledge by slave

START BIT	I²C ADDRESS (7 BITS)	R/$\overline{W}$ = 0	ACK BY SLAVE	SUBADDRESS (8 BITS)	ACK BY SLAVE	DATA BYTE 1 (8 BITS)	STOP BIT

008

Figure 36. Single Word I²C Write Format

S	CHIP ADDRESS, R/$\overline{W}$ = 0	A_S	SUBADDRESS	A_S	DATA WORD 1	A_S	DATA WORD 2	A_S	• • •	P

009

Figure 37. Burst Mode I²C Write Format

S	CHIP ADDRESS, R/$\overline{W}$ = 0	A_S	SUBADDRESS	A_S	S	CHIP ADDRESS, R/$\overline{W}$ = 1	A_S	DATA WORD 1	A_M	DATA BYTE N	P

010

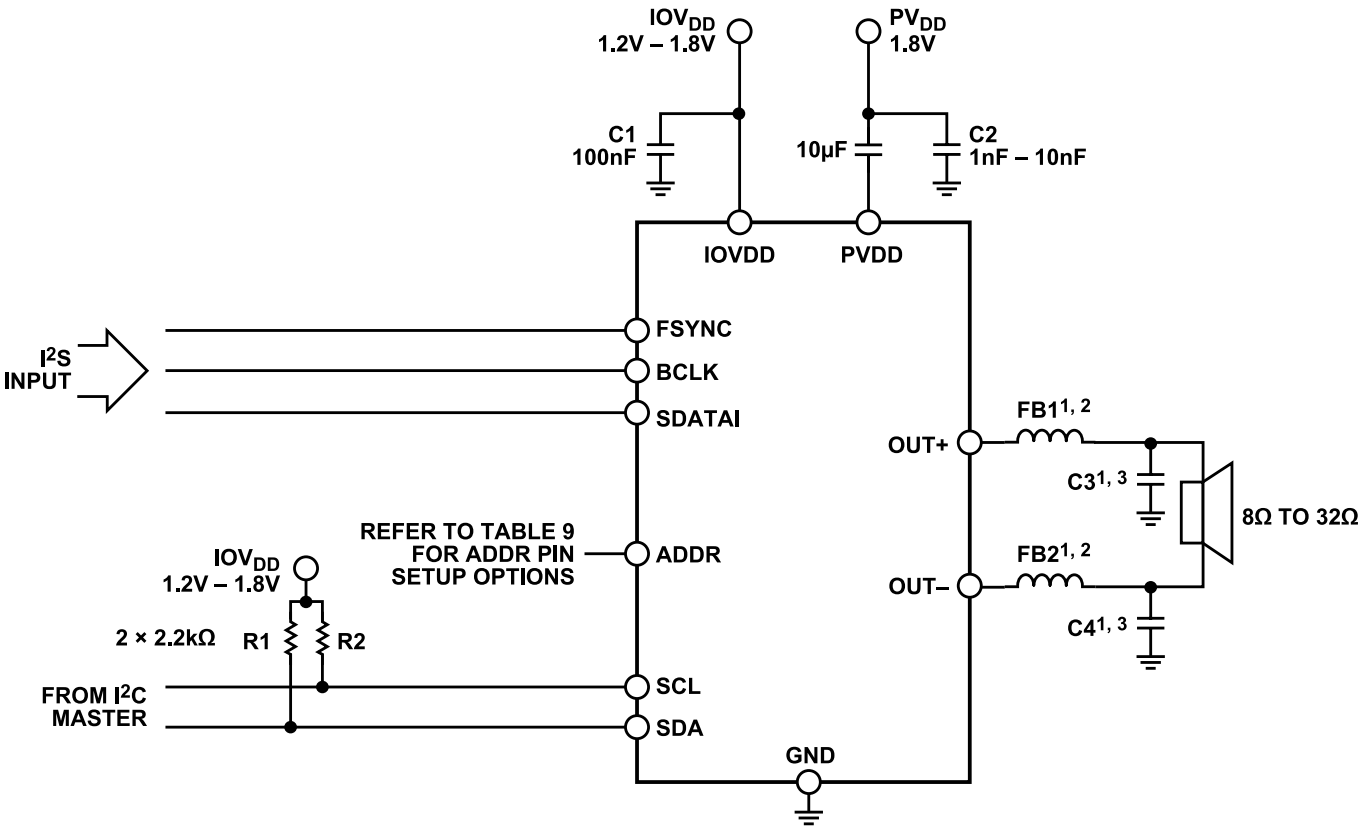
Figure 38. Single Word I²C Read Format

S	CHIP ADDRESS, R/$\overline{W}$ = 0	A_S	SUBADDRESS	A_S	S	CHIP ADDRESS, R/$\overline{W}$ = 1	A_S	DATA WORD 1	A_M	• • •	P

011

Figure 39. Burst Mode I²C Read Format

TYPICAL APPLICATION CIRCUIT



[1]FB1, FB2, C3, C4 CAN BE USED FOR SPEAKER CABLE LENGTHS >4 INCHES
[2]FB1, FB2: TDK MAF1005xxx
[3]C3, C4: 100pF, MLCC

Figure 40. Typical Application Circuit, I²S Mode and I²C Mode

APPLICATIONS INFORMATION

Figure 40 shows the typical application for a single channel using I^2S/TDM input and I^2C control. The PV_{DD} voltage is supplied externally.

The digital input data can be 2-channel I^2S or multichannel TDM format, and the desired format must be selected in the SAI control registers. Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section for more details. Alternatively, the input can be 1-bit PDM data (see the PDM Operating Mode section).

On power-up, the device stays in power-down unless in standalone mode. To enable the amplifier, the SPWDN bit must be set to 0. Once this bit is set to 0, the amplifier turns on and the output starts switching.

The device can be reset to default settings by writing 1 to the SOFT_FULL_RST. The device can be reset while maintaining register settings by writing 1 to SOFT_RST.

By default, the high-pass filter is disabled for the lowest power consumption and lowest latency. The high-pass filter can be enabled by setting the DAC_HPF_EN register to 1.

The fault status register, 0x13, can be read to check for any fault conditions during operation.

REGISTER SUMMARY: I²C REGISTER MAP

Table 16. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	VENDOR_ID	[7:0]	VENDOR								0x41	R
0x01	DEVICE_ID1	[7:0]	DEVICE1								0x65	R
0x02	DEVICE_ID2	[7:0]	DEVICE2								0x15	R
0x03	REVISION	[7:0]	REV								0x02	R
0x04	PWR_CTRL	[7:0]	RESERVED			LIM_EN	RESERVED		APWDN_EN	SPWDN	0x01	R/W
0x05	CLK_CTRL	[7:0]	RESERVED			BCLK_RATE					0x00	R/W
0x06	PDM_CTRL	[7:0]	PDM_PHASE_SEL	RESERVED	PDM_FILT		PDM_CHAN_SEL	PDM_FS		PDM_MODE	0x20	R/W
0x07	DAC_CTRL1	[7:0]	DAC_IBIAS		DAC_PWR_MODE		DAC_FS				0x15	R/W
0x08	DAC_CTRL2	[7:0]	DAC_INVERT	DAC_PERF_MODE	DAC_HARD_VOL	DAC_VOL_ZC	DAC_MORE_FILT	DAC_VOL_MODE		DAC_MUTE	0x13	R/W
0x09	DAC_CTRL3	[7:0]	DAC_HPF_FC				RESERVED			DAC_HPF_EN	0xD0	R/W
0x0A	DAC_VOL	[7:0]	DAC_VOL								0x40	R/W
0x0B	DAC_CLIP	[7:0]	DAC_HF_CLIP								0xFF	R/W
0x0C	SPT_CTRL1	[7:0]	SPT_LRCLK_POL	SPT_BCLK_POL	SPT_SLOT_WIDTH		SPT_DATA_FORMAT			SPT_SAI_MODE	0x00	R/W
0x0D	SPT_CTRL2	[7:0]	RESERVED			SPT_SLOT_SEL					0x00	R/W
0x0E	AMP_CTRL	[7:0]	RESERVED			OCP_EN	AMP_RLOAD		EMI_MODE	AMP_LPM	0x14	R/W
0x0F	LIM_CTRL	[7:0]	RESERVED		LIM_RRT		RESERVED		LIM_ATR		0x22	R/W
0x10	LIM_CTRL2	[7:0]	RESERVED			LIM_THRES					0x0A	R/W
0x11	FAULT_CTRL	[7:0]	RESERVED			MRCV	RESERVED	ARCV_UVLO	ARCV_OTF	ARCV_OCP	0x00	R/W
0x12	STATUS_CLR	[7:0]	RESERVED							STAT_CLR	0x00	R/W
0x13	STATUS	[7:0]	LIM_EG	CLIP	SPT_ERR	CLK_ERR	UVLO	OTW	OTF	OCP	0x00	R
0x14	RESET	[7:0]	RESERVED			SOFT_FULL_RESET	RESERVED			SOFT_RESET	0x00	W

REGISTER DETAILS: I²C REGISTER MAP

VENDOR ID REGISTER

Address: 0x00, Reset: 0x41, Name: VENDOR_ID

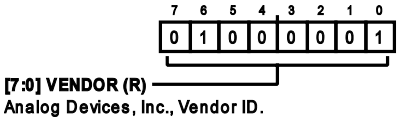


Table 17. Bit Descriptions for VENDOR_ID

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR	Analog Devices, Inc., Vendor ID.	0x41	R

DEVICE ID REGISTER

Address: 0x01, Reset: 0x65, Name: DEVICE_ID1

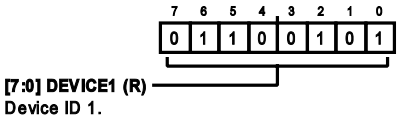


Table 18. Bit Descriptions for DEVICE_ID1

Bits	Bit Name	Description	Reset	Access
[7:0]	DEVICE1	Device ID 1.	0x65	R

Address: 0x02, Reset: 0x15, Name: DEVICE_ID2

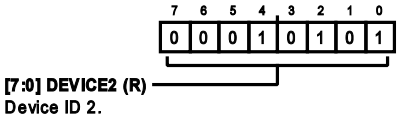


Table 19. Bit Descriptions for DEVICE_ID2

Bits	Bit Name	Description	Reset	Access
[7:0]	DEVICE2	Device ID 2.	0x15	R

REVISION CODE REGISTER

Address: 0x03, Reset: 0x02, Name: REVISION

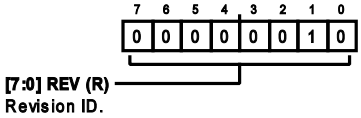


Table 20. Bit Descriptions for REVISION

Bits	Bit Name	Description	Reset	Access
[7:0]	REV	Revision ID.	0x2	R

REGISTER DETAILS: I²C REGISTER MAP

MASTER AND BLOCK POWER CONTROL REGISTER

Address: 0x04, Reset: 0x01, Name: PWR_CTRL

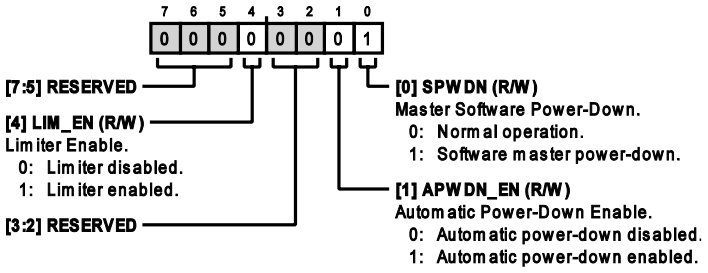
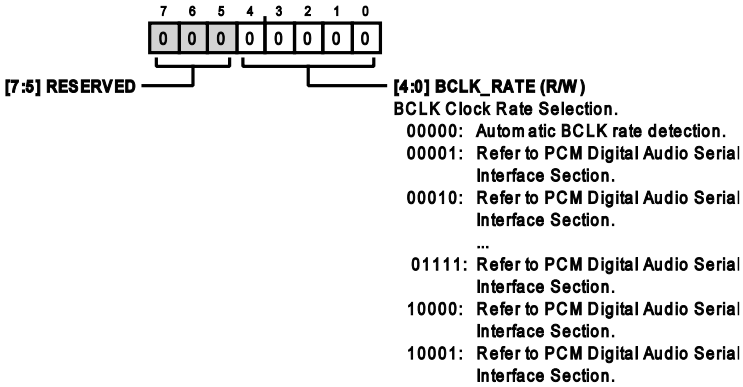


Table 21. Bit Descriptions for PWR_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	LIM_EN		Limiter Enable.	0x0	R/W
		0	Limiter disabled.		
		1	Limiter enabled.		
[3:2]	RESERVED		Reserved.	0x0	R
1	APWDN_EN		Automatic Power-Down Enable. Automatic power-down automatically puts the IC in a low power state when 2048 consecutive zero input samples are received.	0x0	R/W
		0	Automatic power-down disabled.		
		1	Automatic power-down enabled.		
0	SPWDN		Master Software Power-Down. Software power-down puts all blocks except the I²C interface in a low power state.	0x1	R/W
		0	Normal operation.		
		1	Software master power-down.		

BCLK RATE CONTROL REGISTER

Address: 0x05, Reset: 0x00, Name: CLK_CTRL



REGISTER DETAILS: I²C REGISTER MAP

Table 22. Bit Descriptions for CLK_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	BCLK_RATE		BCLK Clock Rate Selection.	0x0	R/W
		00000	Automatic BCLK rate detection.		
		00001	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		00010	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		00011	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		00100	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		00101	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		00110	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		00111	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01000	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01001	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01010	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01011	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01100	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01101	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01110	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		01111	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		10000	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		
		10001	Refer to the Pulse Code Modulation (PCM) Digital Audio Serial Interface section.		

PDM CONTROL REGISTER

Address: 0x06, Reset: 0x20, Name: PDM_CTRL

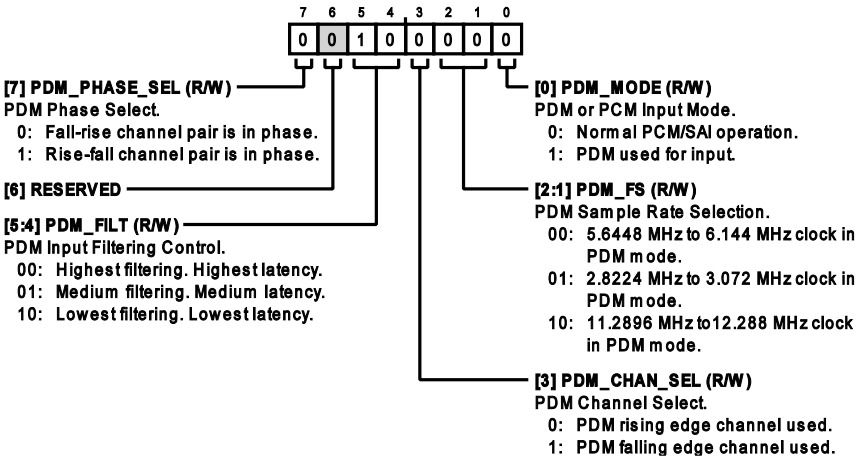


Table 23. Bit Descriptions for PDM_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	PDM_PHASE_SEL		PDM Phase Select.	0x0	R/W
		0	Fall-rise channel pair is in phase.		
		1	Rise-fall channel pair is in phase.		
6	RESERVED		Reserved.	0x0	R

REGISTER DETAILS: I²C REGISTER MAP

Table 23. Bit Descriptions for PDM_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[5:4]	PDM_FILT		PDM Input Filtering Control.	0x2	R/W
		00	Highest filtering. Highest latency.		
		01	Medium filtering. Medium latency.		
		10	Lowest filtering. Lowest latency.		
3	PDM_CHAN_SEL		PDM Channel Select.	0x0	R/W
		0	PDM rising edge channel used.		
		1	PDM falling edge channel used.		
[2:1]	PDM_FS		PDM Sample Rate Selection.	0x0	R/W
		00	5.6448 MHz to 6.144 MHz clock in PDM mode.		
		01	2.8224 MHz to 3.072 MHz clock in PDM mode.		
		10	11.2896 MHz to 12.288 MHz clock in PDM mode.		
0	PDM_MODE		PDM or PCM Input Mode.	0x0	R/W
		0	Normal PCM/SAI operation.		
		1	PDM used for input.		

DAC SAMPLE RATE, POWER MODES, FILTERING CONTROLS REGISTER

Address: 0x07, Reset: 0x15, Name: DAC_CTRL1

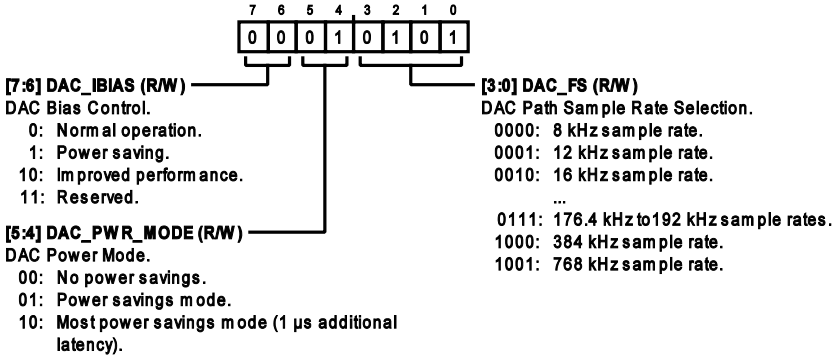


Table 24. Bit Descriptions for DAC_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	DAC_IBIAS		DAC Bias Control.	0x0	R/W
		0	Normal operation.		
		1	Power saving.		
		10	Improved performance.		
		11	Reserved.		
[5:4]	DAC_PWR_MODE		DAC Power Mode.	0x1	R/W
		00	No power savings.		
		01	Power savings mode.		
		10	Most power savings mode (1 µs additional latency).		
[3:0]	DAC_FS		DAC Path Sample Rate Selection.	0x5	R/W
		0000	8 kHz sample rate.		
		0001	12 kHz sample rate.		
		0010	16 kHz sample rate.		

REGISTER DETAILS: I²C REGISTER MAP

Table 24. Bit Descriptions for DAC_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
		0011	24 kHz sample rate.		
		0100	32 kHz sample rate.		
		0101	44.1 kHz to 48 kHz sample rates.		
		0110	88.2 kHz to 96 kHz sample rates.		
		0111	176.4 kHz to 192 kHz sample rates.		
		1000	384 kHz sample rate.		
		1001	768 kHz sample rate.		

DAC MUTE AND VOLUME OPTIONS REGISTER

Address: 0x08, Reset: 0x13, Name: DAC_CTRL2

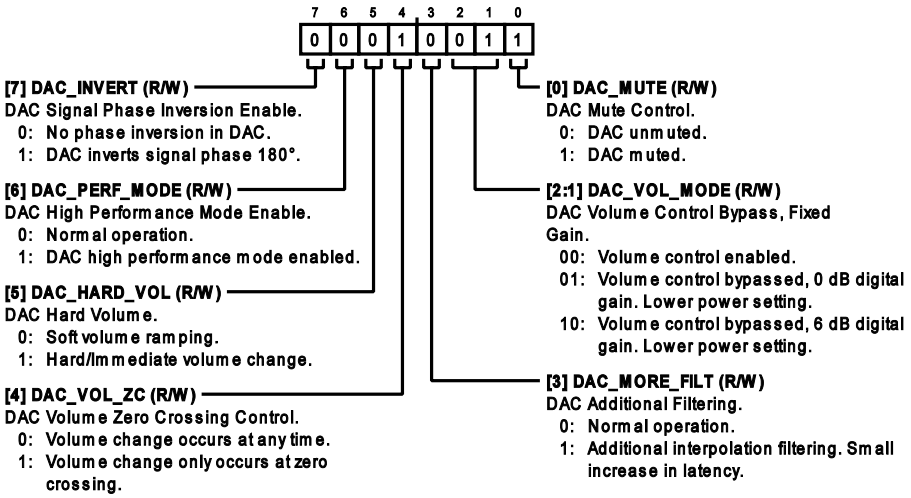


Table 25. Bit Descriptions for DAC_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC_INVERT		DAC Signal Phase Inversion Enable.	0x0	R/W
		0	No phase inversion in DAC.		
		1	DAC inverts signal phase 180°.		
6	DAC_PERF_MODE		DAC High Performance Mode Enable.	0x0	R/W
		0	Normal operation.		
		1	DAC high performance mode enabled.		
5	DAC_HARD_VOL		DAC Hard Volume.	0x0	R/W
		0	Soft volume ramping.		
		1	Hard/immediate volume change.		
4	DAC_VOL_ZC		DAC Volume Zero Crossing Control.	0x1	R/W
		0	Volume change occurs at any time.		
		1	Volume change occurs only at zero crossing.		
3	DAC_MORE_FILT		DAC Additional Filtering.	0x0	R/W
		0	Normal operation.		
		1	Additional interpolation filtering. Small increase in latency.		

REGISTER DETAILS: I²C REGISTER MAP

Table 25. Bit Descriptions for DAC_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[2:1]	DAC_VOL_MODE		DAC Volume Control Bypass, Fixed Gain.	0x1	R/W
		00	Volume control enabled.		
		01	Volume control bypassed, 0 dB digital gain. Lower power setting.		
		10	Volume control bypassed, 6 dB digital gain. Lower power setting.		
0	DAC_MUTE		DAC Mute Control.	0x1	R/W
		0	DAC unmuted.		
		1	DAC muted.		

DAC HIGH-PASS FILTER CONTROLS REGISTER

Address: 0x09, Reset: 0xD0, Name: DAC_CTRL3

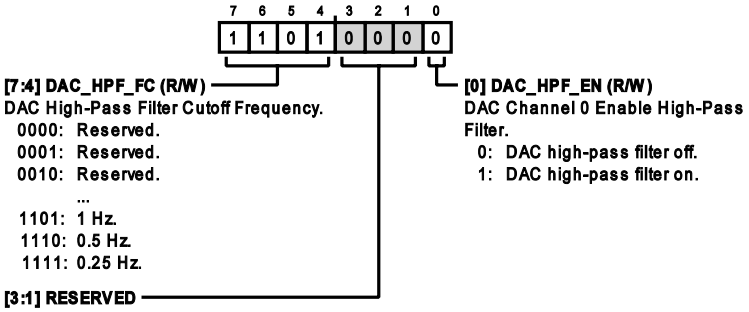


Table 26. Bit Descriptions for DAC_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	DAC_HPF_FC		DAC High-Pass Filter Cutoff Frequency.	0xD	R/W
		0000	Reserved.		
		0001	Reserved.		
		0010	Reserved.		
		0011	Reserved.		
		0100	Reserved.		
		0101	241 Hz.		
		0110	120 Hz.		
		0111	60 Hz.		
		1000	30 Hz.		
		1001	15 Hz.		
		1010	7 Hz.		
		1011	4 Hz.		
		1100	2 Hz.		
		1101	1 Hz.		
		1110	0.5 Hz.		
		1111	0.25 Hz.		
[3:1]	RESERVED		Reserved.	0x0	R
0	DAC_HPF_EN		DAC Channel 0 Enable High-Pass Filter.	0x0	R/W
		0	DAC high-pass filter off.		
		1	DAC high-pass filter on.		

REGISTER DETAILS: I²C REGISTER MAP

DAC VOLUME CONTROL REGISTER

Address: 0x0A, Reset: 0x40, Name: DAC_VOL

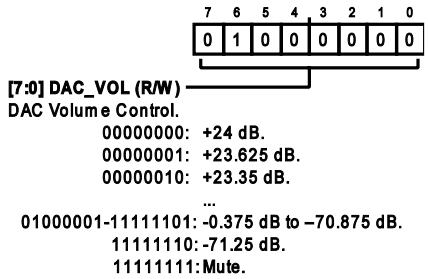


Table 27. Bit Descriptions for DAC_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC_VOL		DAC Volume Control.	0x40	R/W
		00000000	+24 dB.		
		00000001	+23.625 dB.		
		00000010	+23.35 dB.		
		00000011	+22.875 dB.		
		00000100 to 00111111	+22.5 dB to +0.375 dB.		
		01000000	0 dB.		
		01000001 to 11111101	−0.375 dB to −70.875 dB.		
		11111110	−71.25 dB.		
		11111111	Mute.		

DAC CLIPPER CONTROL REGISTER

Address: 0x0B, Reset: 0xFF, Name: DAC_CLIP

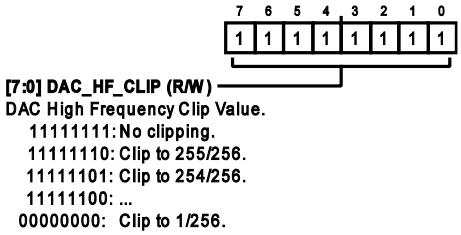


Table 28. Bit Descriptions for DAC_CLIP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC_HF_CLIP		DAC High Frequency Clip Value.	0xFF	R/W
		11111111	No clipping.		
		11111110	Clip to 255/256.		
		11111101	Clip to 254/256.		
		11111100	…		
		00000000	Clip to 1/256.		

REGISTER DETAILS: I²C REGISTER MAP

SERIAL AUDIO PORT SETTINGS REGISTER

Address: 0x0C, Reset: 0x00, Name: SPT_CTRL1

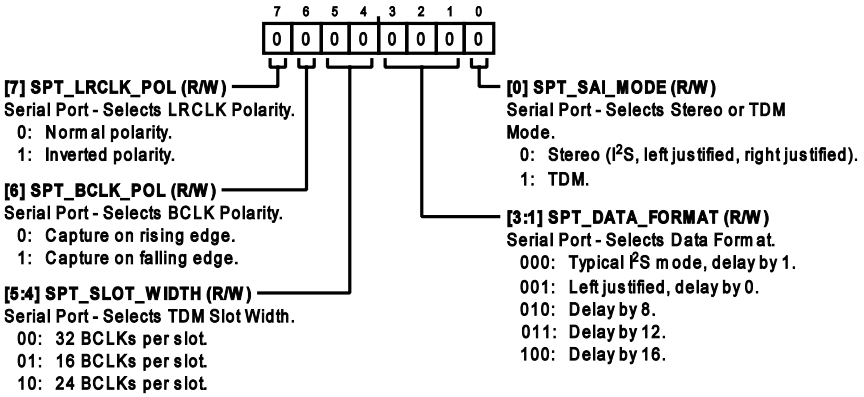


Table 29. Bit Descriptions for SPT_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	SPT_LRCLK_POL		Serial Port–Selects LRCLK Polarity.	0x0	R/W
		0	Normal polarity.		
		1	Inverted polarity.		
6	SPT_BCLK_POL		Serial Port–Selects BCLK Polarity.	0x0	R/W
		0	Capture on rising edge.		
		1	Capture on falling edge.		
[5:4]	SPT_SLOT_WIDTH		Serial Port–Selects TDM Slot Width.	0x0	R/W
		00	32 BCLKs per slot.		
		01	16 BCLKs per slot.		
		10	24 BCLKs per slot.		
[3:1]	SPT_DATA_FORMAT		Serial Port–Selects Data Format.	0x0	R/W
		000	Typical I²S mode, delay by 1.		
		001	Left justified, delay by 0.		
		010	Delay by 8.		
		011	Delay by 12.		
		100	Delay by 16.		
0	SPT_SAI_MODE		Serial Port–Selects Stereo or TDM Mode.	0x0	R/W
		0	Stereo (I²S, left justified, right justified).		
		1	TDM.		

REGISTER DETAILS: I²C REGISTER MAP

SERIAL AUDIO PORT SLOT SELECTION REGISTER

Address: 0x0D, Reset: 0x00, Name: SPT_CTRL2

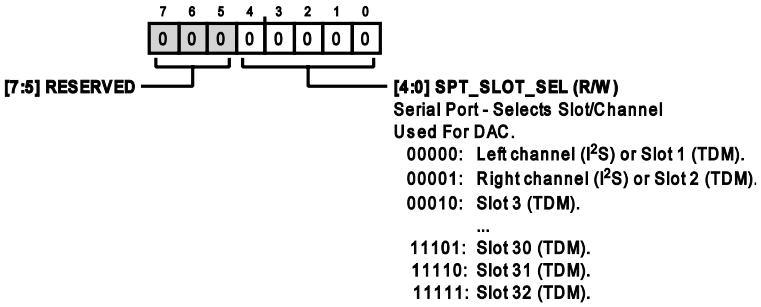


Table 30. Bit Descriptions for SPT_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	SPT_SLOT_SEL		Serial Port–Selects Slot/Channel Used For DAC.	0x0	R/W
		00000	Left channel (I²S) or Slot 1 (TDM).		
		00001	Right channel (I²S) or Slot 2 (TDM).		
		00010	Slot 3 (TDM).		
		00011	Slot 4 (TDM).		
		00100	Slot 5 (TDM).		
		00101	Slot 6 (TDM).		
		00110	Slot 7 (TDM).		
		00111	Slot 8 (TDM).		
		01000	Slot 9 (TDM).		
		01001	Slot 10 (TDM).		
		01010	Slot 11 (TDM).		
		01011	Slot 12 (TDM).		
		01100	Slot 13 (TDM).		
		01101	Slot 14 (TDM).		
		01110	Slot 15 (TDM).		
		01111	Slot 16 (TDM).		
		10000	Slot 17 (TDM).		
		10001	Slot 18 (TDM).		
		10010	Slot 19 (TDM).		
		10011	Slot 20 (TDM).		
		10100	Slot 21 (TDM).		
		10101	Slot 22 (TDM).		
		10110	Slot 23 (TDM).		
		10111	Slot 24 (TDM).		
		11000	Slot 25 (TDM).		
		11001	Slot 26 (TDM).		
		11010	Slot 27 (TDM).		
		11011	Slot 28 (TDM).		
		11100	Slot 29 (TDM).		

REGISTER DETAILS: I²C REGISTER MAP

Table 30. Bit Descriptions for SPT_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
		11101	Slot 30 (TDM).		
		11110	Slot 31 (TDM).		
		11111	Slot 32 (TDM).		

AMPLIFIER CONTROLS REGISTER

Address: 0x0E, Reset: 0x14, Name: AMP_CTRL

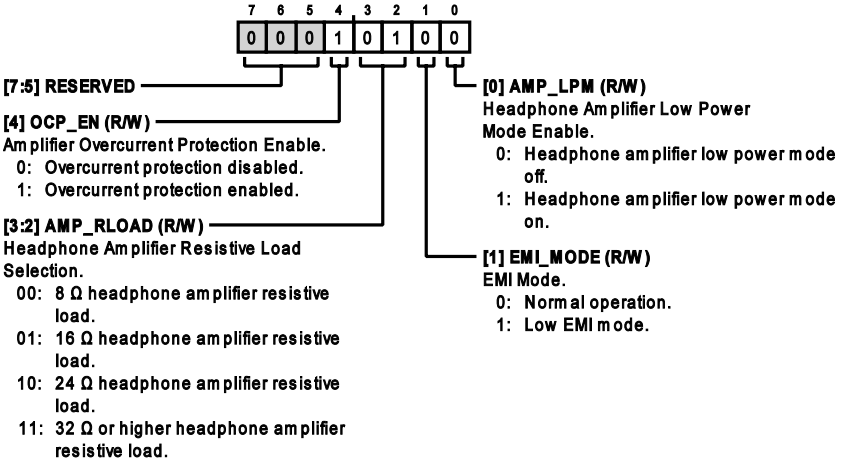


Table 31. Bit Descriptions for AMP_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	OCP_EN		Amplifier Overcurrent Protection Enable.	0x1	R/W
		0	Overcurrent protection disabled.		
		1	Overcurrent protection enabled.		
[3:2]	AMP_RLOAD		Headphone Amplifier Resistive Load Selection.	0x1	R/W
		00	8 Ω headphone amplifier resistive load.		
		01	16 Ω headphone amplifier resistive load.		
		10	24 Ω headphone amplifier resistive load.		
		11	32 Ω or higher headphone amplifier resistive load.		
1	EMI_MODE		EMI Mode.	0x0	R/W
		0	Normal operation.		
		1	Low EMI mode.		
0	AMP_LPM		Headphone Amplifier Low Power Mode Enable.	0x0	R/W
		0	Headphone amplifier low power mode off.		
		1	Headphone amplifier low power mode on.		

REGISTER DETAILS: I²C REGISTER MAP

AUDIO OUTPUT LIMITER ATTACK AND RELEASE RATE CONTROLS REGISTER

Address: 0x0F, Reset: 0x22, Name: LIM_CTRL

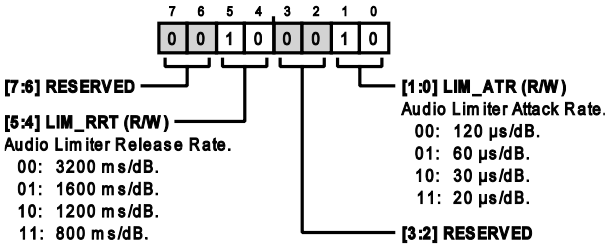


Table 32. Bit Descriptions for LIM_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	LIM_RRT		Audio Limiter Release Rate.	0x2	R/W
		00	3200 ms/dB.		
		01	1600 ms/dB.		
		10	1200 ms/dB.		
		11	800 ms/dB.		
[3:2]	RESERVED		Reserved.	0x0	R
[1:0]	LIM_ATR		Audio Limiter Attack Rate.	0x2	R/W
		00	120 µs/dB.		
		01	60 µs/dB.		
		10	30 µs/dB.		
		11	20 µs/dB.		

AUDIO OUTPUT LIMITER THRESHOLD CONTROL REGISTER

Address: 0x10, Reset: 0x0A, Name: LIM_CTRL2

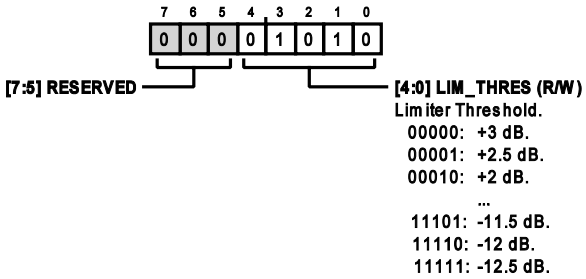


Table 33. Bit Descriptions for LIM_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	LIM_THRES		Limiter Threshold.	0xA	R/W
		00000	+3 dB.		
		00001	+2.5 dB.		
		00010	+2 dB.		
		00011	+1.5 dB.		
		00100	+1 dB.		

REGISTER DETAILS: I²C REGISTER MAP

Table 33. Bit Descriptions for LIM_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
		00101	+0.5 dB.		
		00110	0 dB.		
		00111	−0.5 dB.		
		01000	−1 dB.		
		01001	−1.5 dB.		
		01010	−2 dB.		
		01011	−2.5 dB.		
		01100	−3 dB.		
		01101	−3.5 dB.		
		01110	−4 dB.		
		01111	−4.5 dB.		
		10000	−5 dB.		
		10001	−5.5 dB.		
		10010	−6 dB.		
		10011	−6.5 dB.		
		10100	−7 dB.		
		10101	−7.5 dB.		
		10110	−8 dB.		
		10111	−8.5 dB.		
		11000	−9 dB.		
		11001	−9.5 dB.		
		11010	−10 dB.		
		11011	−10.5 dB.		
		11100	−11 dB.		
		11101	−11.5 dB.		
		11110	−12 dB.		
		11111	−12.5 dB.		

REGISTER DETAILS: I²C REGISTER MAP

FAULT CONTROL REGISTER

Address: 0x11, Reset: 0x00, Name: FAULT_CTRL

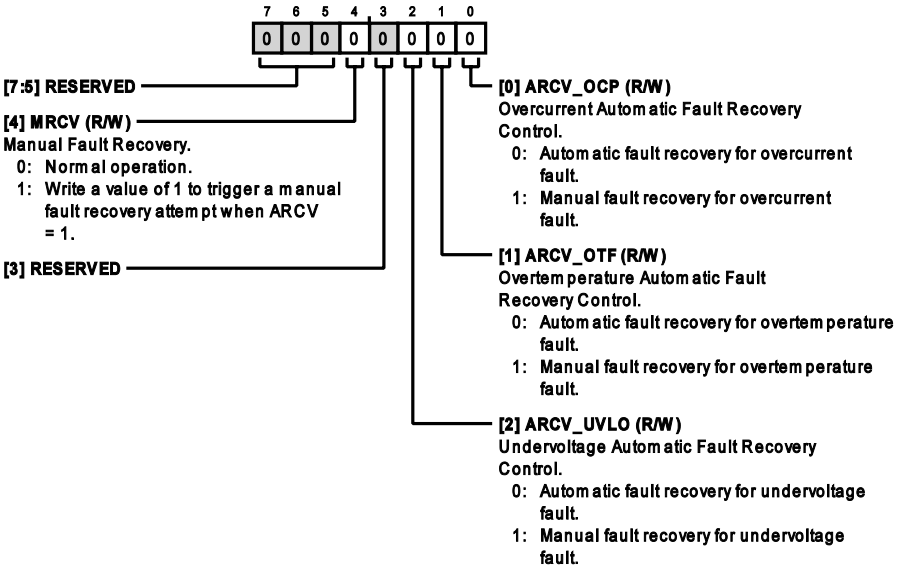


Table 34. Bit Descriptions for FAULT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	MRCV		Manual Fault Recovery.	0x0	R/W
		0	Normal operation.		
		1	Write a value of 1 to trigger a manual fault recovery attempt when ARCV = 1.		
3	RESERVED		Reserved.	0x0	R
2	ARCV_UVLO		Undervoltage Automatic Fault Recovery Control.	0x0	R/W
		0	Automatic fault recovery for undervoltage fault.		
		1	Manual fault recovery for undervoltage fault.		
1	ARCV_OTF		Overtemperature Automatic Fault Recovery Control.	0x0	R/W
		0	Automatic fault recovery for overtemperature fault.		
		1	Manual fault recovery for overtemperature fault.		
0	ARCV_OCP		Overcurrent Automatic Fault Recovery Control.	0x0	R/W
		0	Automatic fault recovery for overcurrent fault.		
		1	Manual fault recovery for overcurrent fault.		

REGISTER DETAILS: I²C REGISTER MAP

STATUS CLEAR REGISTER

Address: 0x12, Reset: 0x00, Name: STATUS_CLR

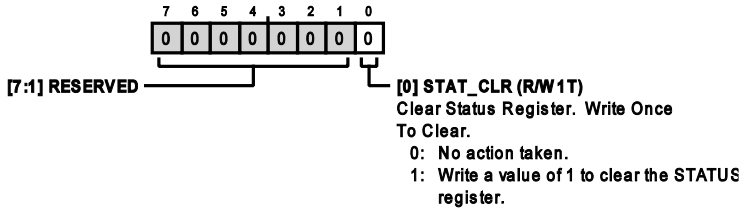


Table 35. Bit Descriptions for STATUS_CLR

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	STAT_CLR		Clear Status Register. Write Once To Clear.	0x0	R/W1T
		0	No action taken.		
		1	Write a value of 1 to clear the STATUS register.		

AMPLIFIER STATUS REGISTER

Address: 0x13, Reset: 0x00, Name: STATUS

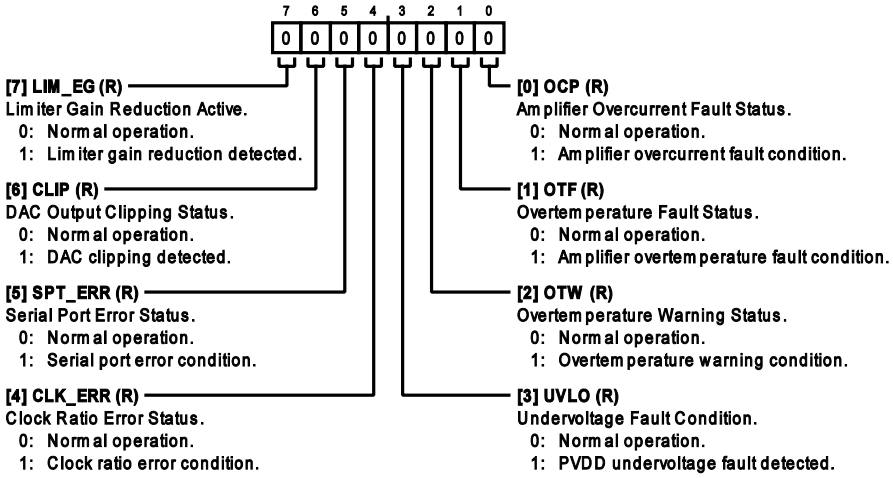


Table 36. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	LIM_EG		Limiter Gain Reduction Active.	0x0	R
		0	Normal operation.		
		1	Limiter gain reduction detected.		
6	CLIP		DAC Output Clipping Status.	0x0	R
		0	Normal operation.		
		1	DAC clipping detected.		

REGISTER DETAILS: I²C REGISTER MAP

Table 36. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
5	SPT_ERR		Serial Port Error Status.	0x0	R
		0	Normal operation.		
		1	Serial port error condition.		
4	CLK_ERR		Clock Ratio Error Status.	0x0	R
		0	Normal operation.		
		1	Clock ratio error condition.		
3	UVLO		Undervoltage Fault Condition.	0x0	R
		0	Normal operation.		
		1	PVDD undervoltage fault detected.		
2	OTW		Overtemperature Warning Status.	0x0	R
		0	Normal operation.		
		1	Overtemperature warning condition.		
1	OTF		Overtemperature Fault Status.	0x0	R
		0	Normal operation.		
		1	Amplifier overtemperature fault condition.		
0	OCP		Amplifier Overcurrent Fault Status.	0x0	R
		0	Normal operation.		
		1	Amplifier overcurrent fault condition.		

SOFT RESET REGISTER

Address: 0x14, Reset: 0x00, Name: RESET

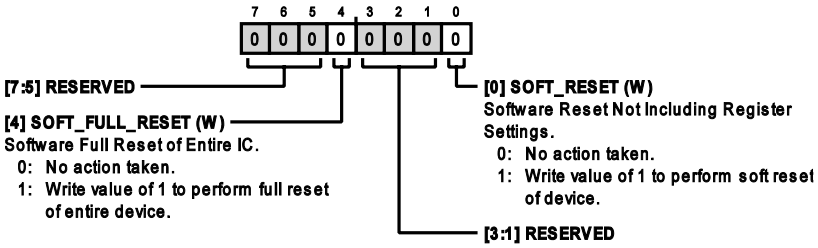


Table 37. Bit Descriptions for RESET

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	SOFT_FULL_RESET		Software Full Reset of Entire IC.	0x0	W
		0	No action taken.		
		1	Write value of 1 to perform a full reset of the device.		
[3:1]	RESERVED		Reserved.	0x0	R
0	SOFT_RESET		Software Reset Not Including Register Settings.	0x0	W
		0	No action taken.		
		1	Write value of 1 to perform a soft reset of the device.		

OUTLINE DIMENSIONS

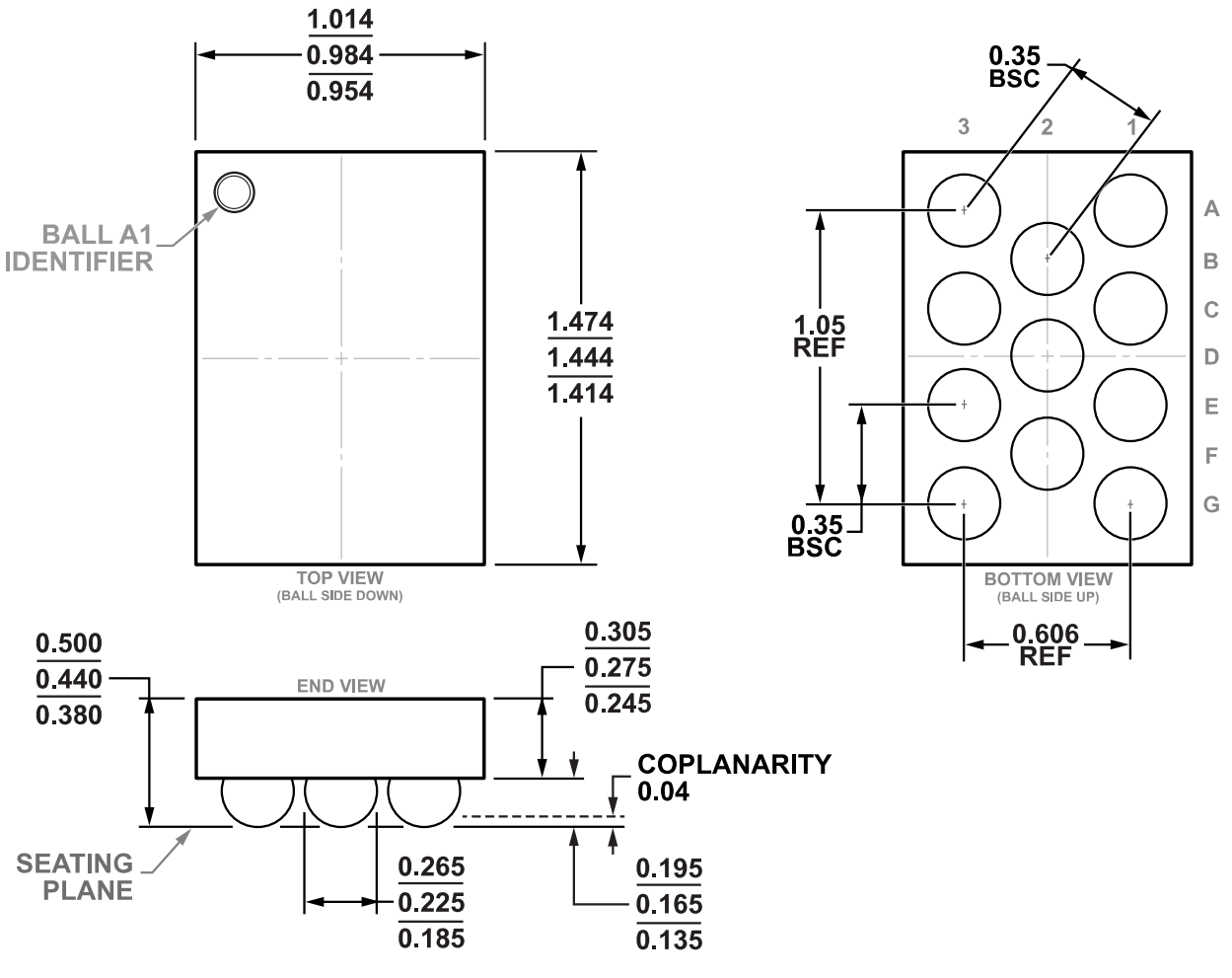


Figure 41. 11-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-11-3)
Dimensions shown in millimeters

Updated: March 03, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
SSM6515BCBZRL	-40°C to +85°C	CHIPS W/SOLDER BUMPS/WLCSP	Reel, 10000	CB-11-3	Y7V
SSM6515BCBZRL7	-40°C to +85°C	CHIPS W/SOLDER BUMPS/WLCSP	Reel, 3000	CB-11-3	Y7V

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Table 38.

Model	Description
EVAL-SSM6515Z	Evaluation Board

I^{2}C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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