- **Very High-Resolution, 1/3-in Solid-State Image Sensor for NTSC Color Applications**
- **340,000 Pixels per Field**
- **Frame Memory**
- **658 (H) × 496 (V) Active Elements in Image-Sensing Area Compatible With Electronic Centering**
- **Multimode Readout Capability**
  - **Progressive Scan**
  - **Interlaced Scan**
  - **Dual-Line Readout**
- **Fast Single-Pulse Clear Capability**
- **Continuous Electronic Exposure Control From 1/60 – 1/50,000 s**
- **7.4-μm Square Pixels**
- **Advanced Lateral-Overflow-Drain Antiblooming**
- **Low Dark Current**
- **High Dynamic Range**
- **High Sensitivity**
- **High Blue Response**
- **Solid-State Reliability With No Image Burn-In, Residual Imaging, Image Distortion, Image Lag, or Microphonics**

description

The TC236 is a frame-transfer, charge-coupled device (CCD) image sensor designed for use in single-chip color NTSC TV, computer, and special-purpose applications requiring low cost and small size.

The image-sensing area of the TC236 is configured into 500 lines with 680 elements in each line. Twenty-two elements are provided in each line for dark reference. The blooming-protection feature of the sensor is based on an advanced lateral-overflow-drain concept. The sensor can be operated in a true-interlace mode as a 658(H) × 496(V) sensor with a very low dark current. One important feature of the TC236 very high-resolution sensor is the ability to capture a full 340,000 pixels per field. The image sensor also provides high-speed image-transfer capability. This capability allows for a continuous electronic exposure control without the loss of sensitivity and resolution inherent in other technologies. The charge is converted to signal voltage at 20 μV per electron by a high-performance structure with a reset and a voltage-reference generator. The signal is further buffered by a low-noise, two-stage, source-follower amplifier to provide high output-drive capability.

The TC236 is built using TI-proprietary advanced virtual-phase (AVP) technology, which provides devices with high blue response, low dark signal, good uniformity, and single-phase clocking. The TC236 is characterized for operation from –10°C to 45°C.

ADVANCE INFORMATION

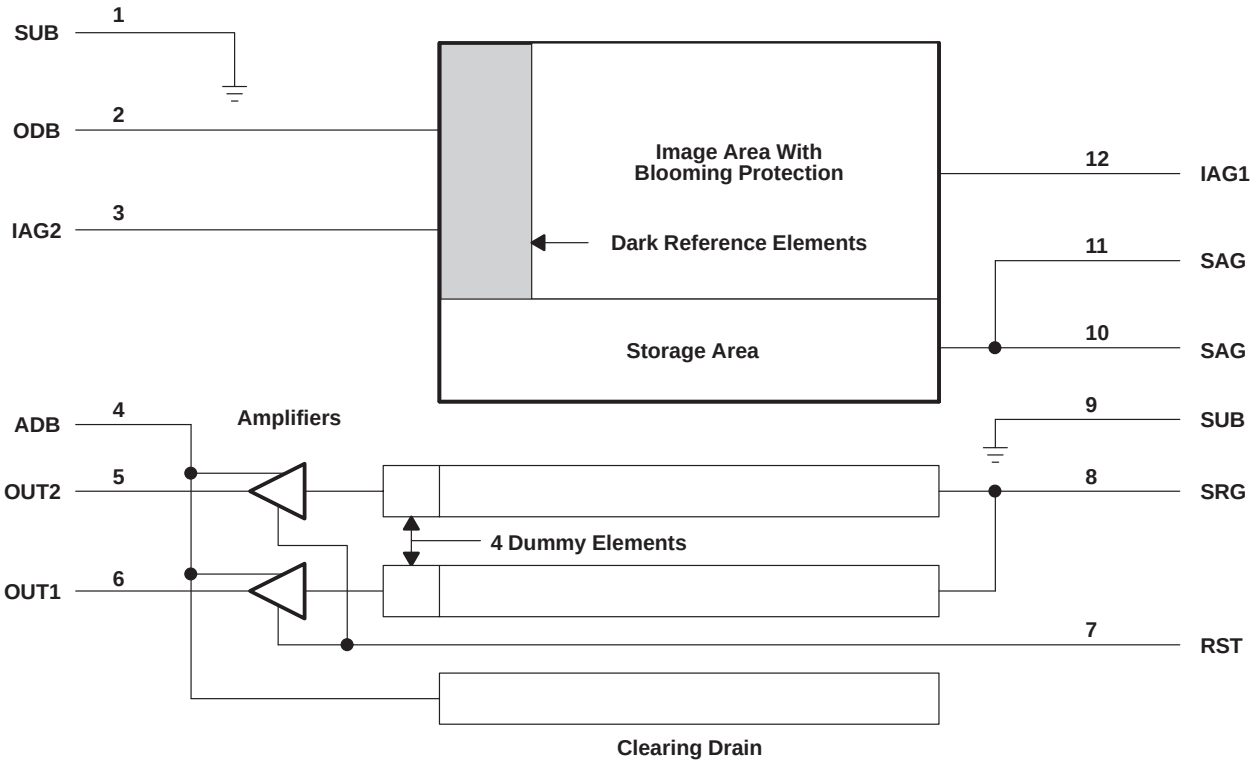
This MOS device contains limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to V_{SS}. Under no circumstances should pin voltages exceed absolute maximum ratings. Avoid shorting OUT to V_{SS} during operation to prevent damage to the amplifier. The device can also be damaged if the output terminals are reverse-biased and an excessive current is allowed to flow. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

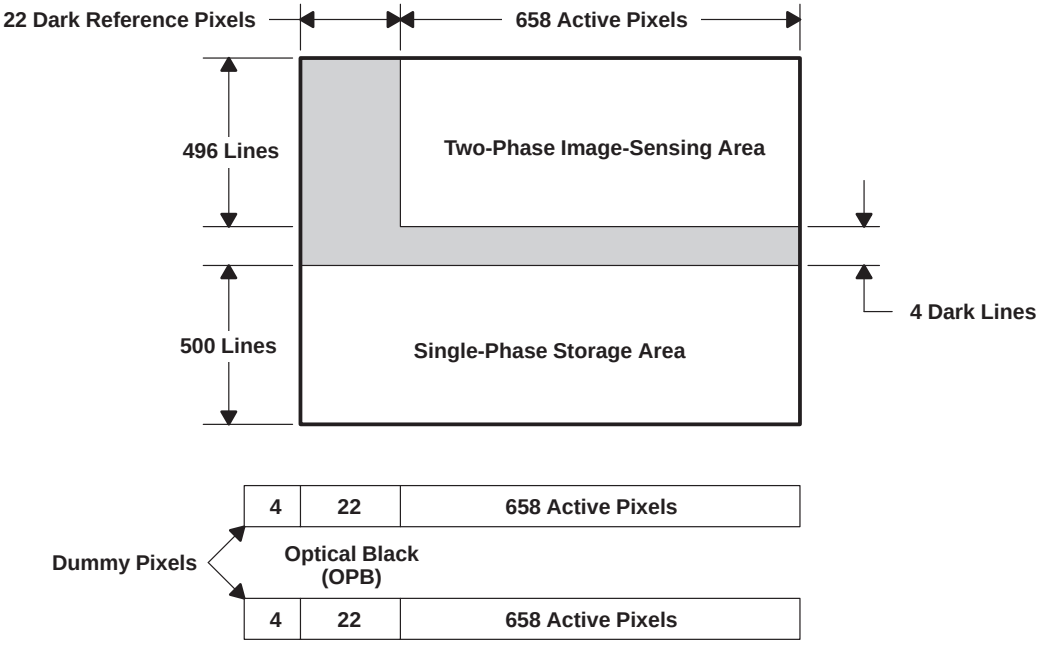
Copyright © 1994, Texas Instruments Incorporated

ADVANCE INFORMATION

functional block diagram



sensor topology diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADB	4	I	Supply voltage for amplifier-drain bias
IAG1	12	I	Image-area gate 1
IAG2	3	I	Image-area gate 2
ODB	2	I	Supply voltage for overflow-drain antiblooming bias
OUT1	6	O	Output signal 1
OUT2	5	O	Output signal 2
RST	7	I	Reset gate
SAG	10, 11	I	Storage-area gate
SRG	8	I	Serial-register gate
SUB	1, 9		Substrate

detailed description

The TC236 consists of four basic functional blocks: the image-sensing area, the image-storage area, the serial register gates, and the low-noise signal processing amplifier block with charge-detection nodes and independent resets. The location of each of these blocks is identified in the functional block diagram.

image-sensing and storage areas

Figure 1 and Figure 2 show top views of the image-sensing and storage-area elements. As light enters the silicon in the image-sensing area, free electrons are generated in both wells and collected in the virtual wells of the sensing elements. The color sensitivity is obtained by manufacturing a mosaic color filter directly onto the photosites of the image-sensing area (see Figure 3 for a mapping of the filter topology). Blooming protection is provided by applying a dc bias to the overflow-drain bias pin. If it is necessary to clear the image before beginning a new integration time (for implementation of electronic fixed shutter or electronic auto-iris), it is possible to do so by applying a pulse at least 1 μs in duration to the overflow-drain bias. After integration is complete, the charge is transferred into the storage area; the transfer timing is dependent on whether the readout mode is interlace or progressive scan. If the progressive-scan readout mode is selected, the readout may be performed normally with one register or high speed by using both registers (see Figure 4 through Figure 6 for the interlace and progressive-scan readout modes).

There are 22 columns at the left edge of the image-sensing area that are shielded from incident light; these elements provide the dark reference used in subsequent video-processing circuits to restore the video black level. There are also four dark lines between the image-sensing and the image-storage area that prevent charge leakage from the image-sensing area into the image-storage area.

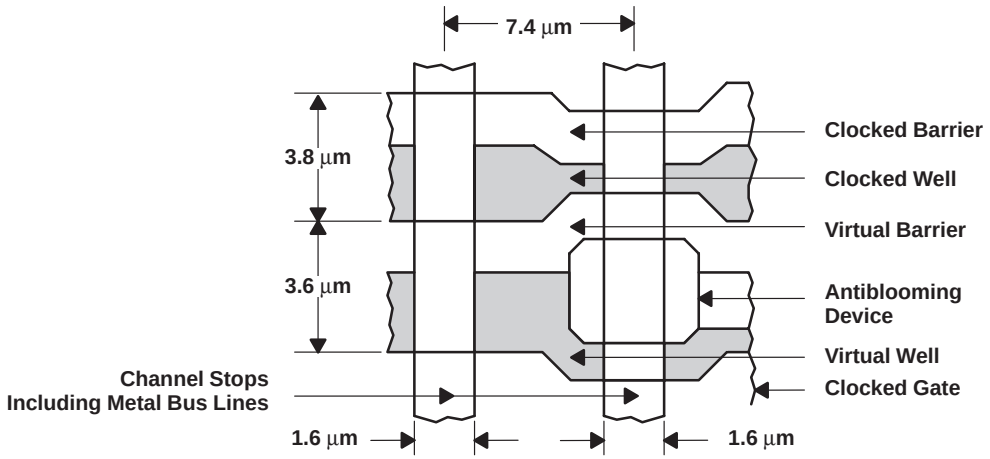


Figure 1. Image-Area Pixel Structure

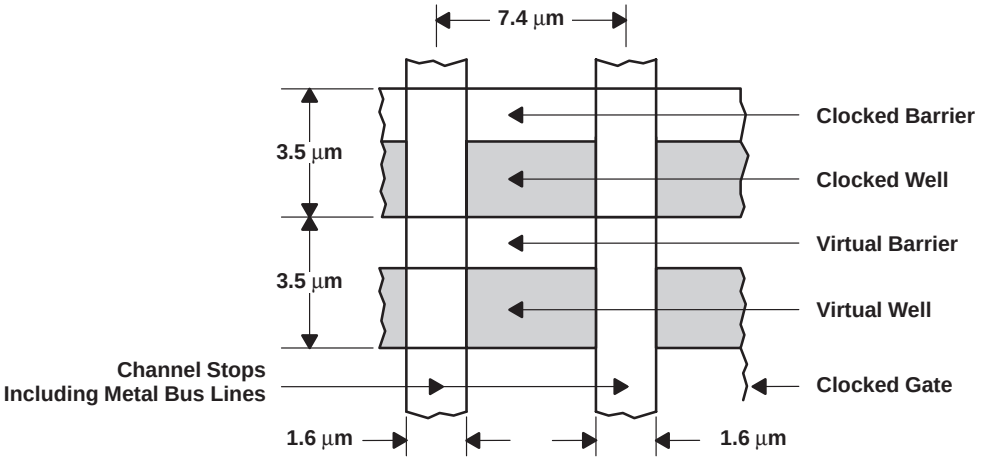


Figure 2. Storage-Area Pixel Structure

ADVANCE INFORMATION

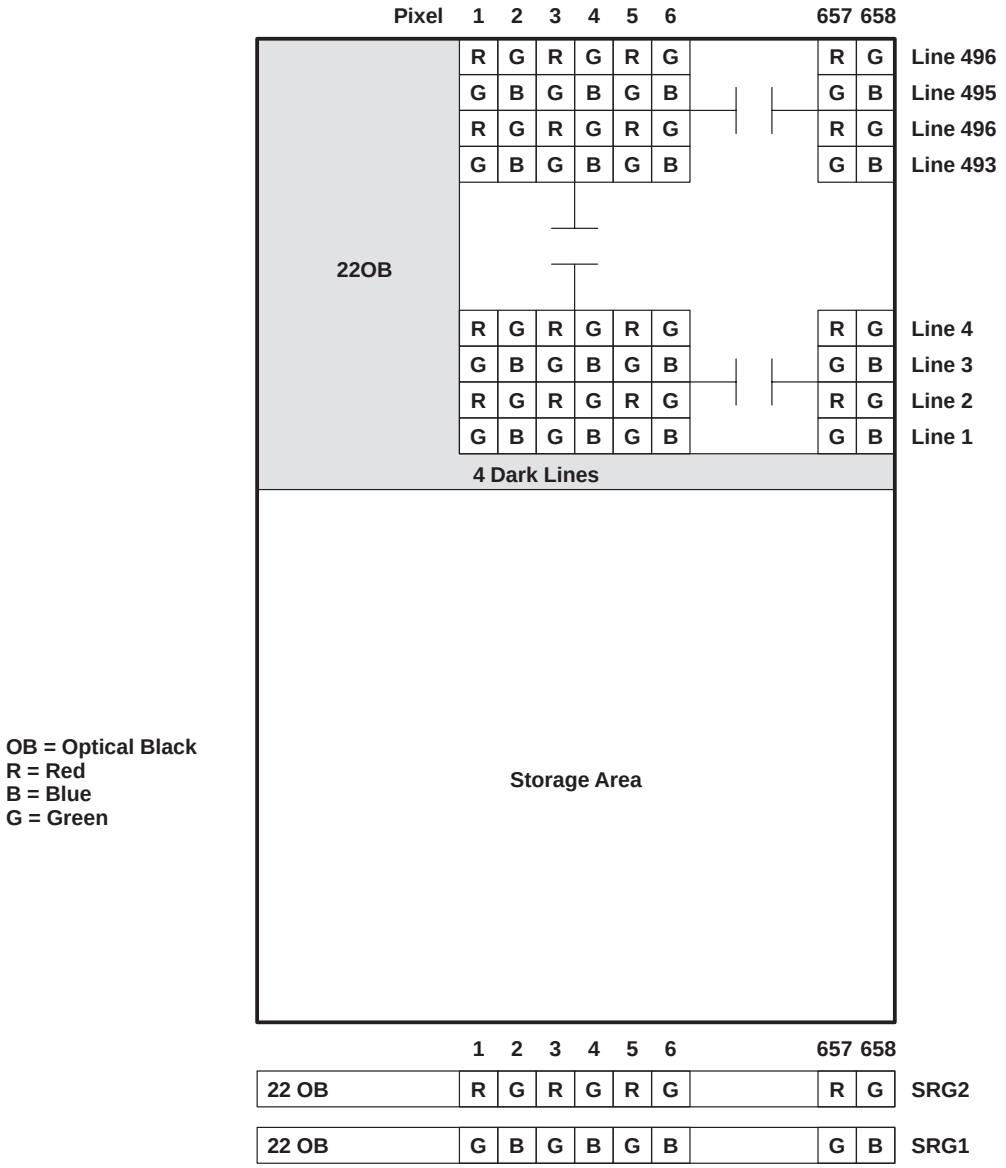


Figure 3. Color-Filter Topology Map

ADVANCE INFORMATION

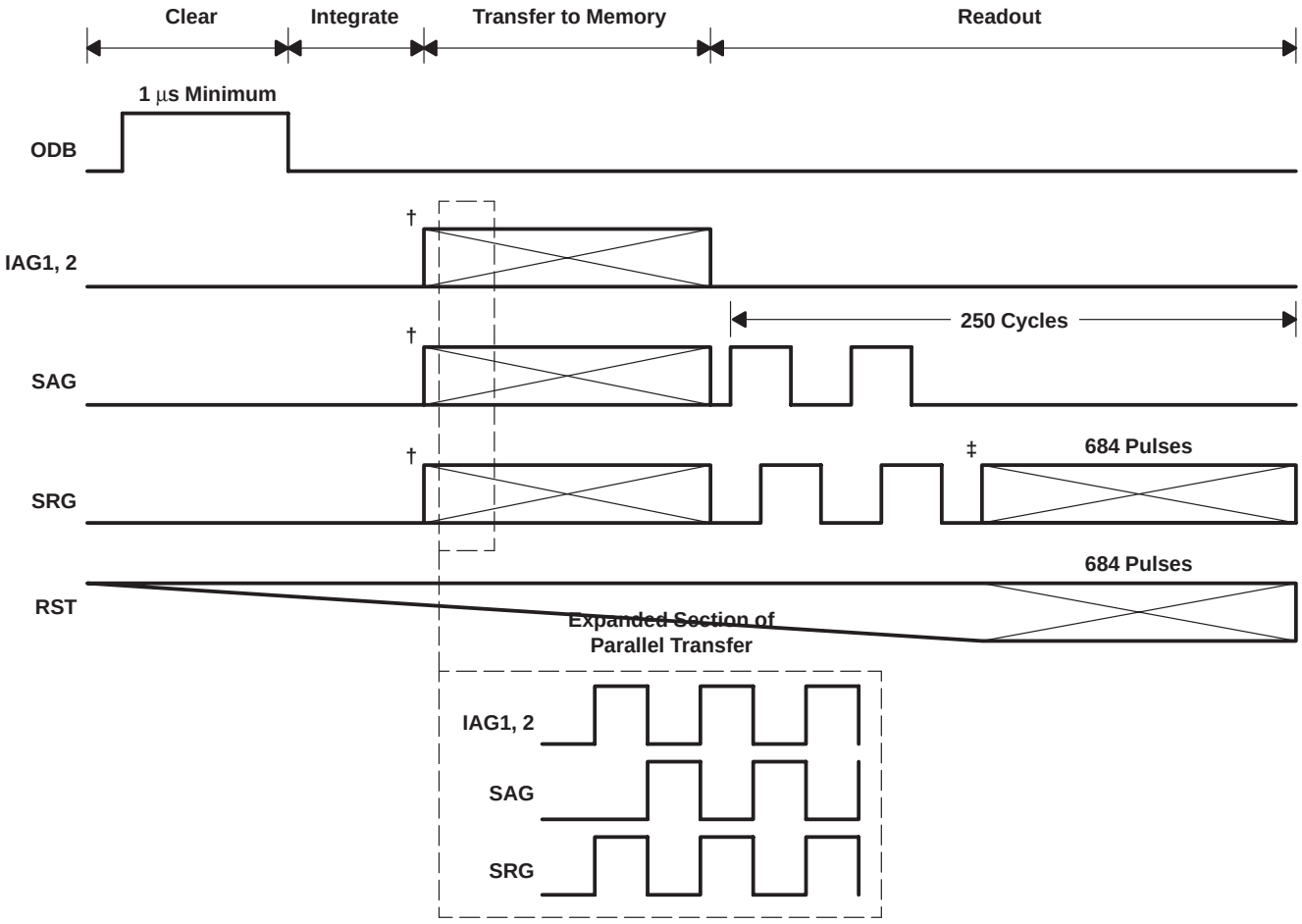
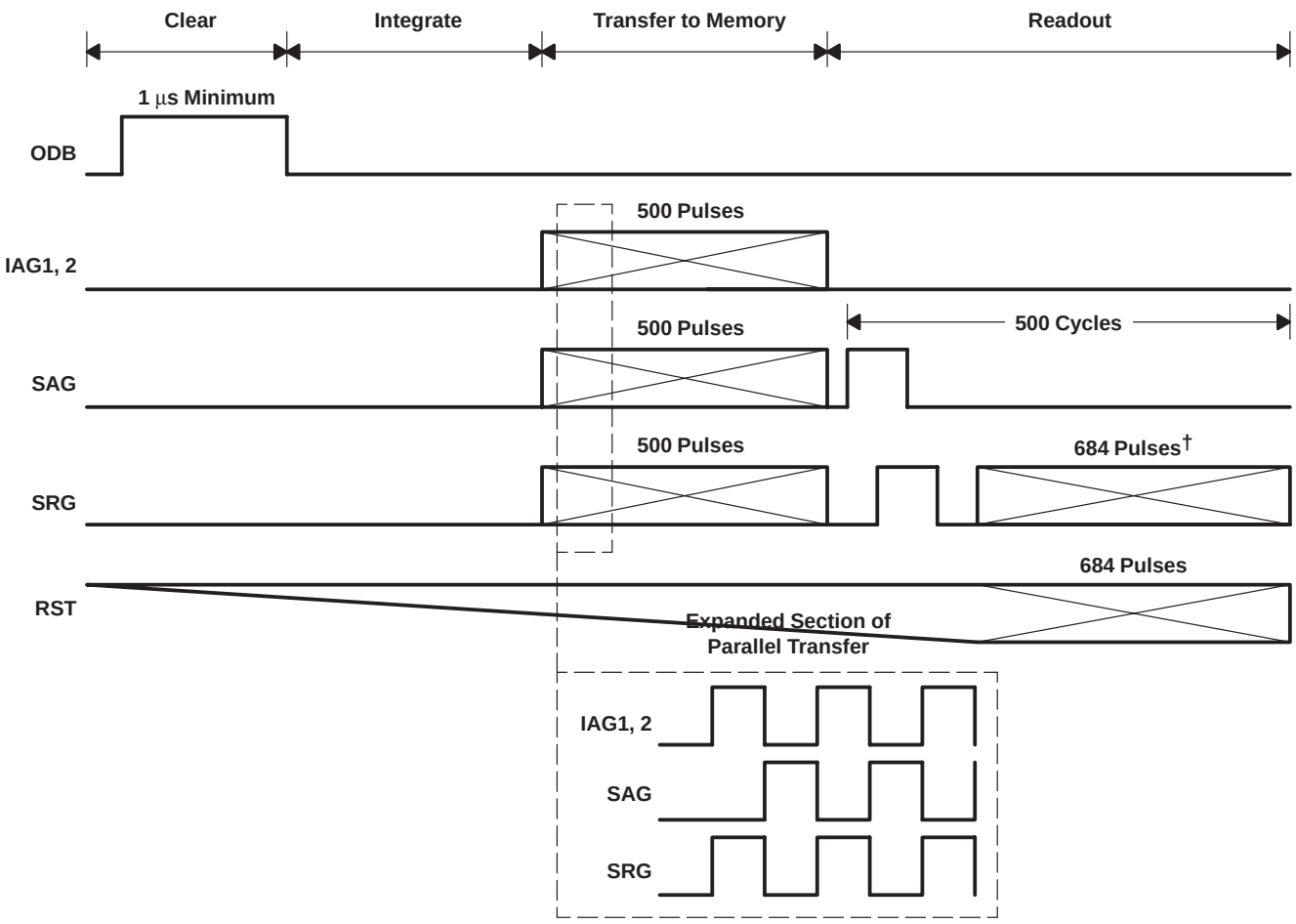


Figure 4. Interlace Timing

† The number of parallel transfer pulses is field dependent. Field 1 has 500 pulses of IAG1, IAG2, SAG, and SRG with appropriate phasing. Field 2 has 501 pulses.
‡ The readout is from register 2.

ADVANCE INFORMATION



† Readout is from register 2.

Figure 5. Progressive-Scan Timing With Single Register Readout

ADVANCE INFORMATION

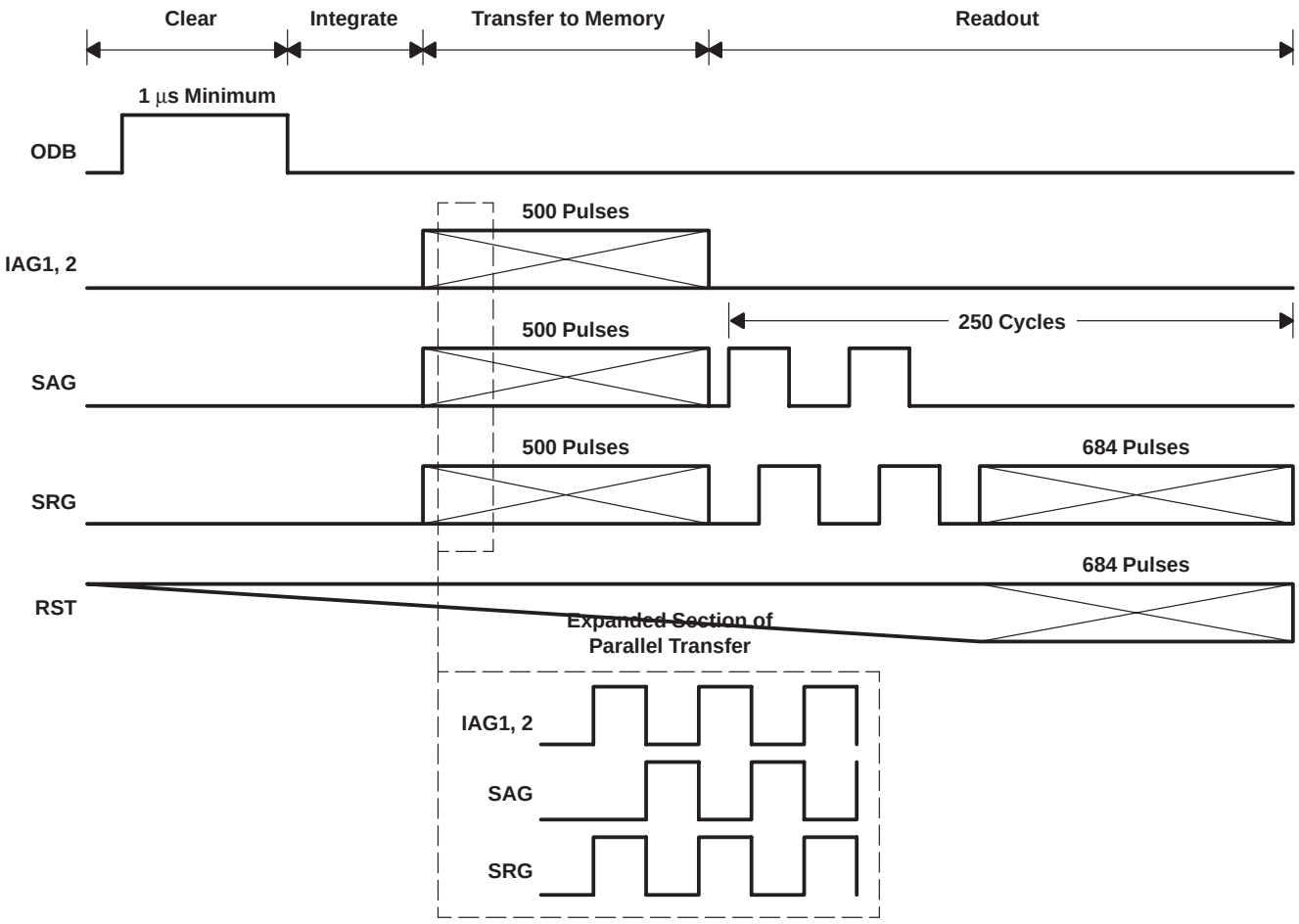


Figure 6. Progressive-Scan Timing With Dual Register Readout

serial registers

The storage-area gate and serial gate(s) are used to transfer the charge line by line from the storage area into the serial register(s). Depending on the readout mode, one or both serial registers is used. If both are used, the registers are read out in parallel.

readout and video processing

After transfer into the serial register(s), the pixels are read out and placed onto a charge-detection node. The node must be reset to a reference level before the next pixel is placed onto the detection node. The timing for the serial-register readout, which includes the external pixel clamp and sample-and-hold signals needed to implement correlated double sampling, is shown in Figure 7. As the charge is transferred onto the detection node, the potential of this node changes in proportion to the amount of signal received. The change is sensed by an MOS transistor and, after proper buffering, the signal is supplied to the output terminal of the image sensor. The buffer amplifier converts charge into a video signal. Figure 8 shows the circuit diagram of the charge-detection node and output amplifier. The detection nodes and amplifiers are placed a short distance away from the edge of the storage area; therefore, each serial register contains four dummy elements that are used to span the distance between the serial registers and the amplifiers.

ADVANCE INFORMATION

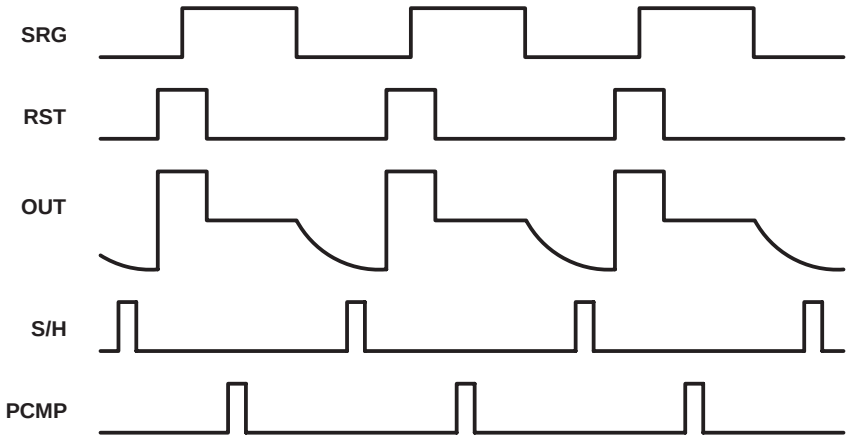


Figure 7. Serial-Readout and Video-Processing Timing

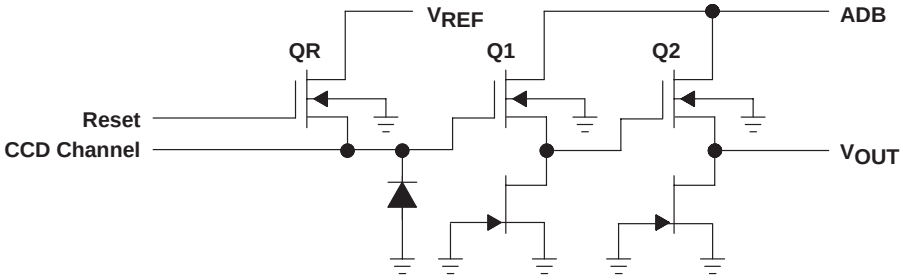


Figure 8. Output Amplifier and Charge-Detection Node

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, ADB (see Note 1) . . . . . SUB to SUB + 15 V
Supply voltage range, ODB . . . . . SUB to SUB + 21 V
Input voltage range for ABG, IAG1, IAG2, SAG, SRG . . . . . 0 V to 15 V
Operating free-air temperature range, T_A . . . . . –10°C to 45°C
Storage temperature range . . . . . –30°C to 85°C
Operating case temperature range . . . . . –10°C to 55°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to substrate terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage for amplifier drain bias, ADB			21	22	23	V
Supply voltage for overflow-drain antiblooming bias, ODB	Standard		17	18	19	V
	For clearing		27	28	29	
Substrate bias voltage				10		V
Input voltage, V_I	IAG1, IAG2	High level	11.5	12	12.5	V
		Low level		0		
	SAG	High level	11.5	12	12.5	
		Low level		0		
	SRG	High level	11.5	12	12.5	
		Low level		0		
Clock frequency, f_{clock}	IAG1, IAG2			25		MHz
	SAG			25		
	SRG, RST			12.5		
Capacitive load	OUT1, OUT2				6	pF
Operating free-air temperature, T_A			–10		45	°C

ADVANCE INFORMATION

electrical characteristics over recommended operating range of supply voltage, T_A = –10°C to 45°C

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 2)	With CDS‡	68	69	70	dB
	Without CDS‡	57	58	59	
Charge conversion factor			20		μV/e
Charge-transfer efficiency (see Note 3)		0.9999	0.99995	1	
Signal-response delay time, τ (see Note 4)			TBD		ns
Gamma (see Note 5)			1		
Output resistance		300	400	500	Ω
Noise-equivalent signal	With CDS‡	8.5	10	12	electrons
	Without CDS‡	30	36	42	
Rejection ratio	ADB (see Note 6)		TBD		dB
	SRG (see Note 7)		TBD		
	ABG (see Note 8)		TBD		
Supply current			5	10	mA
Input capacitance, C_i	IAG1, IAG2		2000		pF
	SRG		70		
	RST		10		
	SAG		4000		

† All typical values are at T_A = 25°C.

‡ CDS = Correlated double sampling, a signal-processing technique that improves noise performance by subtraction of reset noise.

NOTES: 2. Dynamic range is –20 times the logarithm of the mean noise signal divided by saturation output signal.

3. Charge-transfer efficiency is one minus the charge loss per transfer in the output register. The test is performed in the dark using an electrical input signal.

4. Signal-response delay time is the time between the falling edge of the SRG pulse and the output-signal valid state.

5. Gamma (γ) is the value of the exponent is the equation below for two points on the linear portion of the transfer-function curve (this value represents points near saturation).

$$\left(\frac{\text{Exposure (2)}}{\text{Exposure (1)}}\right)^{\gamma} = \left(\frac{\text{Output signal (2)}}{\text{Output signal (1)}}\right)$$

6. ADB rejection ratio is –20 times the logarithm of the ac amplitude at the output divided b the ac amplitude at ADB.

7. SRG rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at SRG.

8. ABG rejection ratio is –20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at ABG.

ADVANCE INFORMATION

optical characteristics, T_A = 40°C, integration time = 16.67 ms (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
Sensitivity (see Note 9)	No IR filter			256		mV/lux
	With IR filter			32		
Saturation signal, V_{sat} (see Note 10)	Antiblooming disabled			600		mV
Maximum usable signal, V_{use}	Antiblooming enabled		300	400	500	mV
Blooming overload ratio (see Note 11)				1000		
Image-area well capacity			22K	30K	38K	electrons
Smear (see Note 12)		See Note 13			–78	dB
Dark current		T_A = 21°C			0.05	nA/cm^2
Dark signal		T_A = 60°C			1	mV
Dark-signal uniformity		T_A = 60°C			0.5	mV
Dark-signal shading		T_A = 60°C			0.5	mV
Spurious nonuniformity	Dark	T_A = 60°C			10	mV
	Illuminated, F#8	T_A = 60°C			15	%
Column uniformity					0.5	mV
Electronic-shutter capability			1/50,000	1/60		s

NOTES: 9. Theoretical value
10. Saturation is the condition in which further increase in exposure does not lead to further increase in output signal.
11. Blooming is the condition in which charge is induced in an element by light incident on another element. Blooming overload ratio is the ratio of blooming exposure to saturation exposure.
12. Smear is a measure of the error introduced by transferring charge through an illuminated pixel in shutterless operation. It is equivalent to the ratio of the single-pixel transfer time to the exposure time using an illuminated section that is 1/10 of the image-area vertical height with recommended clock frequencies.
13. The exposure time is 16.67 ms, the fast-dump clocking rate during vertical transfer is 12.5 MHz, and the illuminated section is 1/10 the height of the image section.

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

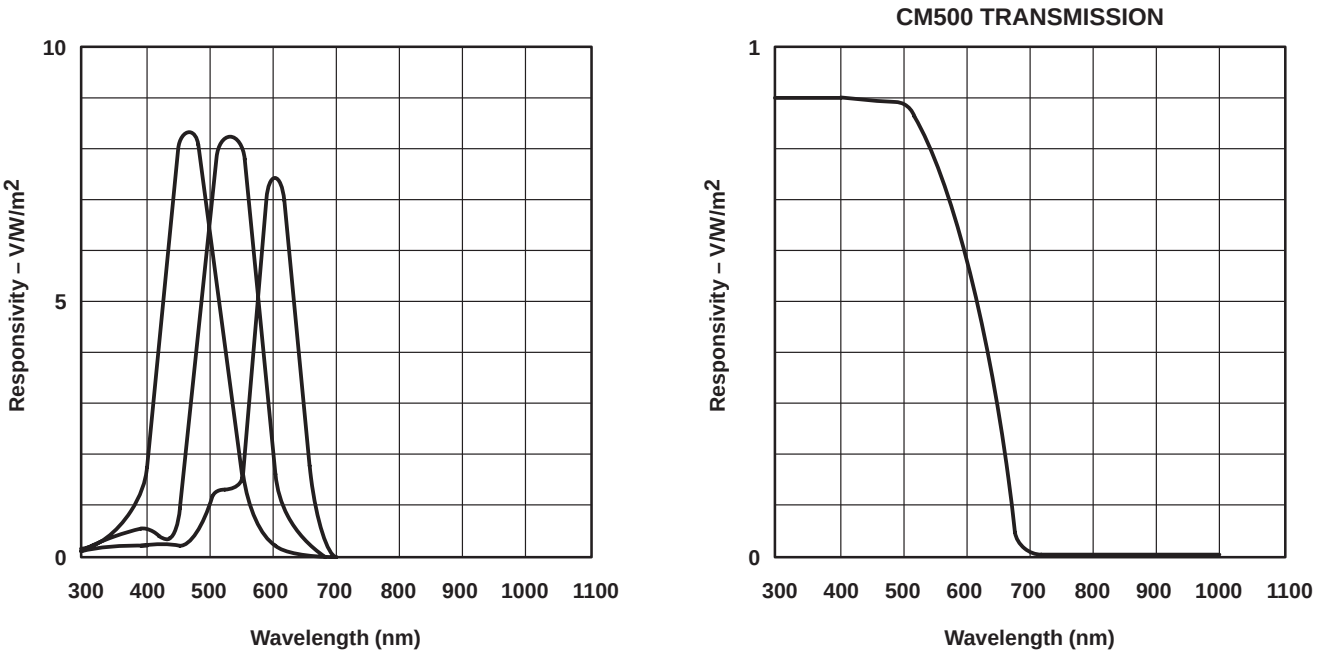


Figure 9. TC236 Sensor Spectral Response With a 1-mm CM500 IR Block Filter

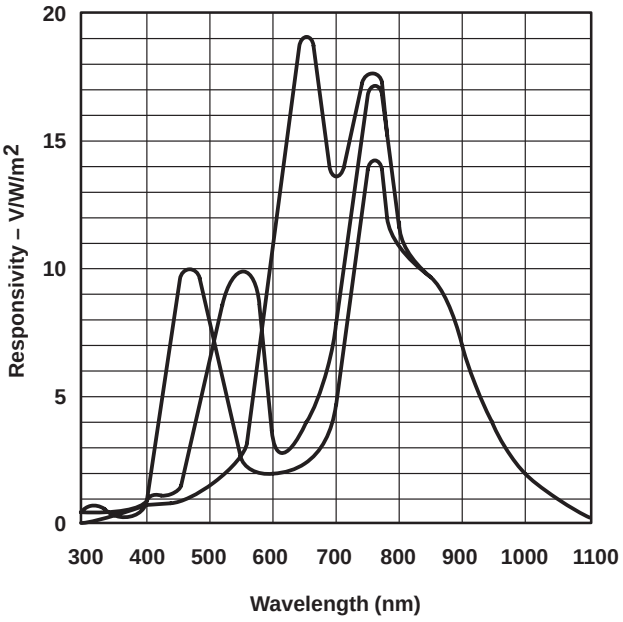
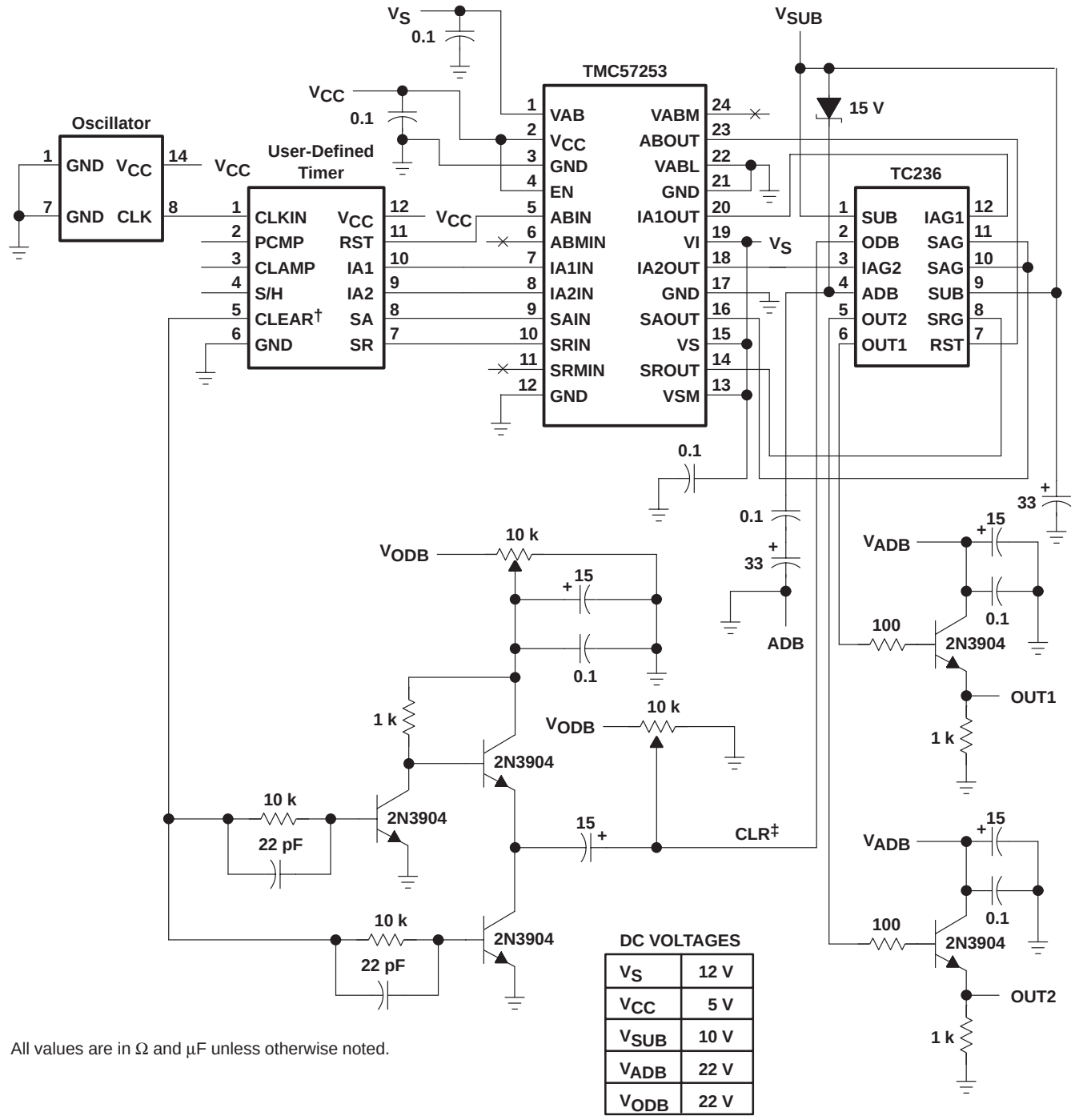


Figure 10. TC236 Sensor Spectral Response Without a 1-mm CM500 IR Block Filter

ADVANCE INFORMATION



DC VOLTAGES	
V_S	12 V
V_{CC}	5 V
V_{SUB}	10 V
V_{ADB}	22 V
V_{ODB}	22 V

All values are in Ω and μF unless otherwise noted.

† CLEAR is active-low TTL.
‡ CLR is nominally 18 VDC with a 10-V pulse for image clear.

Figure 11. Typical Application Circuit Diagram

SUPPORT CIRCUIT			
DEVICE	**PACKAGE**	**APPLICATION**	**FUNCTION**
TMC57253HSOP	44-pin flatpack	Driver	Driver for IAG1, 2, SAG, SRG, and RST

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated