

N-channel 525 V, 1.25 Ω typ., 4.4 A UltraFASTmesh™ Power MOSFETs in DPAK and TO-220FP packages

Datasheet - production data

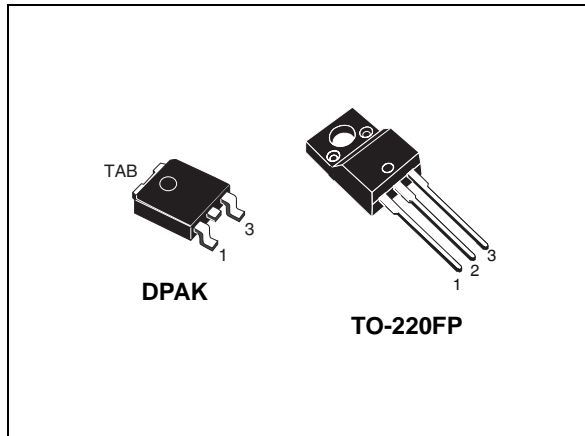
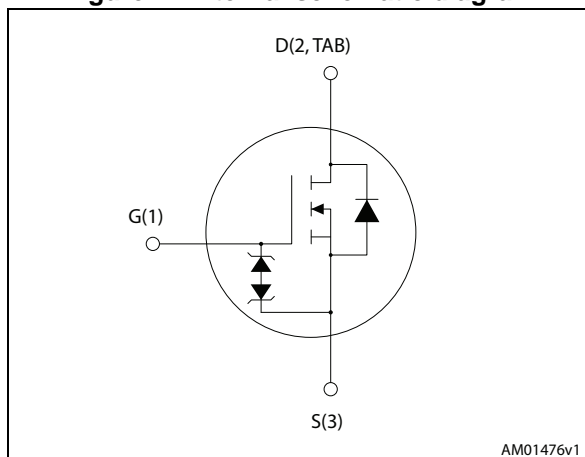


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on) \max}$	I_D	P_{TOT}
STD5N52U	525 V	1.5 Ω	4.4 A	70 W
STF5N52U				25 W

- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low $R_{DS(on)}$
- Extremely low t_{rr}

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using UltraFASTmesh™ technology, which combines the advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with an enhanced fast body-drain recovery diode.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD5N52U	5N52U	DPAK	Tape and reel
STF5N52U		TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	4.4		A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	2.8		A
$I_{DM}^{(1)}$	Drain current (pulsed)	17.6		A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	70	25	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	4.4		A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	170		mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	20		V/ns
ESD	Gate-source human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	2.8		kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}; T_C=25\text{ °C}$)	2500		V
T_J	Operating junction temperature	-55 to 150		°C
T_{stg}	Storage temperature			°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 4.4\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, peak $V_{DS} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1.79	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50		°C/W

1. When mounted on 1 inch² FR-4 board, 2oz Cu

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 1 mA	525			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 525 V			10	μA
		V _{DS} = 525 V, T _C = 125 °C			500	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 2.2 A		1.25	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	529	-	pF
C _{oss}	Output capacitance		-	71	-	pF
C _{rss}	Reverse transfer capacitance		-	13.4	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 420 V, V _{GS} = 0	-	11	-	pF
R _g	Gate input resistance	f = 1 MHz open drain	-	6	-	Ω
Q _g	Total gate charge	V _{DD} = 416 V, I _D = 4.4 A, V _{GS} = 10 V (see Figure 17)	-	16.9	-	nC
Q _{gs}	Gate-source charge		-	4.2	-	nC
Q _{gd}	Gate-drain charge		-	8.4	-	nC

1. C_{oss eq}, time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 260\text{ V}$, $I_D = 2.2\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	11.4	-	ns
t_r	Rise time		-	13.6	-	ns
$t_{d(off)}$	Turn-off-delay time		-	23.1	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		17.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.4\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 18)	-	55		ns
Q_{rr}	Reverse recovery charge		-	95		nC
I_{RRM}	Reverse recovery current		-	3.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	120		ns
Q_{rr}	Reverse recovery charge		-	266		nC
I_{RRM}	Reverse recovery current		-	4.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

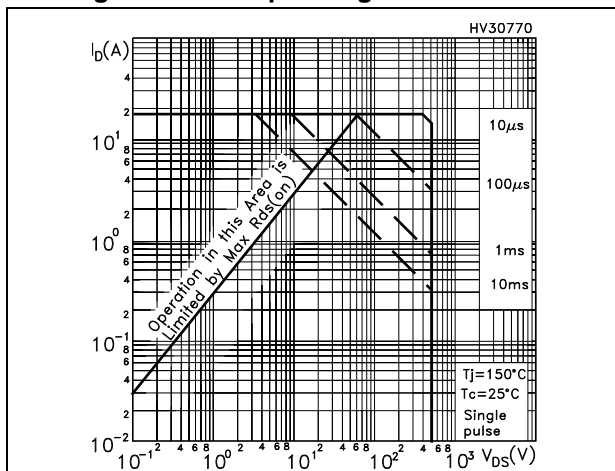


Figure 3. Thermal impedance for DPAK

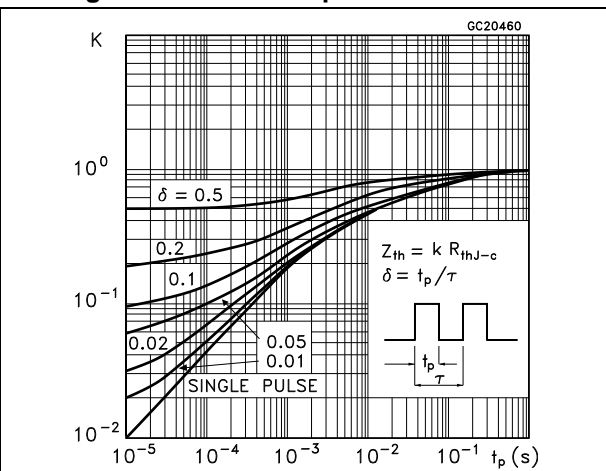


Figure 4. Safe operating area for TO-220FP

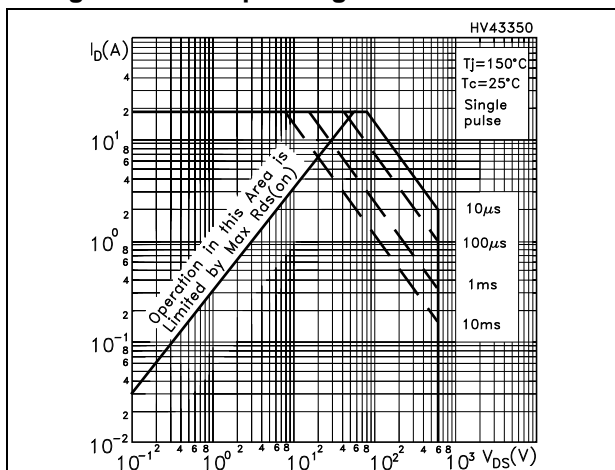


Figure 5. Thermal impedance for TO-220FP

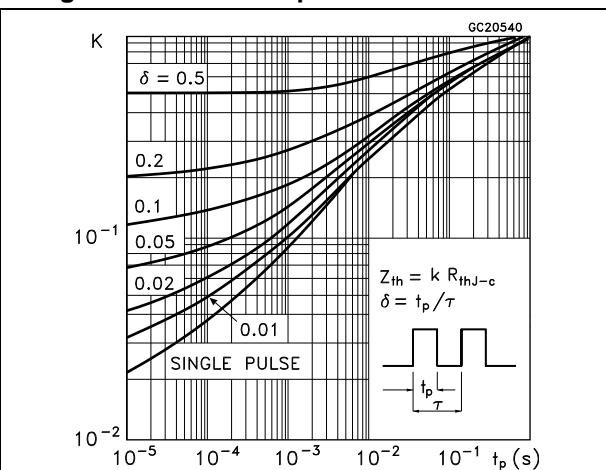


Figure 6. Output characteristics

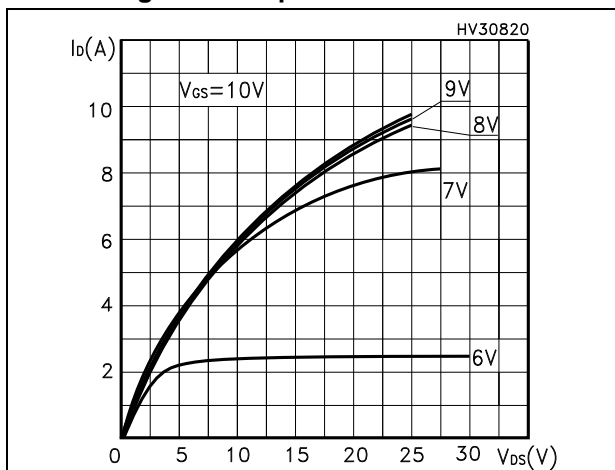


Figure 7. Transfer characteristics

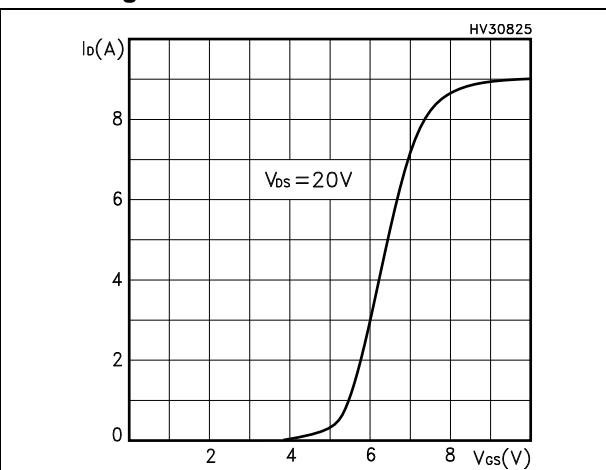


Figure 8. Normalized $V_{(BR)DSS}$ vs temperature

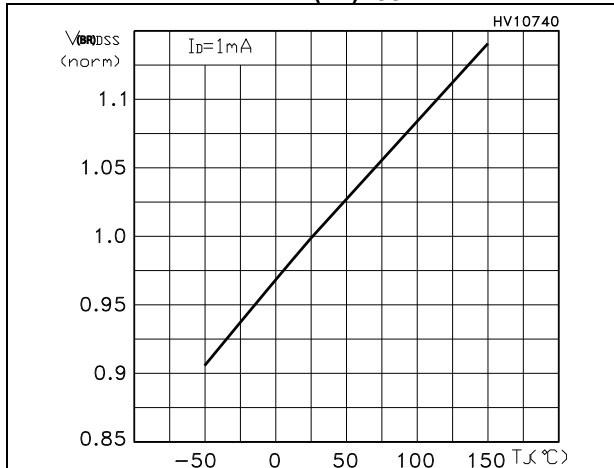


Figure 9. Static drain-source on-resistance

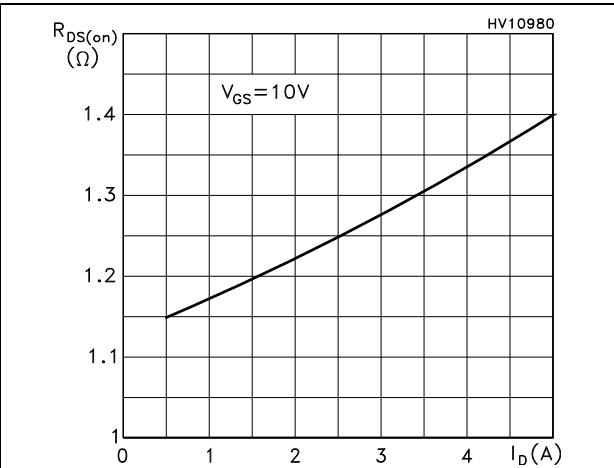


Figure 10. Gate charge vs gate-source voltage

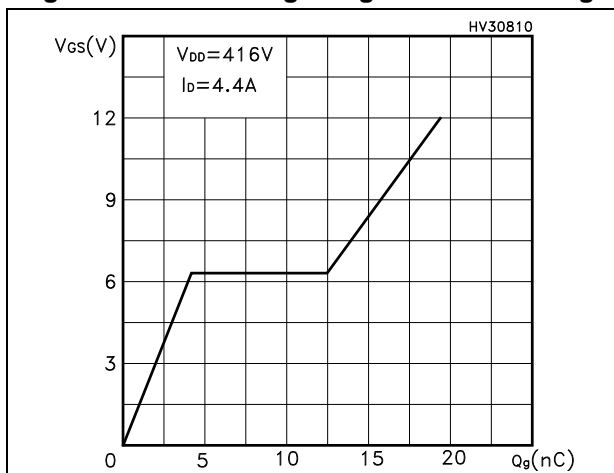


Figure 11. Capacitance variations

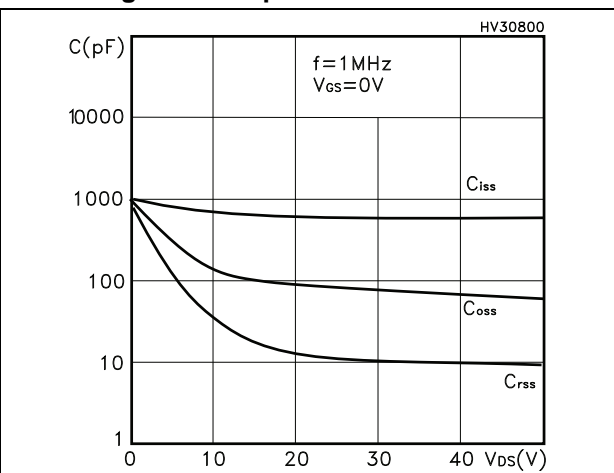


Figure 12. Normalized gate threshold voltage vs temperature

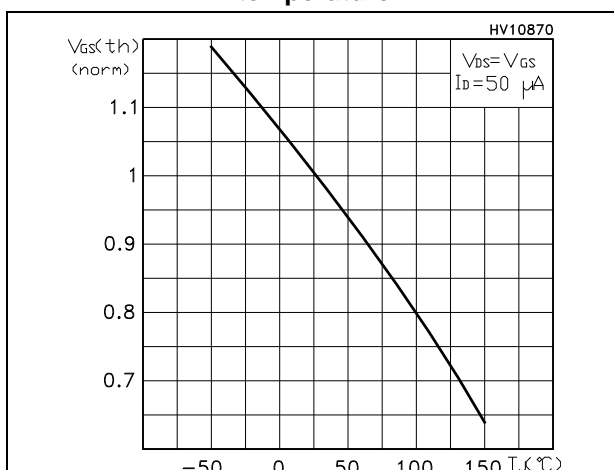


Figure 13. Normalized on-resistance vs temperature

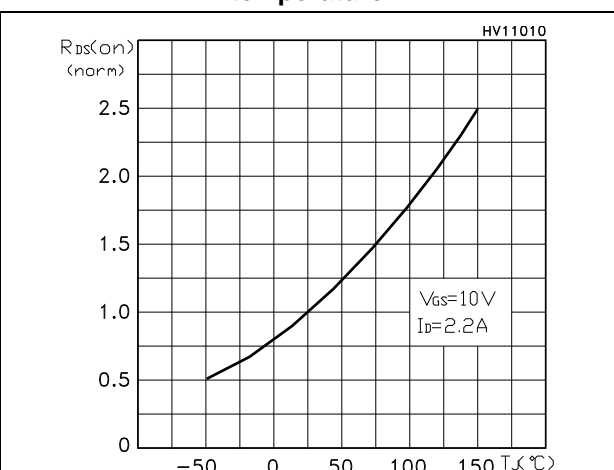


Figure 14. Source-drain diode forward characteristics

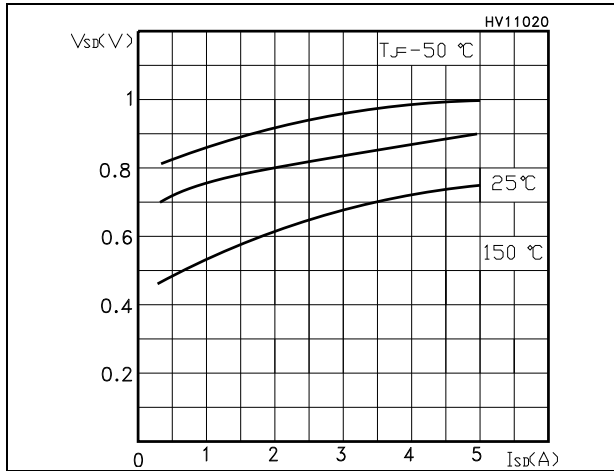
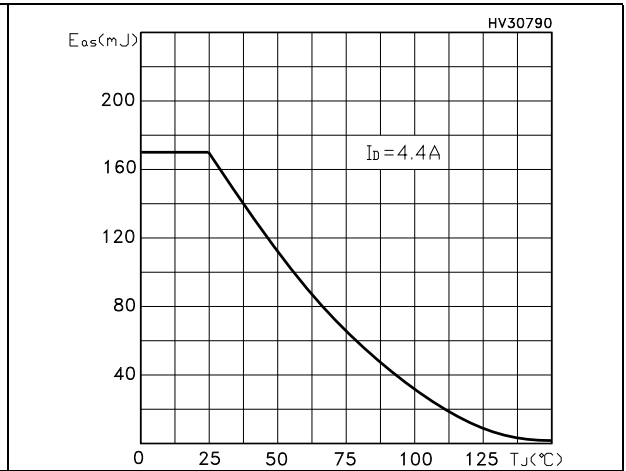


Figure 15. Maximum avalanche energy vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load



Figure 17. Gate charge test circuit



Figure 18. Test circuit for inductive load switching and diode recovery times



Figure 19. Unclamped inductive load test circuit



Figure 20. Unclamped inductive waveform



Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 DPAK, STD5N52U

Figure 22. DPAK (TO-252) type A drawing

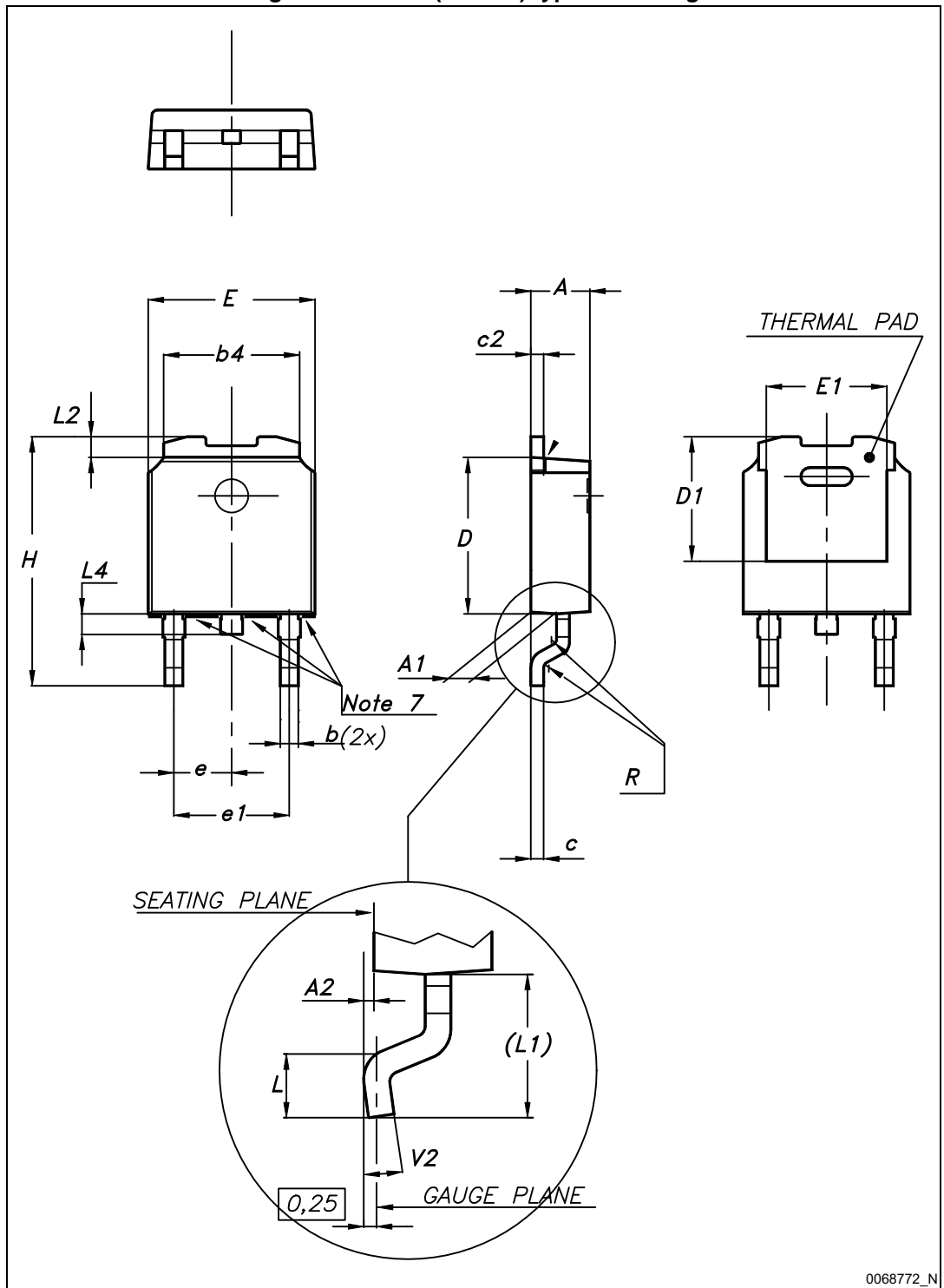
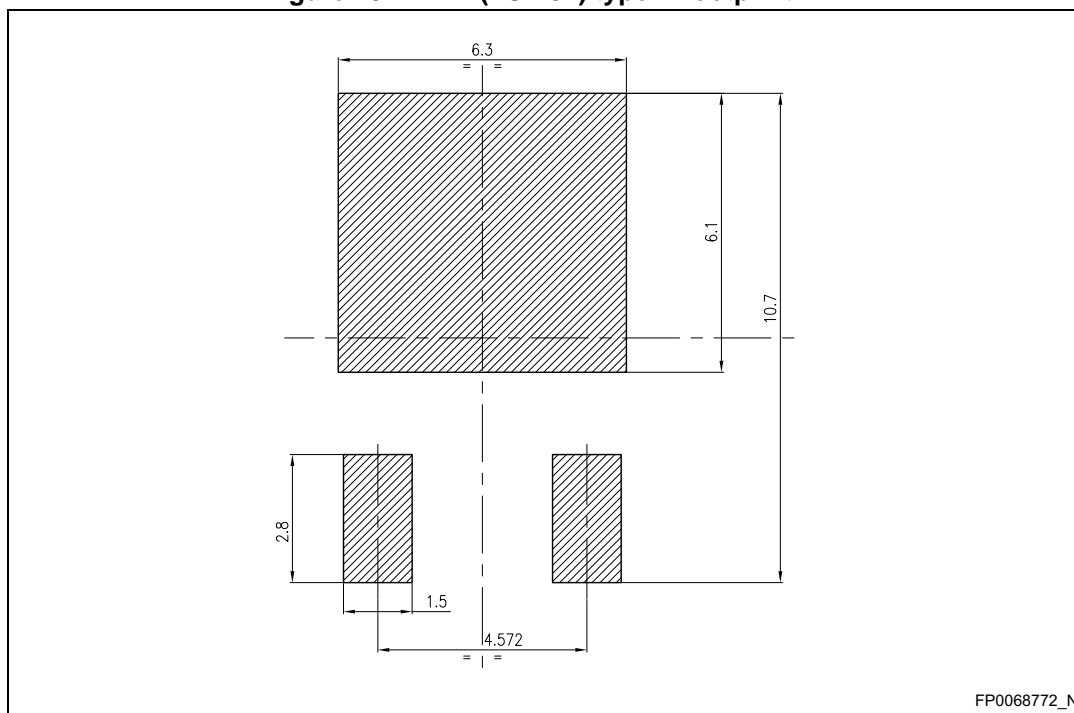


Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

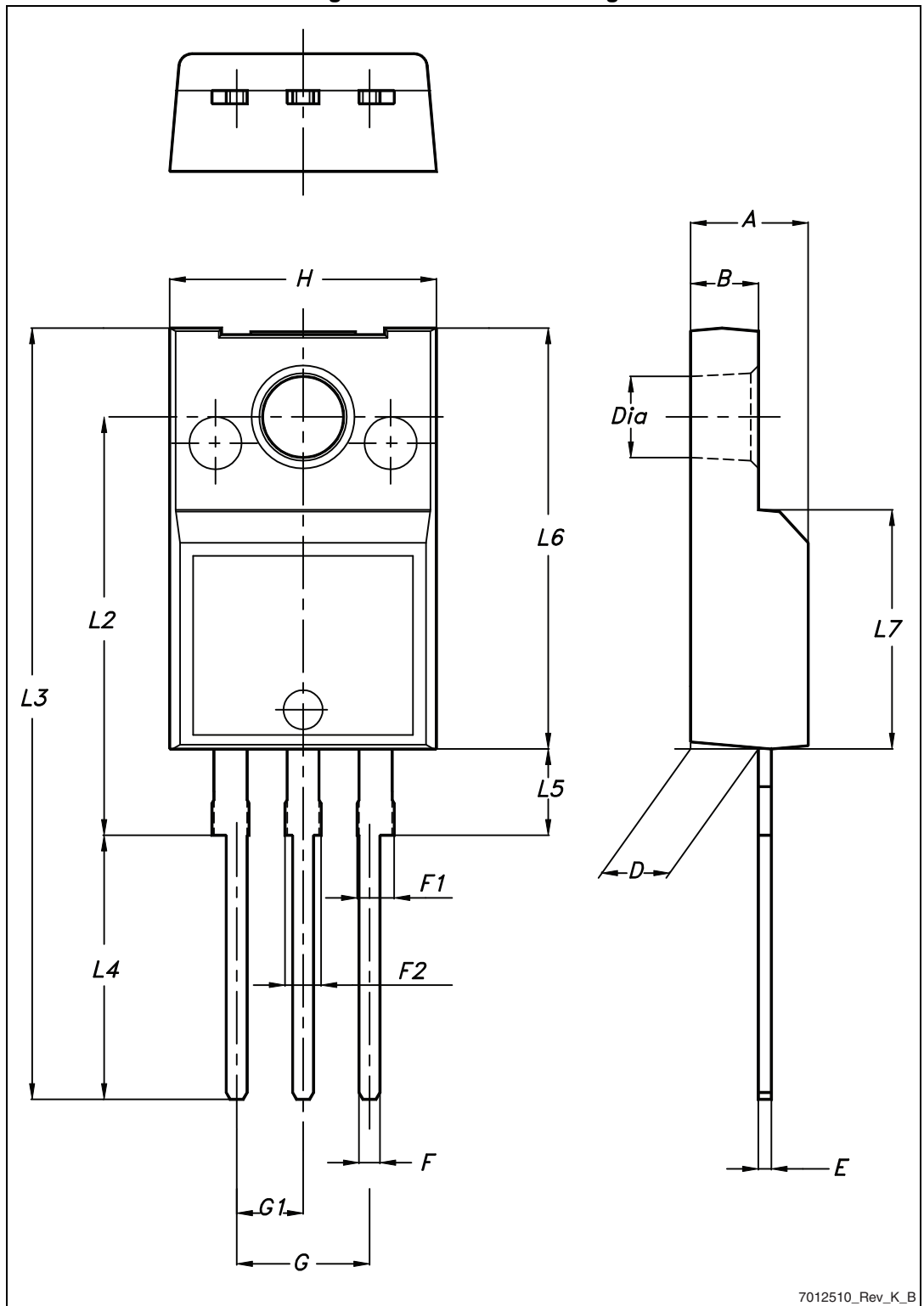
Figure 23. DPAK (TO-252) type A footprint (a)



a. All dimensions are in millimeters

4.2 TO-220FP, STF5N52U

Figure 24. TO-220FP drawing



7012510_Rev_K_B

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Ø	3		3.2

5 Packaging mechanical data

Figure 25. Tape for DPAK (TO-252)

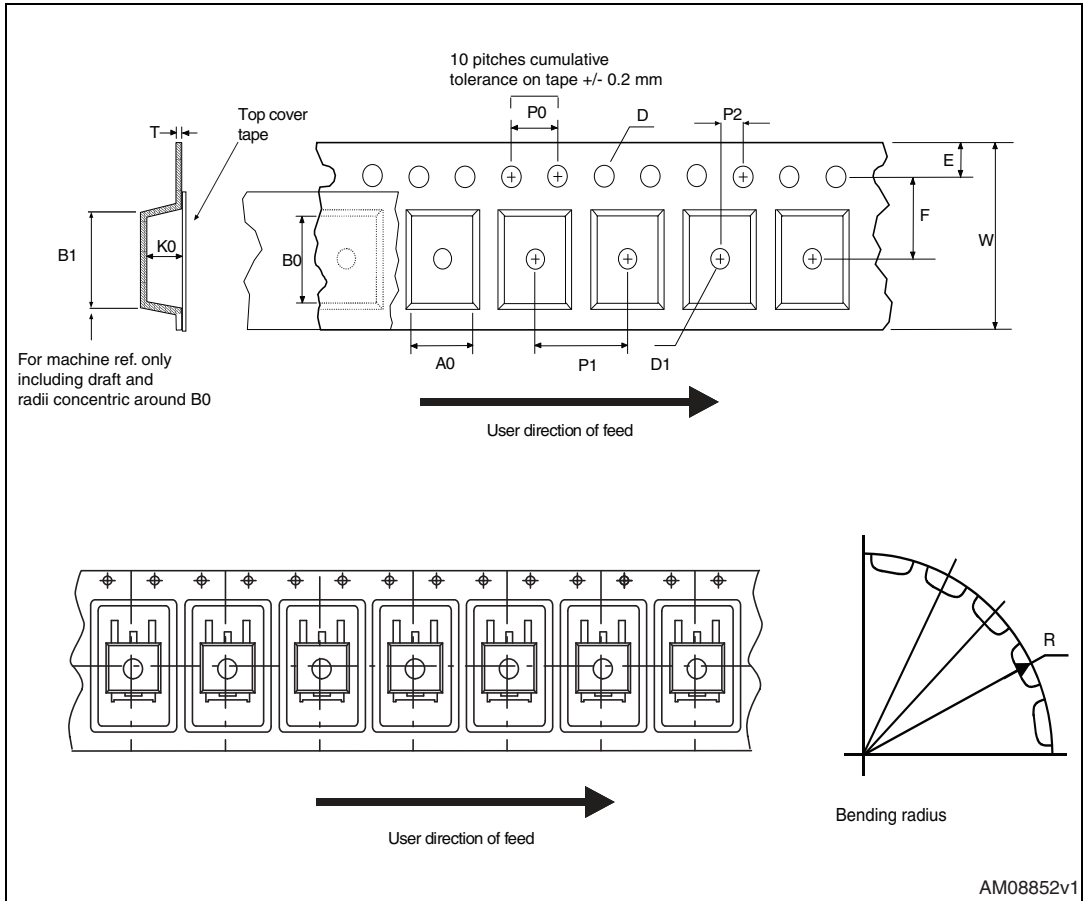


Figure 26. Reel for DPAK (TO-252)

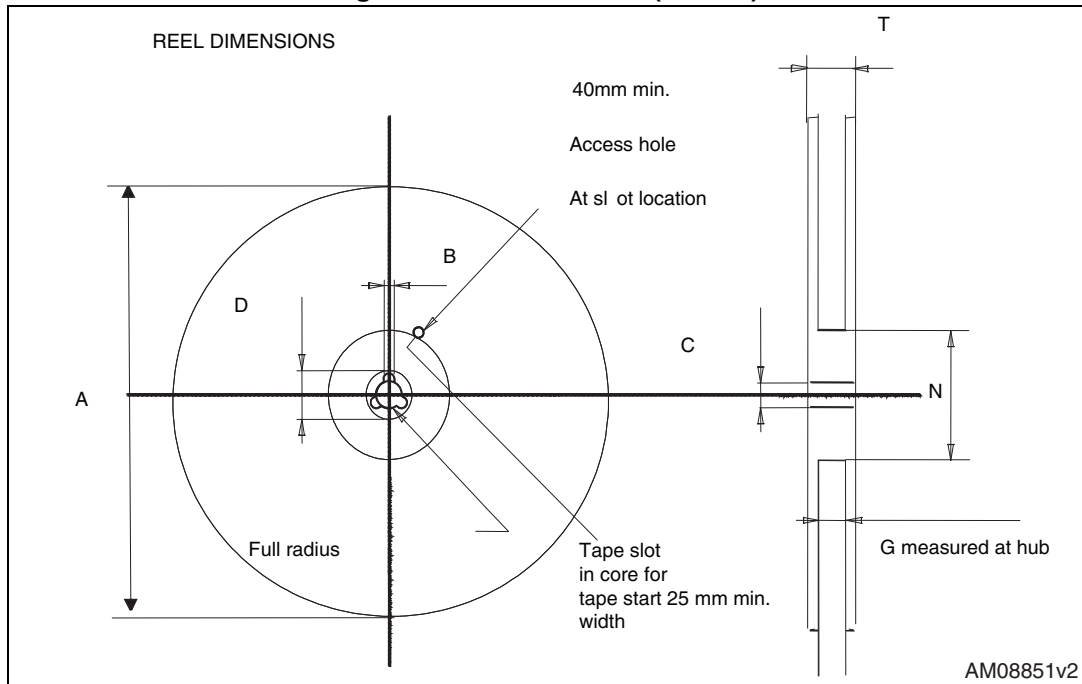


Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

6 Revision history

Table 12. Document revision history

Date	Revision	Changes
06-May-2009	1	First release.
28-Sep-2011	2	<ul style="list-style-type: none">– Inserted new device in I²PAK.– Updated tables 1, 2 and 3 with the new package.– Updated Section 4: Package mechanical data with the new package and Section 5: Packaging mechanical data.– Minor text changes.
24-Apr-2014	3	<ul style="list-style-type: none">– Updated Section 4.1: DPAK, STD5N52U– Modified: Q_{rr} unit in Table 7– Modified: Figure 8 and 11– The part number STI5N52U has been moved to a separate datasheet

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