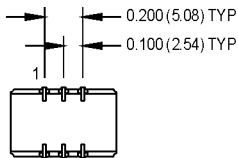
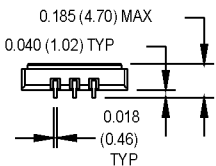
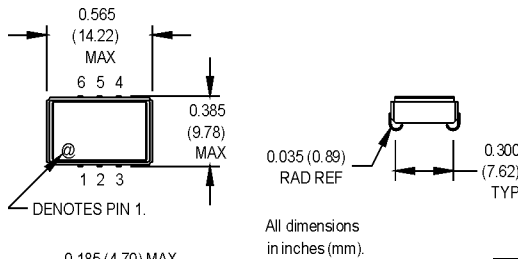


MPV3 Series

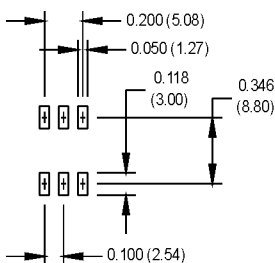
9x14 mm, 3.3 Volt, LVPECL/LVDS, VCXO



- Versatile VCXO to 800 MHz with good jitter (3 ps typical)
- Used in low jitter clock synthesizers and SONET applications



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Enable/Disable or N/C
3	Ground/Case
4	Output Q
5	Output $\bar{Q}$ or N/C
6	+Vcc

Ordering Information

Product Series	MPV3	1	0	R	1	L	J	-R	00.0000 MHz
Temperature Range	1: 0°C to +70°C	2: -40°C to +85°C	6: -20°C to +70°C	8: 0°C to +50°C					
Stability	0: Nominal per APR selection								
Output Type	R: Complementary, Enable	Z: Complementary, w/o Enable							
Absolute Pull Range	1: ±50 ppm (±35 ppm typ. Stability)	2: ±100 ppm (±20 ppm typ. Stability)	5: ±80 ppm (±25 ppm typ. Stability)	8: ±25 ppm (±50 ppm typ. Stability)					
Symmetry/Output Logic Type	L: 45/55% LVDS	P: 45/55% PECL	H: 40/60% LVDS	Q: 40/60% PECL					
Package/Lead Configurations	J: J-lead								
RoHS Compliance	Blank: non-RoHS compliant part	-R: RoHS compliant part							
Frequency (customer specified)									

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	0.75		800	MHz	
Operating Temperature	T _A	(See Ordering Information)				
Storage Temperature	T _s	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 1
Aging						
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz
Pullability/APR		(See Ordering Information)				See Note 2
Control Voltage	V _c	0.3	1.65	3	V	Pin 1 voltage
Linearity			5	10	%	Positive Monotonic Slope
Modulation Bandwidth	f _m	10			kHz	-3 dB bandwidth
Input Impedance	Z _{in}	50k			Ohms	
Input Voltage	V _{cc}	3.135	3.3	3.465	V	
Input Current	I _{cc}					
0.75 MHz to 26 MHz				60/30	mA	PECL/LVDS
26 MHz to 104 MHz				95/60	mA	PECL/LVDS
104 MHz to 800 MHz				105/60	mA	PECL/LVDS
Output Type						PECL/LVDS
Load		50 Ohms to V _{cc} -2 VDC 100 Ohm differential load				See Note 3 PECL waveform LVDS waveform
Symmetry (Duty Cycle) (Per Symmetry Code)		(See Ordering Information)				V _{cc} -1.3 VDC (PECL) 50% of Waveform (LVDS)
Output Skew				200	ps	
Differential Voltage	V _o	250	340	450	mV	LVDS only
Logic “1” Level	V _{oh}	V _{cc} -1.02			V	PECL
Logic “0” Level	V _{ol}			V _{cc} -1.63	V	PECL
Rise/Fall Time	T _r /T _f		0.35 .50	0.55 1.0	ns ns	@ 20/80% LVPECL @ 20/80% LVDS
Enable Function		80% V _{cc} min or N/C: output active 20% V _{cc} max: output disables to high-Z				
Start up Time		5			ps	
Phase Jitter	φ _J		3	5	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)						
@ 19.44 MHz	10 Hz -60	100 Hz -90	1 kHz -112	10 kHz -140	100 kHz -150	Offset from carrier dBc/Hz
@ 155.52 MHz	-60	-90	-112	-123	-120	dBc/Hz

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