# 5-BIT PROGRAMMABLE SYNCHRONOUS BUCK PLUS LDO CONTROLLER AND 200mA LDO ON-BOARD

## FEATURES

- Provides single chip solution for Vcore, GTL+ & clock supply
- 200mA On-Board LDO Regulator
- Designed to meet the latest Intel specification for Pentium II™
- On-Board DAC programs the output voltage from 1.3V to 3.5V
- Linear regulator controller on board for 1.5V GTL+ supply
- Loss-less Short Circuit Protection with HICCUP
- Synchronous operation allows maximum efficiency patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Soft-Start
- High current totem pole driver for direct driving of the external power MOSFET
- Power Good Function monitors all outputs
- Over-Voltage Protection circuitry protects the switcher output and generates a fault signal
- Thermal Shutdown
- Logic Level Enable Input

## APPLICATIONS

- Total Power Solution for Pentium II processor application

## DESCRIPTION

The IRU3018 controller IC is specifically designed to meet Intel specification for Pentium II™ microprocessor applications as well as the next generation of P6 family processors. The IRU3018 provides a single chip controller IC for the Vcore, LDO controller for GTL+ and an internal 200mA regulator for clock supply which are required for the Pentium II applications. These devices feature a patented topology that in combination with a few external components as shown in the typical application circuit, will provide in excess of 18A of output current for an on-board DC-DC converter while automatically providing the right output voltage via the 5-bit internal DAC. The IRU3018 also features loss-less current sensing for both switchers by using the $R_{DS(on)}$ of the high-side power MOSFET as the sensing resistor, internal current limiting for the clock supply, and a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window. Other features of the device are: Under-voltage lockout for both 5V and 12V supplies, an external programmable soft-start function, programming the oscillator frequency via an external resistor, Over-Voltage Protection (OVP) circuitry for both switcher outputs and an internal thermal shutdown.

## TYPICAL APPLICATION

**Note:** Pentium II is trademark of Intel Corp

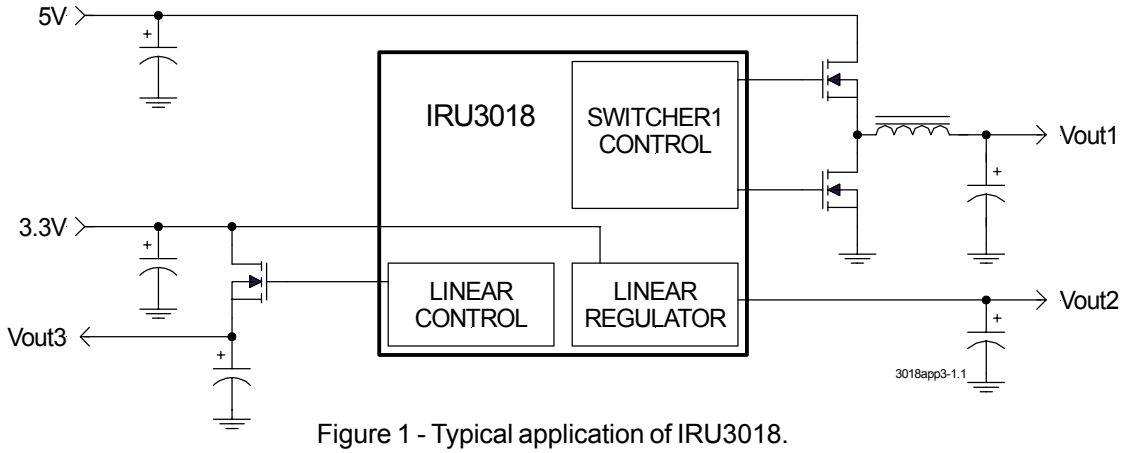



Figure 1 - Typical application of IRU3018.

## PACKAGE ORDER INFORMATION

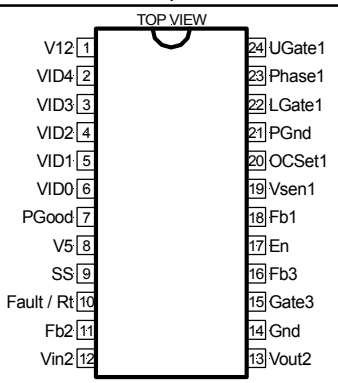
| $T_A$ (°C) | DEVICE | PACKAGE |
|---|---|---|
| 0 To 70 | IRU3018CW | 24-pin Plastic SOIC WB |

## ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage ..... 7V
V12 Supply Voltage ..... 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

## PACKAGE INFORMATION

24-PIN WIDE BODY PLASTIC SOIC (W)




$\theta_{JA}$ =80°C/W

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and $T_A$=0 to 70°C. Typical values refer to $T_A$=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply UVLO Section** | | | | | | |
| UVLO Threshold-12V | | Supply Ramping Up | | 10 | | V |
| UVLO Hysteresis-12V | | | | 0.4 | | V |
| UVLO Threshold-5V | | Supply Ramping Up | | 4.3 | | V |
| UVLO Hysteresis-5V | | | | 0.3 | | V |
| **Supply Current** | | | | | | |
| Operating Supply Current | $I_{12}$ | V12 | | 6 | | |
| | $I_5$ | V5 | | 20 | | mA |
| **Switching Controller, Vcore (Vout 1)** | | | | | | |
| **VID Section** | | | | | | |
| DAC Output Voltage (Note 1) | $V_{DAC}$ | | 0.99Vs | Vs | 1.01Vs | V |
| DAC Output Line Regulation | | | | 0.1 | | % |
| DAC Output Temp Variation | | | | 0.5 | | % |
| VID Input LO | | | | | 0.8 | V |
| VID Input HI | | | 2 | | | V |
| VID Input Internal Pull-Up Resistor to V5 | | | | 27 | | KΩ |
| **Error Comparator Section** | | | | | | |
| Input Bias Current | | | | | 2 | μA |
| Input Offset Voltage | | | -2 | | +2 | mV |
| Delay to Output | | Vdiff=10mV | | | 100 | ns |
| **Oscillator Section (Internal)** | | | | | | |
| Osc Frequency | | | | 200 | | KHz |

| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Current Limit Section** | | | | | | |
| CS Threshold Set Current | | | | 200 | | µA |
| CS Comp Offset Voltage | | | -5 | | +5 | mV |
| Hiccup Duty Cycle | | Css=0.1µF | | 10 | | % |
| **Output Drivers Section** | | | | | | |
| Rise Time | | $C_L$=3000pF | | 70 | | ns |
| Fall Time | | $C_L$=3000pF | | 70 | | ns |
| Dead Band Time Between High Side and Synch Drive Vcore Switcher Only | | $C_L$=3000pF | | 200 | | ns |
| **2.5V Regulator (Vout 2)** | | | | | | |
| Reference Voltage | Vo2 | $T_A$=25°C, Vout2=Fb2 | | 1.260 | | V |
| Reference Voltage | | | | 1.260 | | V |
| Dropout Voltage | | Io=200mA | | 0.6 | | V |
| Load Regulation | | 1mA< Io <200mA | | 0.5 | | % |
| Line Regulation | | 3.1V<Vin2<4V, Vo=2.5V | | 0.2 | | % |
| Input Bias Current | | | | | 2 | µA |
| Output Current | | | 200 | | | mA |
| Current Limit | | | 300 | | | mA |
| Thermal Shutdown | | | | 145 | | °C |
| **1.5V Regulator (Vout 3)** | | | | | | |
| Reference Voltage | Vo3 | $T_A$=25°C, Gate3=Fb3 | | 1.260 | | V |
| Reference Voltage | | | | 1.260 | | V |
| Input Bias Current | | | | | 2 | µA |
| Output Drive Current | | | 50 | | | mA |
| **Power Good Section** | | | | | | |
| Core UV Lower Trip Point | | Vsen1 Ramping Down | | 0.90Vs | | V |
| Core UV Upper Trip Point | | Vsen1 Ramping Up | | 0.92Vs | | V |
| Core UV Hysterises | | | | 0.02Vs | | V |
| Core OV Upper Trip Point | | Vsen1 Ramping Up | | 1.10Vs | | V |
| Core OV Lower Trip Point | | Vsen1 Ramping Down | | 1.08Vs | | V |
| Core OV Hysterises | | | | 0.02Vs | | V |
| Fb2 Lower Trip Point | | Fb2 Ramping Down | | 0.95 | | V |
| Fb2 Upper Trip Point | | Fb2 Ramping Up | | 1.05 | | V |
| Fb3 Lower Trip Point | | Fb3 Ramping Down | | 0.95 | | V |
| Fb3 Upper Trip Point | | Fb3 Ramping Up | | 1.05 | | V |
| Power Good Output LO | | $R_L$=3mA | | 0.4 | | V |
| Power Good Output HI | | $R_L$=5K, Pull-Up to 5V | | 4.8 | | V |
| **Fault (Overvoltage) Section** | | | | | | |
| Core OV Upper Trip Point | | Vsen1 Ramping Up | | 1.17Vs | | V |
| Core OV Lower Trip Point | | Vsen1 Ramping Down | | 1.15Vs | | V |
| Vin2 Upper Trip Point | | Vin2 Ramping Up | | 4.3 | | V |
| Vin2 Lower Trip Point | | Vin2 Ramping Down | | 4.2 | | V |
| Fault Output HI | | Io=3mA | | 10 | | V |
| **Soft-Start Section** | | | | | | |
| Pull-Up Resistor to 5V | | OCSet=0V, Phase=5V | | 23 | | KΩ |
| **Enable Section** | | | | | | |
| En Pin Input LO Voltage | Venl | Regulator OFF | | | 0.8 | V |
| En Pin Input HI Voltage | Venh | Regulator ON | 2 | | | V |
| En Pin Input LO Current | | Ven=0V to 0.8V | | 0.01 | | µA |
| En Pin Input HI Current | | Ven=2V to 5V | | 20 | | µA |

**Note 1:** Vs refers to the set point voltage given in Table 1

| D4 | D3 | D2 | D1 | D0 | Vs |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1.30 |
| 0 | 1 | 1 | 1 | 0 | 1.35 |
| 0 | 1 | 1 | 0 | 1 | 1.40 |
| 0 | 1 | 1 | 0 | 0 | 1.45 |
| 0 | 1 | 0 | 1 | 1 | 1.50 |
| 0 | 1 | 0 | 1 | 0 | 1.55 |
| 0 | 1 | 0 | 0 | 1 | 1.60 |
| 0 | 1 | 0 | 0 | 0 | 1.65 |
| 0 | 0 | 1 | 1 | 1 | 1.70 |
| 0 | 0 | 1 | 1 | 0 | 1.75 |
| 0 | 0 | 1 | 0 | 1 | 1.80 |
| 0 | 0 | 1 | 0 | 0 | 1.85 |
| 0 | 0 | 0 | 1 | 1 | 1.90 |
| 0 | 0 | 0 | 1 | 0 | 1.95 |
| 0 | 0 | 0 | 0 | 1 | 2.00 |
| 0 | 0 | 0 | 0 | 0 | 2.05 |

| D4 | D3 | D2 | D1 | D0 | Vs |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 2.0 |
| 1 | 1 | 1 | 1 | 0 | 2.1 |
| 1 | 1 | 1 | 0 | 1 | 2.2 |
| 1 | 1 | 1 | 0 | 0 | 2.3 |
| 1 | 1 | 0 | 1 | 1 | 2.4 |
| 1 | 1 | 0 | 1 | 0 | 2.5 |
| 1 | 1 | 0 | 0 | 1 | 2.6 |
| 1 | 1 | 0 | 0 | 0 | 2.7 |
| 1 | 0 | 1 | 1 | 1 | 2.8 |
| 1 | 0 | 1 | 1 | 0 | 2.9 |
| 1 | 0 | 1 | 0 | 1 | 3.0 |
| 1 | 0 | 1 | 0 | 0 | 3.1 |
| 1 | 0 | 0 | 1 | 1 | 3.2 |
| 1 | 0 | 0 | 1 | 0 | 3.3 |
| 1 | 0 | 0 | 0 | 1 | 3.4 |
| 1 | 0 | 0 | 0 | 0 | 3.5 |

Table 1 - Set point voltage vs. VID codes

## PIN DESCRIPTIONS

| PIN# | PIN SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 1 | V12 | This pin is connected to the 12 V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1μF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for the noise free operation. |
| 2 | Vid4 | This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V and when it switches to HI state the range is 2.0V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply. |
| 3 | Vid3 | MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply. |
| 4 | Vid2 | Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply. |
| 5 | Vid1 | Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply. |
| 6 | Vid0 | LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply. |
| 7 | PGood | This pin is an open collector output that switches LO when any of the outputs are outside of the specified under voltage trip point. It also switches low when Vsen1 pin is more than 10% above the DAC voltage setting. |
| 8 | V5 | 5V supply voltage. A high frequency capacitor (0.1 to 1μF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation. |
| 9 | SS | This pin provides the soft start for the switching regulator. An internal resistor charges an external capacitor that is connected from 5V supply to this pin which ramps up the outputs of the switching regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting. |

| PIN# | PIN SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 10 | Fault / Rt | This pin has dual function. It acts as an output of the OVP circuitry or it can be used to program the frequency using an external resistor. When used as a fault detector, if the switcher output exceed the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered as shown in the application circuit. |
| 11 | Fb2 | This pin provides the feedback for the internal LDO regulator which its output is Vout4. |
| 12 | Vin2 | This pin is the input that provides power for the internal LDO regulator. It is also monitored for the under-voltage and over-voltage conditions. |
| 13 | Vout2 | This pin is the output of the internal LDO regulator. |
| 14 | Gnd | This pin serves as the ground pin and must be connected directly to the ground plane. |
| 15 | Gate3 | This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator. |
| 16 | Fb3 | This pin provides the feedback for the linear regulator which its output drive is Gate3. |
| 17 | En | This pin is a TTL compatible Enable pin. When this pin is left open or pulled high, the device is enabled and when it is pulled low, it will disable the switcher and the LDO controller (Vout3) leaving the internal 200mA regulator operational. When signal is given to enable the device, both switcher and Vout3 will go through soft-start, the same as during start-up. |
| 18 | Fb1 | This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to Vout1 and Gnd to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from Vout1 to Fb1 must be less than 100Ω. |
| 19 | Vsen1 | This pin is internally connected to the Under-voltage and over-voltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply. |
| 20 | OCSet1 | This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the CS threshold depending on the $R_{DS}$ of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering. |
| 21 | PGnd | This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1μF) must be connected from V12 pin to this pin for noise free operation. |
| 22 | LGate1 | Output driver for the synchronous power MOSFET for the Core supply. |
| 23 | Phase1 | This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry. |
| 24 | UGate1 | Output driver for the high side power MOSFET for the Core supply. |

## BLOCK DIAGRAM

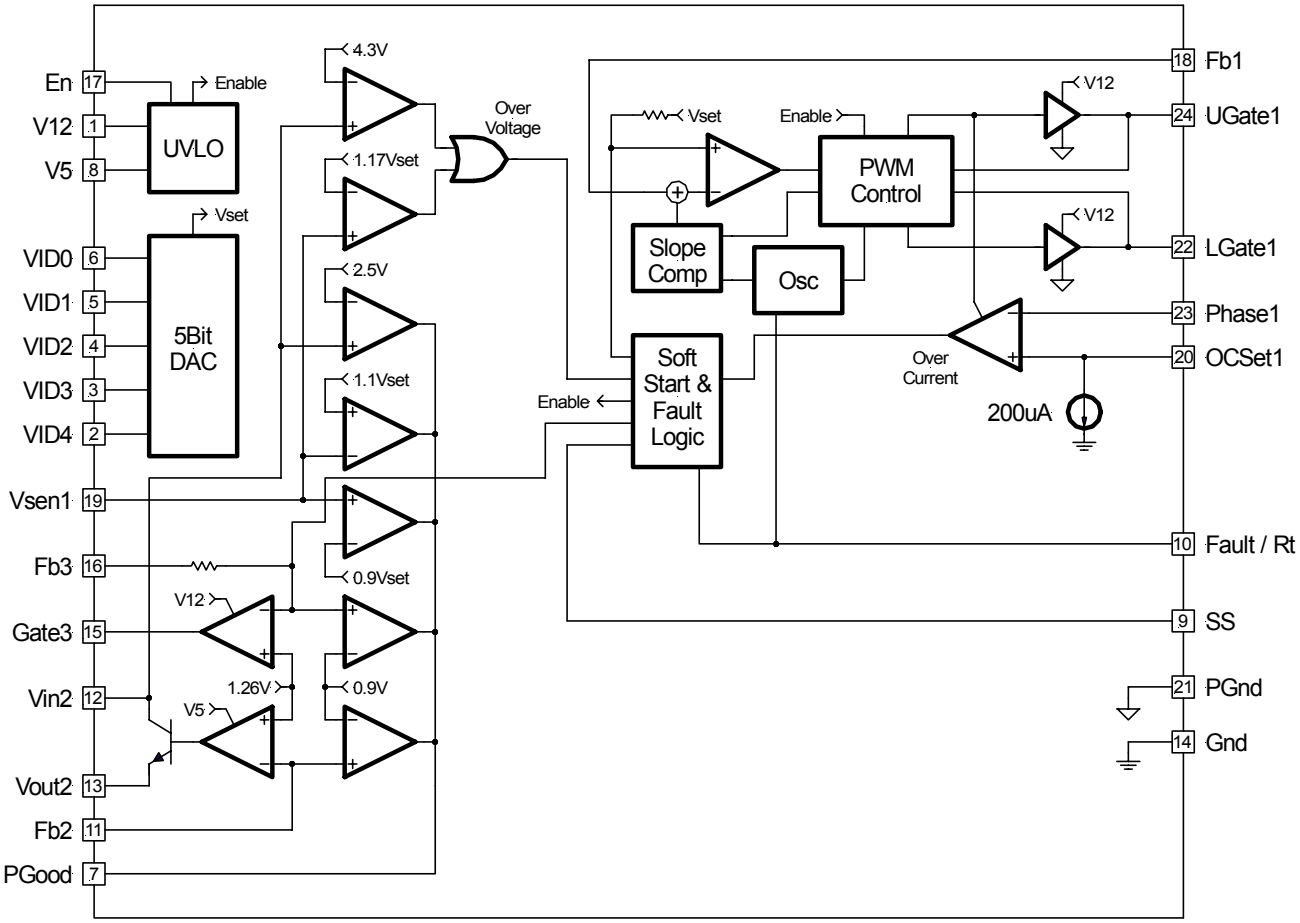



Figure 2 - Simplified block diagram of the IRU3018.

# TYPICAL APPLICATION

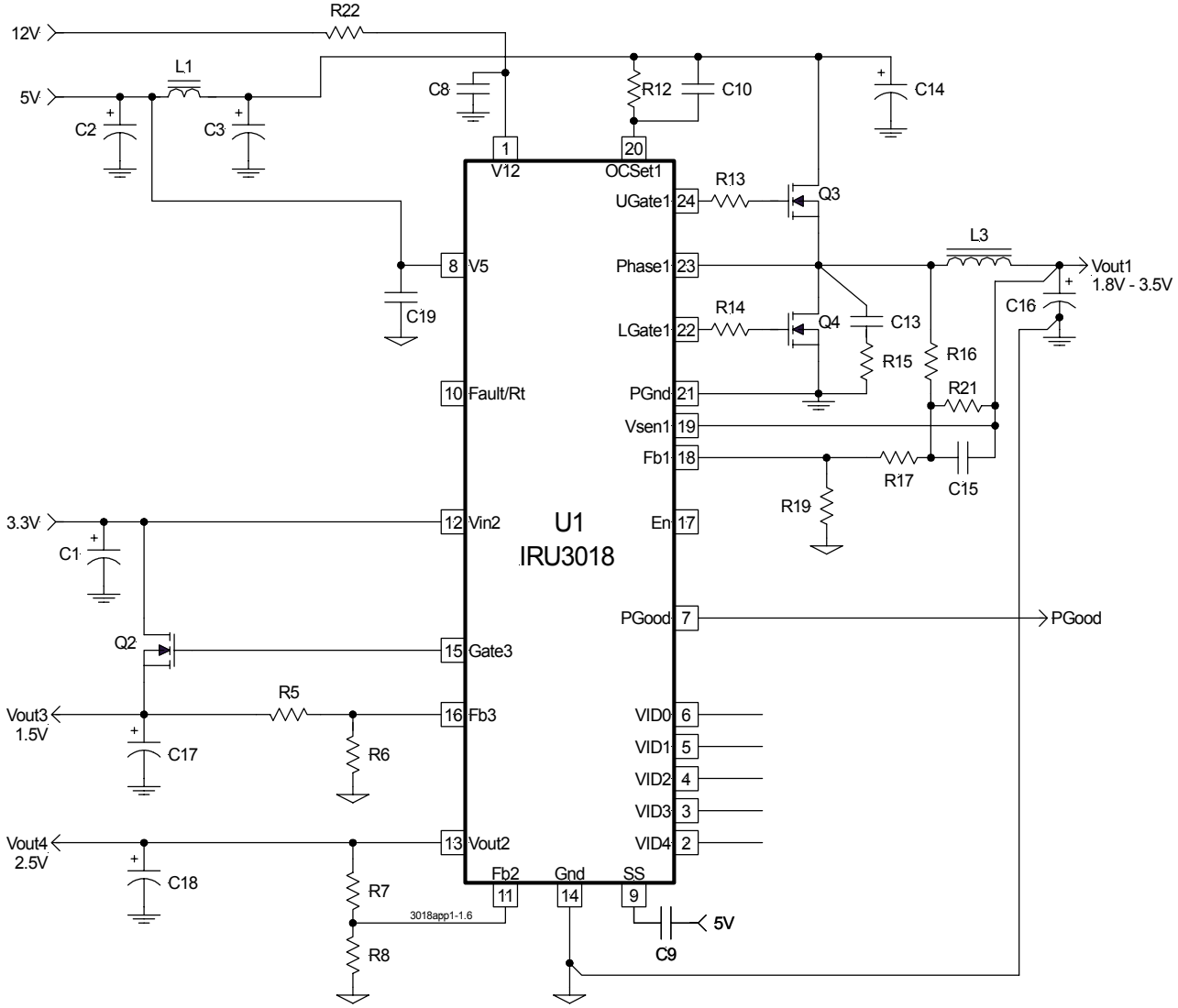



Figure 3 - Typical application of IRU3018 for an on board DC-DC converter providing power for the Vcore, GTL+ & Clock supply for the Deschutes and the next generation processor applications.

# IRU3018 APPLICATION PARTS LIST

| Ref Desig | Description | Qty | Part # | Manuf |
|---|---|---|---|---|
| Q2 | MOSFET | 1 | IRLR024, TO-252 package | IR |
| Q3 | MOSFET | 1 | IRL3103S, TO-263 package | IR |
| Q4 | MOSFET with Schottky | 1 | IRL3103D1S, TO-263 package | IR |
| L1 | Inductor | 1 | L=1μH, 5052 core with 4 turns of 1.0mm wire | Micro Metal |
| L3 | Inductor | 1 | L=2.7μH, 5052B core with 7 turns of 1.2mm wire | Micro Metal |
| C1,17 | Capacitor, Electrolytic | 2 | 6MV1000GX, 1000μF, 6.3V | Sanyo |
| C2 | Capacitor, Electrolytic | 1 | 10MV470GX, 470μF, 10V | Sanyo |
| C3 | Capacitor, Electrolytic | 1 | 10MV1200GX, 1200μF, 10V | Sanyo |
| C8 | Capacitor, Ceramic | 1 | 1μF, 0805 | |
| C9,15,19 | Capacitor, Ceramic | 3 | 1μF, 0603 | |
| C10 | Capacitor, Ceramic | 1 | 220pF, 0603 | |
| C13 | Capacitor, Ceramic | 1 | 1000pF, 0603 | |
| C14 | Capacitor, Electrolytic | 2 | 10MV1200GX, 1200μF, 10V | Sanyo |
| C16 | Capacitor, Electrolytic | 6 | 6MV1500GX, 1500μF, 6.3V | Sanyo |
| C18 | Capacitor, Electrolytic | 1 | 6MV150GX, 150μF, 6.3V | Sanyo |
| R5 | Resistor | 1 | 19.1Ω, 1%, 0603 | |
| R6,7,8 | Resistor | 3 | 100Ω, 1%, 0603 | |
| R12 | Resistor | 1 | 3.3KΩ, 5%, 0603 | |
| R13,14,15 | Resistor | 3 | 4.7Ω, 5%, 1206 | |
| R16,17,21 | Resistor | 3 | 2.2KΩ, 1%, 0603 | |
| R22 | Resistor | 1 | 10Ω, 5%, 0603 | |

# TYPICAL APPLICATION

**(Dual Layout with HIP6018)**

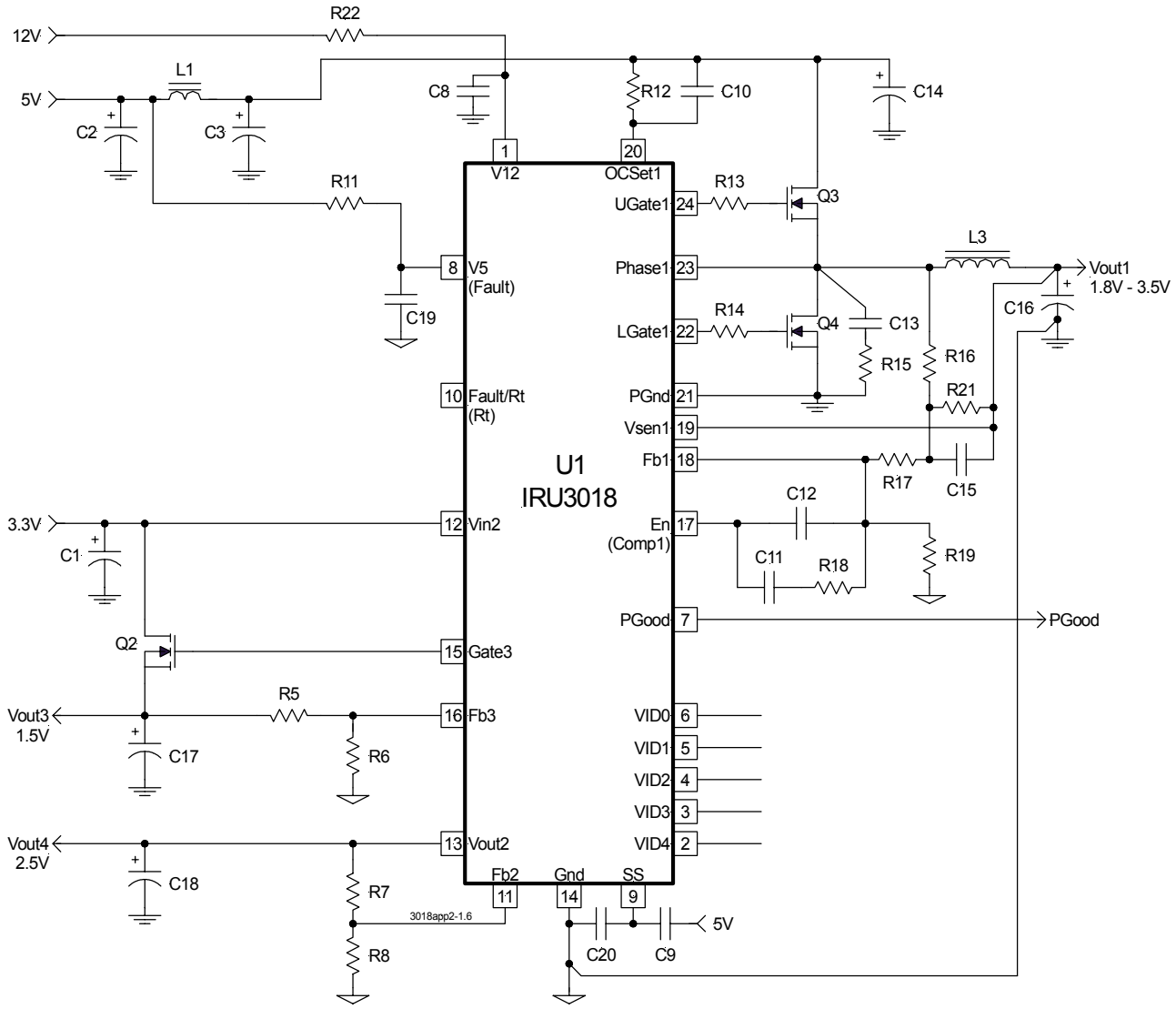



Figure 4 - Typical application of IRU3018 in a dual layout with HIP6018 for an on-board DC-DC converter providing power for the Vcore, GTL+ & Clock supply for the Deschutes and the next generation processor applications.

| Part # | R11 | R18 | C9 | C11 | C12 | C19 | C20 |
|---|---|---|---|---|---|---|---|
| HIP6018 | O | V | O | V | V | O | V |
| IRU3018 | S | O | V | O | O | V | O |

S - Short O - Open V - See IR or Harris parts list for the value

Table 2 - Dual layout component table. Components that need to be modified to make the dual layout work for IRU3018 and HIP6018.

# IRU3018 APPLICATION PARTS LIST

**Dual Layout with HIP6018**

| Ref Desig | Description | Qty | Part # | Manuf |
|---|---|---|---|---|
| Q2 | MOSFET | 1 | IRLR024, TO-252 package | IR |
| Q3 | MOSFET | 1 | IRL3103S, TO-263 package | IR |
| Q4 | MOSFET with Schottky | 1 | IRL3103D1S, TO-263 package | IR |
| L1 | Inductor | 1 | L=1μH, 5052 core with 4 turns of 1.0mm wire | Micro Metal |
| L3 | Inductor | 1 | L=2.7μH, 5052B core with 7 turns of 1.2mm wire | Micro Metal |
| C1,17 | Capacitor, Electrolytic | 2 | 6MV1000GX, 1000uF, 6.3V | Sanyo |
| C2 | Capacitor, Electrolytic | 1 | 10MV470GX, 470μF, 10V | Sanyo |
| C3 | Capacitor, Electrolytic | 1 | 10MV1200GX, 1200μF, 10V | Sanyo |
| C8 | Capacitor, Ceramic | 1 | 1μF, 0805 | |
| C9,15,19 | Capacitor, Ceramic | 3 | 1μF, 0603 | |
| C10 | Capacitor, Ceramic | 1 | 220pF, 0603 | |
| C11,12,20 | Capacitor, Ceramic | 3 | See Table 2, dual layout component 0603 × 3 | |
| C13 | Capacitor, Ceramic | 1 | 1000pF, 0603 | |
| C14 | Capacitor, Electrolytic | 2 | 10MV1200GX, 1200μF, 10V | Sanyo |
| C16 | Capacitor, Electrolytic | 6 | 6MV1500GX, 1500μF, 6.3V | Sanyo |
| C18 | Capacitor, Electrolytic | 1 | 6MV150GX, 150μF, 6.3V | Sanyo |
| R5 | Resistor | 1 | 19.1Ω, 1%, 0603 | |
| R6,7,8 | Resistor | 3 | 100Ω, 1%, 0603 | |
| R11 | Resistor | 1 | 0Ω, 0603 | |
| R12 | Resistor | 1 | 3.3kΩ, 5%, 0603 | |
| R13,14,15 | Resistor | 3 | 4.7Ω, 5%, 1206 | |
| R16,17,21 | Resistor | 3 | 2.2kΩ, 1%, 0603 | |
| R18 | Resistor | 1 | See Table 2, dual layout component 0603 × 1 | |
| R19 | Resistor | 1 | 220kΩ, 1%, 0603 | |
| R22 | Resistor | 1 | 10Ω, 5%, 0603 | |

# APPLICATION INFORMATION

An example of how to calculate the components for the application circuit is given below.

Assuming, two set of output conditions that this regulator must meet for Vcore:

a) Vo=2.8V, Io=14.2A, ΔVo=185mV, ΔIo=14.2A
b) Vo=2V, Io=14.2A, ΔVo=140mV, ΔIo=14.2A

The regulator design will be done such that it meets the worst case requirement of each condition.

**Output Capacitor Selection**

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as:

$$ESR \leq \frac{100}{14.2} = 7m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX, 1500μF, 6.3V has an ESR of less than 36mΩ typical. Selecting 6 of these capacitors in parallel has an ESR of ≈ 6mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic FA series or the Nichicon PL series.

**Reducing the Output Capacitors Using Voltage Level Shifting Technique**

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3018 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by half the total trace resistance. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ then after level shifting the new ESR will only need to be 8.5mΩ if the trace resistance is 5mΩ (7+5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$Rs \leq 2 \times (Vspec - 0.02 \times Vo - \Delta Vo) / \Delta I$$

Where:

Rs = Total maximum trace resistance allowed
Vspec = Intel total voltage spec
Vo = Output voltage
ΔVo = Output ripple voltage
ΔI = load current step

For example, assuming:

Vspec = ±140mV = ±0.1V for 2V output
Vo = 2V
ΔVo = assume 10mV = 0.01V
ΔI = 14.2A

Then the Rs is calculated to be:

$$Rs \leq 2 \times (0.140 - 0.02 \times 2 - 0.01) / 14.2 = 12.6m\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6mΩ, the power dissipated is:

$$Io^2 \times Rs = 14.2^2 \times 12.6 = 2.54W$$

This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6 of the 1500μF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously effect the life time of the output capacitors.

**Output Inductor Selection**
The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step.

However, if the inductor is too small, the output ripple current and ripple voltage become too large. One solution to bring the ripple current down is to increase the switching frequency, however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve the optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation:

$$L = ESR \times C \times [Vin(min) - Vo(max)] / ( 2 \times \Delta I )$$

Where :

Vin(min) = Minimum input voltage
For Vo=2.8V, $\Delta$I=14.2A

$$L = 0.006 \times 9000 \times (4.75 - 2.8) / (2 \times 14.2) = 3.7\mu H$$

Assuming that the programmed switching frequency is set at 200KHz, an inductor is designed using the Micrometals' Powder Iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wound with 8 turns of #16 AWG wire, resulting in 3$\mu$H inductance with $\approx$ 3m$\Omega$ of DC resistance.

Assuming L=3$\mu$H and Fsw=200KHz (switching frequency), the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

T $\equiv$ Switching Period
D $\equiv$ Duty Cycle
Vsw $\equiv$ High-side MOSFET ON Voltage
$R_{DS} \equiv$ MOSFET On-resistance
Vsync $\equiv$ Synchronous MOSFET ON Voltage
$\Delta$Ir $\equiv$ Inductor Ripple Current
$\Delta$Vo $\equiv$Output Ripple Voltage

$$T = 1 / Fsw$$

$$Vsw = Vsync = Io \times R_{DS}$$

$$D \approx (Vo + Vsync) / (Vin - Vsw + Vsync)$$

$$Ton = D \times T$$

$$Toff = T - Ton$$

$$\Delta Ir = (Vo + Vsync) \times Toff / L$$

$$\Delta Vo = \Delta Ir \times ESR$$

In our example for Vo=2.8V and 14.2 A load, assuming IRL3103 MOSFET for both switches with maximum on resistance of 19m$\Omega$, we have:

$T = 1 / 200000 = 5\mu s$
$Vsw = Vsync = 14.2 \times 0.019 = 0.27V$
$D \approx (2.8 + 0.27) / (5 - 0.27 + 0.27) = 0.61$
$Ton = 0.61 \times 5 = 3.1\mu s$
$Toff = 5 - 3.1 = 1.9\mu s$
$\Delta Ir = (2.8 + 0.27) \times 1.9 / 3 = 1.94A$
$\Delta Vo = 1.94 \times 0.006 = 0.011V = 11mV$

**Power Component Selection**
Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high-side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$Dmax \approx (2.8 + 0.27) / (4.75 - 0.27 + 0.27) = 0.65$
$P_{DH} = Dmax \times Io^2 \times R_{DS(max)}$
$P_{DH} = 0.65 \times 14.2^2 \times 0.029 = 3.8W$
$R_{DS(max)}$ = Maximum $R_{DS(on)}$ of the MOSFET at 125°C

For synch MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$Dmin \approx (2 + 0.27) / (5.25 - 0.27 + 0.27) = 0.43$
$P_{DS} = (1-Dmin) \times Io^2 \times R_{DS(max)}$
$P_{DS} = (1 - 0.43) \times 14.2^2 \times 0.029 = 3.33$ W

**Heat Sink Selection**
Selection of the heat sink is based on the maximum allowable junction temperature of the MOSFETS. Since we previously selected the maximum $R_{DS(on)}$ at 125°C, then we must keep the junction below this temperature. Selecting TO-220 package gives $\theta_{JC}$=1.8°C/W (from the venders' data sheet) and assuming that the selected heat sink is black anodized, the heat-sink-to-case thermal resistance is: $\theta$cs=0.05°C/W, the maximum heat sink temperature is then calculated as:

$$Ts = T_J - P_D \times (\theta_{JC} + \theta cs)$$

$$Ts = 125 - 3.82 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance ($\theta_{SA}$) is calculated as follows:

Assuming $T_A$ = 35°C:

$\Delta T = Ts - T_A = 118 - 35 = 83°C$
Temperature Rise Above Ambient

$$\theta_{SA} = \Delta T / P_D = 83 / 3.82 = 22°C/W$$

Next, a heat sink with lower $\theta_{SA}$ than the one calculated in the previous step must be selected. One way to do this is to look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" given in the heat sink manufacturers' catalog and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

| Co. | Part # |
|---|---|
| Thermalloy | 6078B |
| AAVID | 577002 |

Following the same procedure for the Schottky diode results in a heat sink with $\theta_{SA}$=25°C/W. Although it is possible to select a slightly smaller heat sink, for simplicity the same heat sink as the one for the high side MOSFET is also selected for the synchronous MOSFET.

**Switcher Current Limit Protection**

The IRU3018 uses the MOSFET $R_{DS(on)}$ as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "OCSet1" terminal of the IC as shown in the application circuit. For example, if the desired current limit point is set to be 22A, for the synchronous and 16A for the non-synchronous, and from our previous selection, the maximum MOSFET $R_{DS(on)}$=19mΩ, then the current sense resistor Rcs is calculated as:

$$Vcs = I_{CL} \times R_{DS} = 22 \times 0.019 = 0.418V$$
$$Rcs = Vcs / I_B = (0.418V) / (200\mu A) = 2.1K\Omega$$

Where:

$I_B$ = 200μA is the internal current setting of the IRU3018

**Switcher Frequency Selection**

The IRU3018 frequency is internally set at 200KHz with no external timing resistor. However, it can be adjusted up by using an external resistor from Rt pin to Gnd or can be adjusted down if the resistor is connected to the 12V supply.

**1.5V, GTL+ Supply LDO Power MOSFET Selection**

The first step in selecting the power MOSFET for the 1.5V linear regulator is to select its maximum $R_{DS(on)}$ of the pass transistor based on the input to output Dropout voltage and the maximum load current.

$$R_{DS(max)} = (Vin - Vo) / I_L$$

For Vo = 1.5V, Vin = 3.3V and, $I_L$ = 2A

$$R_{DS(max)} = (3.3 - 1.5) / 2 = 0.9\Omega$$

Note that since the MOSFETs $R_{DS(on)}$ increases with temperature, this number must be divided by ≈ 1.5, in order to find the $R_{DS(on)}$ max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω $R_{DS(on)}$ at room temperature, which meets our requirement.

To select the heat sink for the LDO MOSFET, first calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.

$$P_D = (Vin - Vo) \times I_L$$

Where:

$P_D$ = Power Dissipation of the Linear Regulator
$I_L$ = Linear Regulator Load Current

For the 1.5V and 2A load:

$$P_D = (3.3 - 1.5) \times 2 = 3.6W$$

Assuming $T_J$(max) = 125°C:

$$Ts = T_J - P_D \times (\theta_{JC} + \theta cs)$$
$$Ts = 125 - 3.6 \times (1.8 + 0.05) = 118°C$$

With the maximum heat sink temperature calculated in the previous step, the heat-sink-to-air thermal resistance ($\theta_{SA}$) is calculated as follows:

Assuming $T_A$ = 35°C:

$\Delta T$ = Ts - Ta = 118 - 35 = 83 °C
Temperature Rise Above Ambient

$$\theta_{SA} = \Delta T / P_D = 83 / 3.6 = 23°C/W$$

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator.

**2.5V, Clock Supply**

The IRU3018 provides an internal ultra low dropout regulator with a minimum of 200mA current capability that converts 3.3V supply to a programmable regulated 2.5V supply to power the clock chip. The internal regulator has short circuit protection with internal thermal shutdown.

**1.5V and 2.5V Supply Resistor Divider Selection**

Since the internal voltage reference for the linear regulators is set at 1.26V for IRU3018, there is a need to use external resistor dividers to step up the voltage. The resistor dividers are selected using the following equations:

$$Vo = (1 + Rt/R_B) \times Vref$$

Where:

Rt = Top resistor divider
$R_B$ = Bottom resistor divider
Vref = 1.26V typical

For 1.5V supply
Assuming $R_B$=100Ω:

$Rt = R_B \times [(Vo/Vref) - 1]$
$Rt = 100 \times [(1.5/1.26) - 1] = 19.1\Omega$

For 2.5V supply
Assuming $R_B$=200Ω:

$Rt = R_B \times [(Vo/Vref) - 1]$
$Rt = 200 \times [(2.5/1.26) - 1] = 197\Omega$

Select Rt=200Ω

**Switcher Output Voltage Adjust**
As it was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the Gnd pin of the IRU3018 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider (R17 in the application circuit) is set at 100Ω, and the R19 is calculated. For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R19 is calculated using the following formula:

$R19 = 100 \times [V_{DAC}/(Vo - 1.004 \times V_{DAC})]$ (Ω)
$R19 = 100 \times [2.8/(2.835 - 1.004 \times 2.800)] = 11.76K\Omega$

Select 11.8KΩ, 1%

**Note:** The value of the top resistor must not exceed 100Ω. The bottom resistor can then be adjusted to raise the output voltage.

**Soft-Start Capacitor Selection**
The soft-start capacitor must be selected such that during the start-up when the output capacitors are charging up, the peak inductor current does not reach the current limit threshold. A minimum of 1μF capacitor insures this for most applications. An internal resistor charges the soft-start capacitor which slowly ramps up the inverting input of the PWM comparator Vfb3. This insures the output voltage to ramp at the same rate as the soft-start cap thereby limiting the input current. For example, with 1μF of soft-start capacitor, the ramp up rate is approximated to be 1V/20ms. For example if the output capacitance is 9000μF, the maximum start up current will be:

$I = 9000\mu F \times (1V/20ms) = 0.45A$

The other function of the soft-start cap is to provide an off time between the current limit cycles(HICCUP) in order for the synchronous MOSFET to cool off and survive the short circuit condition. The off time between the current limit cycles is approximated as:

$T_{HICCUP} = 60 \times Css$ (ms)
For example if Css=1μF, $T_{HICCUP} = 60 \times 1 = 60ms$

**Input Filter**
It is recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3μH will be sufficient in this type of application.

**External Shutdown**
The best way to shutdown the IRU3018 is to pull down on the soft-start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

**Layout Considerations**
Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.

Start the layout by first placing the power components:

1) Place the input capacitor C14 and the high-side MOSFET, Q3 as close to each other as possible.

2) Place the synchronous MOSFET, Q4 and the Q3 as close to each other as possible with the intention that the source of Q3 and drain of the Q4 has the shortest length.

3) Place the snubber R15 & C13 between Q4 & Q3.

4) Place the output inductor, L3 and the output capacitors, C16 between the mosfet and the load with output capacitors distributed along the slot 1 and close to it.

5) Place the bypass capacitors, C8 and C19 right next to 12V and 5V pins. C8 next to the 12V, pin 1 and C19 next to the 5V, pin 8.

6) Place the IRU3018 such that the PWM output drives, pins 24 and 22 are relatively short distance from gates of Q3 and Q4.

7) Place all resistor dividers close to their respective feedback pins.

8) Place the 2.5V output capacitor, C18 close to the pin 13 of the IC and the 1.5V output capacitor, C17 close to the Q2 MOSFET.

   **Note:** It is better to place the 1.5V linear regulator components close to the 3018 and then run a trace from the output of the regulator to the load. However, if this is not possible then the trace from the linear drive output pin, pin 16 must be run away from any high frequency data signals.

   It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.

9) Place R12 and C10 close to pin 20

10) Place C9 close to pin 9

Component connections:

**Note:** It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using the 4 layer board, dedicate on layer to ground, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible for the 2.5V.

Connect all grounds to the ground plane using direct vias to the ground plane.

Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side.

a) C14 to Q3 Drain
b) Q3 Source to Q4 Drain
c) Q4 drain to L3
d) L3 to the output capacitors, C16
e) C16 to the load, slot 1
f) Input filter L1 to the C16 and C3
g) C1 to Q2 drain
h) C17 to the Q2 source
I) A minimum of 0.2 inch width trace from the C18 capacitor to pin 13

Connect the rest of the components using the shortest connection possible.

# IRU3018 APPLICATION PARTS LIST

**Dual Layout with HIP6016**

| Ref Desig | Description | Qty | Part # | Manuf |
|---|---|---|---|---|
| Q3,4 | MOSFET | 2 | IRL3103<br>IRL3103S (Note 1) | <br>IR |
| Q5 | MOSFET, GP | 1 | 2N7002 | Motorola |
| Q2 | MOSFET | 1 | MTP3055VL, TO-263 package | Motorola |
| L1 | Inductor | 1 | L=1μH | Micro Metal |
| L3 | Inductor | 1 | Core: L=2μH, R=2mΩ | Micro Metal |
| C16 | Capacitor, Electrolytic | 6 | 6MV1500GX, 1500μF, 6.3V, | Sanyo |
| C14 | Capacitor, Electrolytic | 2 | 6MV1500GX, 1500μF, 6.3V, | Sanyo |
| C3 | Capacitor, Electrolytic | 1 | 6MV1500GX, 1500μF, 6.3V, | Sanyo |
| C18 | Capacitor, Electrolytic | 1 | 220μF, 6.3V, ECAOJFQ221 | Panasonic |
| C17,C1 | Capacitor, Electrolytic | 2 | 680μF, 10V, EEUFA1A681L | Panasonic |
| C2 | Capacitor, Electrolytic | 1 | 680μF, 10V, EEUFA1A681L | Panasonic |
| C8,19 | Capacitor, Ceramic | 2 | 0805Z105P250NT<br>1μF, 25V, Z5U, 0805 SMT | Novacap |
| C9 | Capacitor , Ceramic | 1 | 0805Z105P250NT<br>1μF, 25V, Z5U, 0805 SMT<br>See Table 2, Dual layout component | Novacap |
| C10 | Capacitor, Ceramic | 1 | 220pF, SMT 0805 size | |
| C13 | Capacitor, Ceramic | 1 | 470pF, SMT 0805 size | |
| C9,11, 12,15,20 | | | See Table 2, Dual layout component | |
| R12 | Resistor | 1 | 2.21KΩ, 1%, SMT 0805 size | |
| R13,14 | Resistor | 2 | 10Ω, 5%, SMT 1206 size | |
| R15 | Resistor | 1 | 10Ω, 5%, SMT 1206 size | |
| R20 | Resistor | 1 | 10kΩ, 5%, SMT 0805 size | |
| R6 | Resistor | 1 | 100Ω, 1%, SMT 0805 size | |
| R8 | Resistor | 1 | 200Ω, 1%, SMT 0805 size | |
| R5 | Resistor | 1 | 19.1Ω, 1%, SMT 0805 size | |
| R7 | Resistor | 1 | 200Ω, 1%, SMT 0805 size | |
| R17 | Resistor | 1 | 100Ω, 1%, SMT 0805 size | |
| R19 | Resistor | 1 | 10kΩ, 1%, SMT 0805 size | |
| HS3,4 | Q1,3,4 Heatsink | 2 | 6270 | Thermalloy |
| R11,16,18, 21, 22 | | | See Table 2, Dual layout component | |

**Note 1:** For the applications where it is desirable not to use the Heat sink, the IRL3103S MOSFET in the TO-263 SMT package with 1" square of pad area using top and bottom layers of the board as a minimum is required.

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