

Low Power 32-Bit Mobile Embedded Controller

Product Features

- 3.3V Operation
- ACPI Compliant
- LPC Interface
 - Supports LPC Bus frequencies of 19.2MHz to 33MHz
- VTR (standby) and VBAT Power Planes
 - Low Standby Current in Sleep Mode
- Configuration Register Set
 - Compatible with ISA Plug-and-Play Standard
 - EC-Programmable Base Address
- ARC-625D Embedded Controller (EC)
 - 16 KB Single Cycle 32-bit Wide Dual-ported SRAM, Accessible as Closely Coupled Data Memory and Instruction Memory
 - 4KB Boot ROM
 - 32 x 32 → 64 Fast Multiply
 - Divide Assist and Saturation Arithmetic
 - Maskable Interrupt Aggregator/Accelerator Interface
 - Maskable Hardware Wake-Up Events
 - Sleep mode
 - JTAG Debug Port, Includes JTAG Master
 - MCU Serial Debug Port
 - 1μS Delay Register
 - 10-Channel DMA Interface Supports SMBus Controllers and EC/Host GP-SPI Controllers
- Embedded Flash
 - 192 KB user space, 32-bit Access, 10 K Cycles Endurance
 - Flash Security Enhancements
 - 4K Boot Block Protection
 - Direct JTAG and Direct LPC-protected (2) Pages at or Near Top of Memory for Password Protection
 - Multiple Flash Programming Options
 - JTAG programmable
 - BIOS programmable
 - Programmable by EC at Power-on Using UART
 - Programmable on a Gang Programmer via Gang-programmer Interface
- Embedded Non-volatile Read/Write Memory
 - 2 KB of EEPROM, Single Byte Access, 250K Cycles Endurance
 - 8-byte Block Erasable, 128 Blocks
 - Independent of main Flash memory
- Legacy Support
 - Fast GATEA20 & Fast CPU_RESET
- System to EC Message Interface
 - 8042 Style Host Interface
 - Embedded Memory Interface
 - Host Serial or Parallel IRQ Source
 - Provides Two Windows to On-Chip SRAM for Host Access
 - Two Register Mailbox Command Interface
 - Host Access of Virtual Registers Without EC Intervention
 - Mailbox Registers Interface
 - Thirty-two 8-Bit Scratch Registers
 - Two Register Mailbox Command Interface
 - Two Register SMI Source Interface
 - ACPI Embedded Controller Interface
 - Four Instances
 - 1 or 4 Byte Data transfer capable
 - Full-duplex Register Access
 - ACPI Power Management Interface
 - SCI Event-Generating Functions
- Battery Backed Resources
 - Power-Fail Status Register
 - 32 KHz Clock Generator
 - Week Alarm Timer Interface with Programmable Wake-up from 1ms to 45 Days
 - VBAT-Powered Control Interface
 - Six Wake-up Input Signals
 - Optional Latching of Wake-up Inputs
 - VBAT-Backed 64 Byte Memory
- Four EC-based SMBus 2.0 Host Controllers
 - Allows Master or Dual Slave Operation
 - Controllers are Fully Operational on Standby Power
 - DMA-driven I²C Network Layer Hardware
 - I²C Datalink Compatibility Mode
 - Multi-Master Capable
 - Supports Clock Stretching
 - Programmable Bus Speed up to 400KHz
 - Hardware Bus Access "Fairness" Interface
 - SMBus Time-outs Interface
 - AMD-TSI Port
 - 12 Ports Assignable to Any Controller
 - 3 SMBus Isolation Switches
 - Three Pairs of Ports Can Be Joined
- PECI Interface 3.0
- 18 x 8 Interrupt Capable Multiplexed Keyboard Scan Matrix
 - Optional Push-Pull Drive for Fast Signal Switching

- Three independent Hardware Driven PS/2 Ports
 - Fully functional on Main and/or Suspend Power
 - PS/2 Edge Wake Capable
- General Purpose I/O Pins
 - 135 GPIOs
 - 8 GPIO Pass-Through Port (GTPP)
 - Glitch protection on all GPIO pins
 - 6 Battery-powered General Purpose Outputs
- Low Power Programmable LED Interface
 - Supports three modes of operation:
 - Blinking Mode with Programmable Blink Rates
 - Breathing LED Output
 - 8-bit PWM
 - Breathing LED Supports Piecewise-linear Brightness Curves, Symmetric or Asymmetric
 - Supports Low Power Operation in Blinking and Breathing Modes
 - Operates on Standby Power
 - Operates in Chip's System Deepest Sleep State on 32kHz standby clock
 - Operational in EC Sleep State
 - Provides Three LED pins
 - LED pin buffers capable of sinking up to 20 mA
- Programmable 16-bit Counter/Timer Interface
 - Four Wake-capable 16-bit Auto-reloading Counter/Timer Instances
 - Four Operating Modes per Instance: Timer, One-shot, Event and Measurement
 - 4 External Inputs, 4 External Outputs
- Hibernation Timer Interface
 - Two 32.768 KHz Driven Timers
 - Programmable Wake-up from 0.5ms to 128 Minutes
- System Watch Dog Timer (WDT)
- Input Capture and Compare Timer
 - 32-bit Free-running timer
 - Six 32-bit Capture Registers
 - Two 32-bit Compare Registers
 - Capture, Compare and Overflow Interrupts
- BC-Link™ Interconnection Bus
 - Two High Speed and one Low Speed Bus Masters Controllers
- Two General Purpose Serial Peripheral Interface Controllers (ECGP-SPI)
 - One 3-pin EC-driven Full Duplex Serial Communication Interface
 - One 4-pin EC/Host-driven Full Duplex Serial Communication Interface to SPI Flash Interface
 - Flexible Clock Rates
 - SPI Burst Capable
- FAN Support
 - Six Programmable Pulse-Width Modulator (PWM) Outputs
 - Multiple Clock Rates
 - 16-Bit 'On' & 16-Bit 'Off' Counters
 - Six Fan Tachometer Inputs
- 6 x 2 Capture/Compare Timer Interface
- ADC Interface
 - 10-bit Conversion in 10µs
 - 16 Channels
 - Integral Non-Linearity of ± 0.5 LSB; Differential Non-Linearity of ± 0.5 LSB
- 2-Pin Debug Port with Standard 16C550 Register Interface
 - Accessible from Host and EC
 - Programmable Input/output Pin Polarity Inversion
 - Programmable Main Power or Standby Power Functionality
- Port 80h Debug Ports for BIOS Debug
 - Two Ports, Assignable to Any LPC IO Address
 - 24-bit Timestamp with Adjustable Timebase
 - 16-Entry FIFO
- Resistor/Capacitor Identification Detection (RC_ID)
 - Single Pin Interface to External Inexpensive RC Circuit
 - Replacement for Multiple GPIO's
 - Provides 8 Quantized States on One Pin
- Integrated Standby Power Reset Generator
 - Reset Input Pin
 - Reset Output Pin
- HDMI Consumer Electronics Control (CEC) Bus Controller
- Thermal Monitoring
 - Monitors Temperatures with up to Six External Diodes and one Internal Diode
 - Three Parallel and Three Anti-parallel Diodes Supported on 6 Pins
 - $\pm 1^{\circ}\text{C}$ Accuracy 60°C to 100°C
 - Resistance Error Correction
 - Beta Compensation for Processor Diodes
 - Voltage Programmable Fail-Safe Monitor
 - Thermal Shutdown Temperature Set by a Single External 1% Resistor
 - Can Use Either a Remote Diode or Thermistor
- Clock Generator
 - 32.768KHz Clock Source
 - Low power 32KHz crystal oscillator
 - Optional use of a crystal-free silicon oscillator with $\pm 2\%$ Accuracy
 - Optional use of 32.768 KHz input Clock
 - Operational on Suspend Power
- Programmable Clock Power Management Control & Distribution
 - 20.27 MHz silicon oscillator, $\pm 2\%$ Accuracy
- Real Time Clock
- Package
 - 169 Pin LFBGA RoHS Compliant package

Tool Requirements

For information on the latest version of the Metaware Development system, please see Application Note #26.14, "ARC Metaware Development System."

Description

The MEC1633 is the mixed signal base component of a multi-device advanced I/O controller architecture. The MEC1633 incorporates a high-performance 32-bit ARC 625D embedded microcontroller with a 192 Kilobyte Embedded Flash Subsystem, 16 Kilobytes of SRAM, 1 Kilobyte EEPROM emulation, and a 2 Kilobyte EEPROM. The MEC1633 communicates with the system host using the Intel® Low Pin Count bus.

The MEC1633 is the EC Base Component of a split-architecture Advanced I/O Controller system which uses BC-Link communication protocol to access up to three companion components. The BC-Link protocol is peer-to-peer providing communication between the MEC1633 embedded controller and registers located in a companion.

The MEC1633 is directly powered by two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on" and system power management functions. The MEC1633 also contains an integrated VTR Reset Interface and a system Power Management Interface that supports low-power states and can drive state changes as a result of hardware wake events as defined by the MEC1633 Wake Interface.

The MEC1633 defines a software development system interface that includes an MCU Serial Debug Port, a two pin serial debug port with a 16C550A register interface that is accessible to the EC or to the LPC host and can operate up to 2 MB/s, a flexible Flash programming interface, a Port 80 BIOS Debug Port, Gang Programmer Interface, and a JTAG interface. The EC can also drive the JTAG interface as a master.

A top-level block diagram of the MEC1633 is shown in [Figure 1](#).

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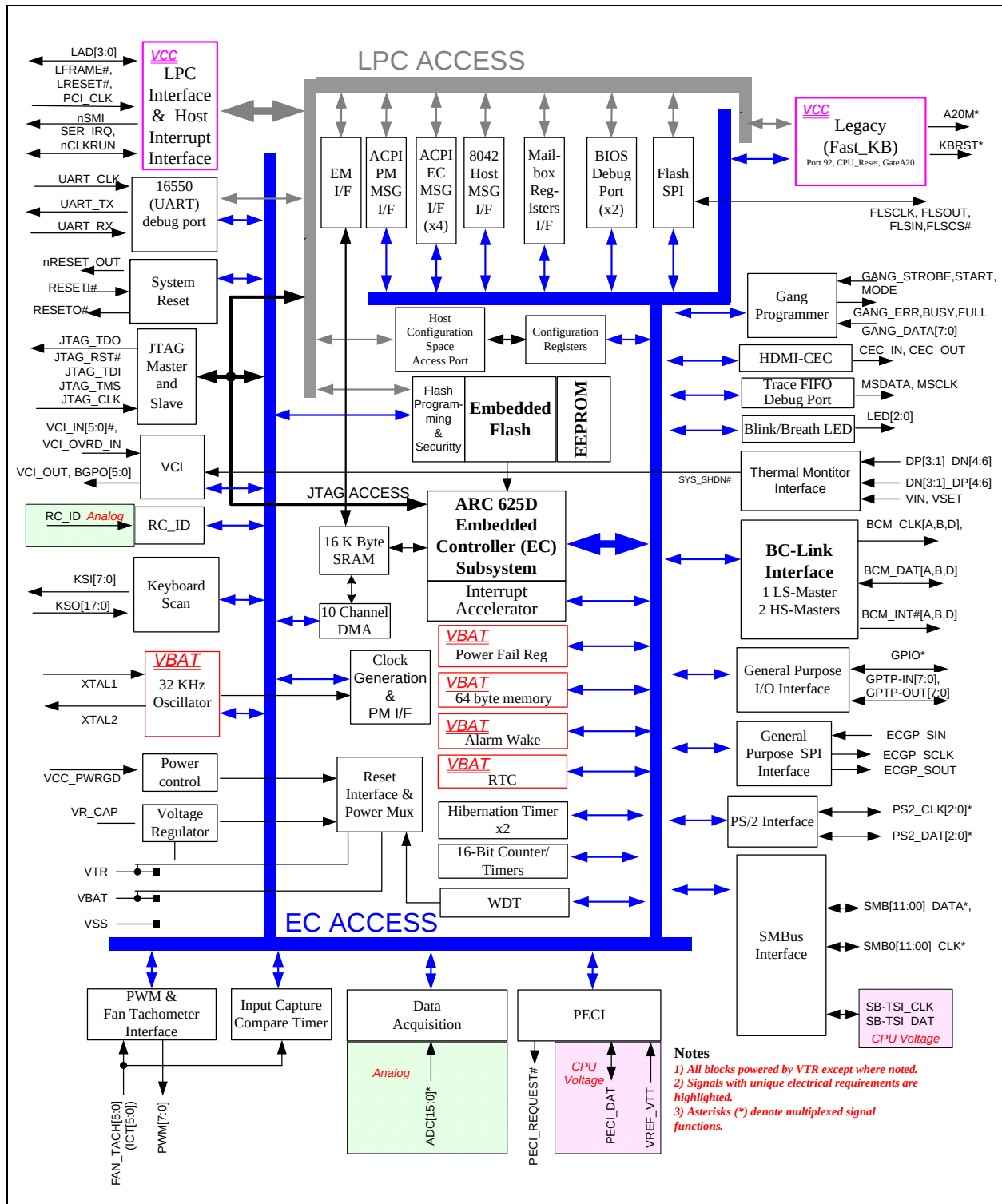
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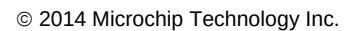
BLOCK DIAGRAM

FIGURE 1: MEC1633 TOP-LEVEL BLOCK DIAGRAM



PACKAGE OUTLINE

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001775B (08-19-14)	Product Features	Added to LPC bullet: "Supports LPC Bus frequencies of 19.2MHz to 33MHz"
DS00001775A (06-16-14)	Document Release	

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