OKI Semiconductor

This version: Aug. 1998
Previous version: Nov. 1996

MSM7507-01/02/03

Single Rail CODEC

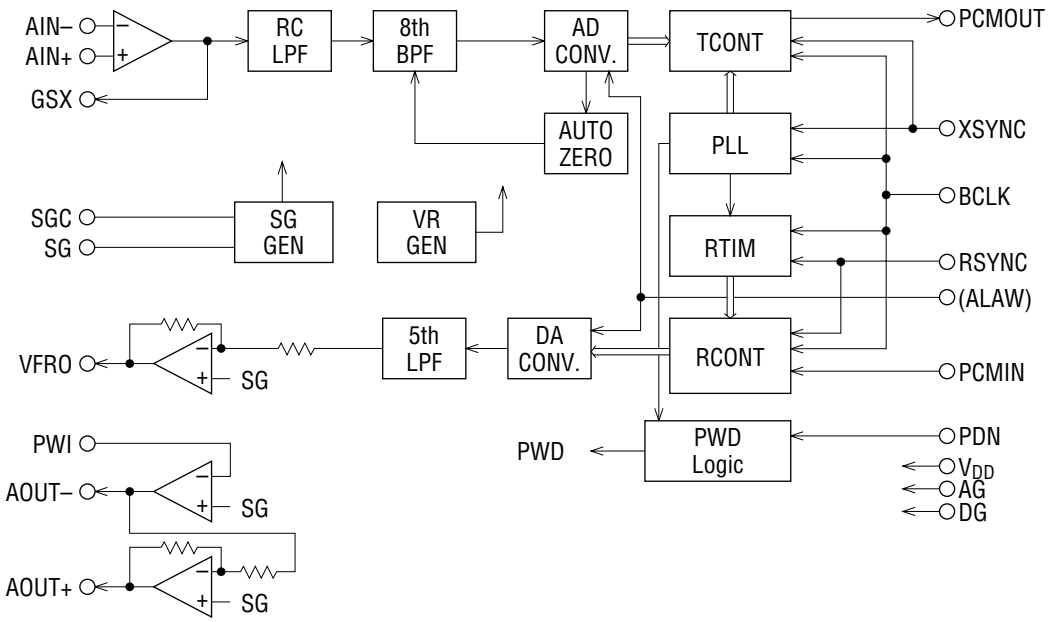
GENERAL DESCRIPTION

The MSM7507 is a single-channel CODEC CMOS IC for voice signals ranging from 300 to 3400 Hz with filters for A/D and D/A conversion.
Designed especially for a single-power supply and low-power applications, the device is optimized for ISDN terminals, digital wireless systems, and digital PBX systems.
The device uses the same transmission clocks as those used in the MSM7508B and MSM7509B.
The analog output signal, which is of a differential type and can drive a 600 Ω load, can directly drive a handset receiver.

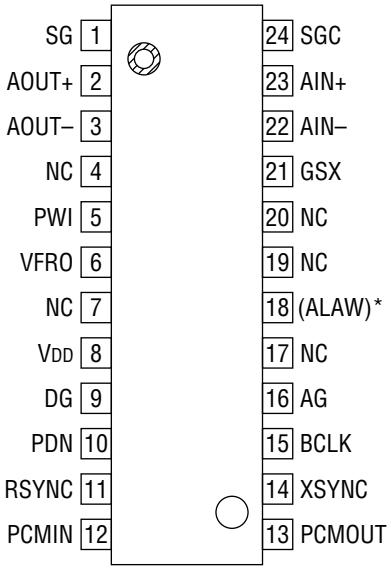
FEATURES

- Single power supply: +5 V ±5%
- Low power consumption
  Operating mode: 20 mW Typ. 40 mW Max. V_{DD} = 5 V
  Power down mode: 0.03 mW Typ. 0.3 mW Max. V_{DD} = 5 V
- ITU-T Companding law
  MSM7507-01: μ/A-law pin selectable
  MSM7507-02: μ-law
  MSM7507-03: A-law
- Transmission characteristics conforms to ITU-T G.714
- Built-in PLL eliminates a master clock
- Serial data rate: 64/128/256/512/1024/2048 kHz
  96/192/384/768/1536/1544/200 kHz
- Adjustable transmit gain
- Adjustable receive gain
- Built-in reference voltage supply
- Analog output can directly drive a 600 Ω line transformer
- The 24-Pin SOP package products provide pin compatibility with the MSM7543/7544
- The 20-Pin SSOP package products have 1/3 the foot print of conventional products
- Package options:
  24-pin plastic SOP (SOP24-P-430-1.27-K) (Product name : MSM7507-01GS-K)
  (Product name : MSM7507-02GS-K)
  (Product name : MSM7507-03GS-K)
  20-pin plastic SSOP (SSOP20-P-250-0.95-K) (Product name : MSM7507-01MS-K)
  (Product name : MSM7507-02MS-K)
  (Product name : MSM7507-03MS-K)

BLOCK DIAGRAM

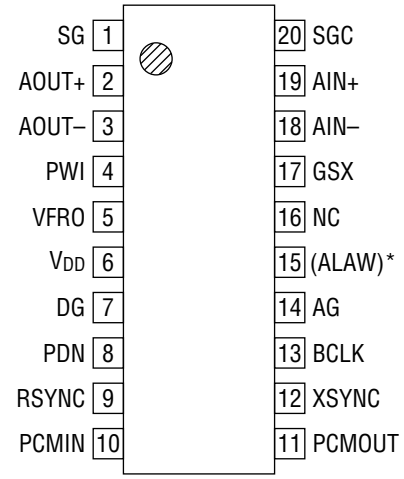


PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

24-Pin Plastic SOP



NC : No connect pin

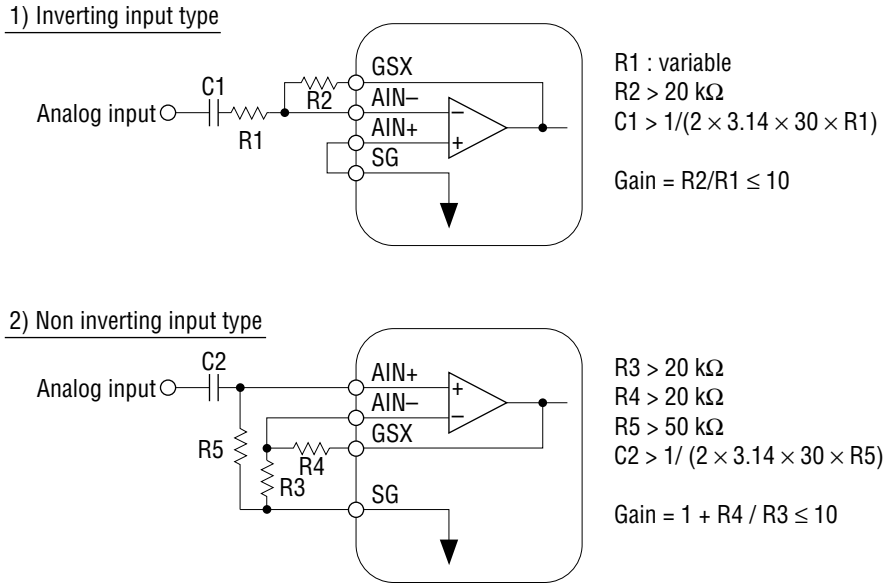
20-Pin Plastic SSOP

* The ALAW pin is only applied to the MSM7507-01GS-K/MSM7507-01MS-K.

PIN AND FUNCTIONAL DESCRIPTIONS

AIN+, AIN–, GSX

Transmit analog input and transmit level adjustment.
AIN+ is a non-inverting input to the op-amp; AIN– is an inverting input to the op-amp; GSX is connected to the output of the op-amp and is used to adjust the level, as shown below.
When not using AIN– and AIN+, connect AIN– to GSX and AIN+ to SG. During power saving and power down modes, the GSX output is at AG voltage.



AG

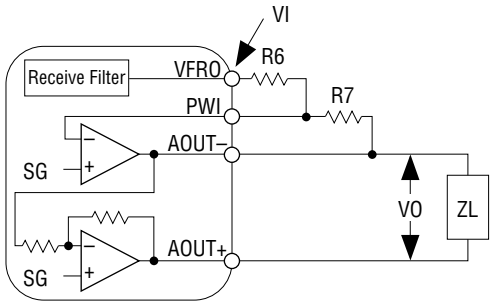
Analog signal ground.

VFRO

Receive filter output.
The output signal has an amplitude of 2.4 V_{PP} above and below the signal ground voltage (SG) when the digital signal of +3 dBmO is input to PCMIN and can drive a load of 20 kΩ or more. For driving a load of 20 kΩ or less, connect a resistor of 20 kΩ or more between the pins VFRO and PWI.
When adding the frequency characteristics to the receive signal, refer to the application example.
During power saving or power down mode, the output of VFRO is at the voltage level of SG.

PWI, AOUT+, AOUT–

PWI is connected to the inverting input of the receive driver. The receive driver output is connected to the AOUT– pin. Therefore, the receive level can be adjusted with the pins VFRO, PWI, and AOUT–. When the PWI pin is not used, connect the PWI pin to the AOUT– pin, and leave open the pins AOUT– and AOUT+. The output of AOUT+ is inverted with respect to the output of AOUT–. Since the signal from which provides differential drive of an impedance of 1.2 kΩ, these outputs can directly be connected to a receiver of handset using a piezoelectric earphone. Refer to the application example.



R6 > 20 kΩ
ZL ≥ 1.2 kΩ

Gain = VO/VI = 2 × R7/R6 ≤ 2

During power saving and power down modes, the outputs of AOUT+ and AOUT– are in a high impedance state.
The electrical driving capability of the AOUT– pin and AOUT+ pin is ±1.3 V maximum. The output load resistor has a minimum value of 0.6 kΩ.
If an output amplitude less than ±1.3 V is allowed, these outputs can drive a load resistance less than that described above. For more details, refer to SINGLE POWER SUPPLY PCM CODEC APPLICATION NOTE.

V_{DD}

Power supply for +5 V.

PCMIN

PCM signal input.
A serial PCM signal input to this pin is converted to an analog signal in synchronization with the RSYNC signal and BCLK signal.
The data rate of the PCM signal is equal to the frequency of the BCLK signal.
The PCM signal is shifted at a falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.
The start of the PCM data (MSD) is identified at the rising edge of RSYNC.

BCLK

Shift clock signal input for the PCMIN and PCMOUT signal.
The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, 2048, or 200 kHz. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

RSYNC

Receive synchronizing signal input.
Eight required bits are selected from serial PCM signals on the PCMIN pin by the receive synchronizing signal.
Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK. The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the receive section.
However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of 8 kHz ±2 kHz, but the electrical characteristics in this specification are not guaranteed.

XSYNC

Transmit synchronizing signal input.
The PCM output signal from the PCMOUT pin is output in synchronization with this transmit synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.
This synchronizing signal must be synchronized in phase with BCLK.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the transmit section.
However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of 8 kHz ±2 kHz, but the electrical characteristics in this specification are not guaranteed.
Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

DG

Ground for the digital signal circuits.
This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

PDN

Power down control signal.
A logic "0" level drives both transmit and receive circuits to a power down state.

PCMOUT

PCM signal output.
The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLK signal.
MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.
This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power saving or power down modes.
A pull-up resistor must be connected to this pin because its output is configured as an open drain.
This device is compatible with the ITU-T recommendation on coding law and output coding format.
The MSM7507-03 (A-law) outputs the character signal, inverting the even bits.

Input/Output Level	PCMIN/PCMOUT	
	MSD MSB	MSD MSB
+Full scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
+0	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
–0	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
–Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

	MSM7507-02 (μ-law)	MSM7507-03 (A-law)

SG

Signal ground voltage output.
The output voltage is 1/2 of the power supply voltage.
The output drive current capability is ±300 µA.
This pin provides the SG level for CODEC peripherals.
This output voltage level is undefined during power saving or power down modes.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor.
Connect a 0.1 µF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

ALAW

Control signal input of the companding law selection.
Provides only for the MSM7507-01GS-K/7507-01MS-K. The CODEC will operate in the µ-law when this pin is at a logic "0" level and the CODEC will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the µ-law if the pin is left open, since the pin is internally pulled down.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	4.75	5.0	5.25	V
Operating Temperature	Ta	—	–30	+25	+85	°C
Analog Input Voltage	V_{AIN}	Connect AIN– and GSX	—	—	2.4	V_{PP}
Input High Voltage	V_{IH}	XSYNC, RSYNC, BCLK,	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	PCMIN, PDN, ALAW	0	—	0.8	V
Clock Frequency	F_C	BCLK	64, 128, 256, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544, 200			kHz
Sync Pulse Frequency	F_S	XSYNC, RSYNC	6.0	8.0	9.0	kHz
Clock Duty Ratio	D_C	BCLK	40	50	60	%
Digital Input Rise Time	t_{Ir}	XSYNC, RSYNC, BCLK,	—	—	50	ns
Digital Input Fall Time	t_{If}	PCMIN, PDN, ALAW	—	—	50	ns
Transmit Sync Pulse Setting Time	t_{XS}	BCLK→XSYNC, See Timing Diagram	100	—	—	ns
	t_{SX}	XSYNC→BCLK, See Timing Diagram	100	—	—	ns
Receive Sync Pulse Setting Time	t_{RS}	BCLK→RSYNC, See Timing Diagram	100	—	—	ns
	t_{SR}	RSYNC→BCLK, See Timing Diagram	100	—	—	ns
Sync Pulse Width	t_{WS}	XSYNC, RSYNC	1 BCLK	—	100	µs
PCMIN Set-up Time	t_{DS}	—	100	—	—	ns
PCMIN Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Load	R_{DL}	Pull-up resistor	0.5	—	—	kΩ
	C_{DL}	—	—	—	100	pF
Analog Input Allowable DC Offset	V_{off}	Transmit gain stage, Gain = 1	–100	—	+100	mV
		Transmit gain stage, Gain = 10	–10	—	+10	mV
Allowable Jitter Width	—	XSYNC, RSYNC	—	—	500	ns

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode	—	5.0	10	mA
	I_{DD2}	Power-save mode, PDN = 1, XSYNC → OFF	—	1.5	3.0	mA
	I_{DD3}	Power-down mode, PDN = 0	—	0.01	0.05	mA
Input High Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	0.8	V
High Level Input Leakage Current	I_{IH}	—	—	—	2.0	µA
Low Level Input Leakage Current	I_{IL}	—	—	—	0.5	µA
Digital Output Low Voltage	V_{OL}	Pull-up resistance > 500 Ω	0.0	0.2	0.4	V
Digital Output Leakage Current	I_O	—	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Transmit Analog Interface Characteristics

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN+, AIN–	10	—	—	MΩ
Output Load Resistance	R_{LGX}	GSX with respect to SG	20	—	—	kΩ
Output Load Capacitance	C_{LGX}		—	—	30	pF
Output Amplitude	V_{OGX}		–1.2	—	+1.2	V
Offset Voltage	V_{OSGX}	Gain = 1	–20	—	+20	mV

Receive Analog Interface Characteristics

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INPW}	PWI	10	—	—	MΩ
Output Load Resistance	R_{LVF}	VFRO with respect to SG	20	—	—	kΩ
	R_{LAO}	AOUT+, AOUT– (each) with respect to SG	0.6	—	—	kΩ
Output Load Capacitance	C_{LVF}	VFRO	—	—	30	pF
	C_{LAO}	AOUT+, AOUT–	—	—	50	pF
Output Amplitude	V_{OVF}	VFRO, R_L = 20 kΩ with respect to SG	–1.2	—	+1.2	V
	V_{OAO}	AOUT+, AOUT–, R_L = 0.6 kΩ with respect to SG	–1.3	—	+1.3	V
Offset Voltage	V_{OSVF}	VFRO with respect to SG	–100	—	+100	mV
	V_{OSAO}	AOUT+, AOUT–, Gain = 1 with respect to SG	–100	—	+100	mV

AC Characteristics

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C, SYNC = 8 kHz)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Transmit Frequency Response	Loss T1	60	0		20	26	—	dB
	Loss T2	300			–0.15	+0.07	+0.20	dB
	Loss T3	1020			Reference			dB
	Loss T4	2020			–0.15	–0.04	+0.20	dB
	Loss T5	3000			–0.15	+0.06	+0.20	dB
	Loss T6	3400			0	0.4	0.80	dB
Receive Frequency Response	Loss R1	300	0		–0.15	–0.03	+0.20	dB
	Loss R2	1020			Reference			dB
	Loss R3	2020			–0.15	0.0	+0.20	dB
	Loss R4	3000			–0.15	+0.05	+0.20	dB
	Loss R5	3400			0.0	0.56	0.80	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3		35	43	—	dB
	SD T2		0		35	41	—	
	SD T3		–30	*1	35	38	—	
	SD T4		–40	*2	29	31.5	—	
						31		
	SD T5		–45	*2	24	27	—	
						26		
Receive Signal to Distortion Ratio	SD R1	1020	3		36	43	—	dB
	SD R2		0		36	41	—	
	SD R3		–30		36	40	—	
	SD R4		–40	*1 *2	30	33.5	—	
						32		
	SD R5		–45	*2	25	30	—	
						27		
Transmit Gain Tracking	GT T1	1020	3		–0.3	+0.01	+0.3	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.3	0	+0.3	
	GT T4		–50		–0.5	–0.03	+0.5	
	GT T5		–55		–1.2	+0.15	+1.2	
Receive Gain Tracking	GT R1	1020	3		–0.3	0	+0.3	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.3	+0.08	+0.3	
	GT R4		–50		–0.5	+0.12	+0.5	
	GT R5		–55		–0.8	+0.15	+0.8	

*1 Psophometric filter is used

*2 Upper is specified for the μ-law, lower for the A-law

AC Characteristics (Continued)

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C, SYNC = 8 kHz)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Idle Channel Noise	Nidle T	—	—	AIN = SG *1 *2	—	–74.5	–70	dBm0p
						–72.5	–69	
	Nidle R	—	—	*1 *3	—	–78	–75	
Absolute Level (Initial Difference)	AV T	1020	0	V_{DD} = 5.0 V Ta = 25°C *4	0.58	0.6007	0.622	Vrms
	AV R				0.58	0.6007	0.622	
Absolute Level (Deviation of Temperature and Power)	AV Tt			V_{DD} = +5 V ±5% Ta = –30 to 85°C *4	–0.2	—	+0.2	dB
	AV Rt				–0.2	—	+0.2	dB
Absolute Delay	Td	1020	0	A to A BCLK = 64 kHz	—	—	0.60	ms
Transmit Group Delay	tgd T1	500	0	*5	—	0.19	0.75	ms
	tgd T2	600			—	0.11	0.35	
	tgd T3	1000			—	0.02	0.125	
	tgd T4	2600			—	0.05	0.125	
	tgd T5	2800			—	0.07	0.75	
Receive Group Delay	tgd R1	500	0	*5	—	0.00	0.75	ms
	tgd R2	600			—	0.00	0.35	
	tgd R3	1000			—	0.00	0.125	
	tgd R4	2600			—	0.09	0.125	
	tgd R5	2800			—	0.12	0.75	
Crosstalk Attenuation	CR T	1020	0	TRANS → RECV	75	80	—	dB
	CR R			RECV → TRANS	70	76	—	

*1 Psophometric filter is used
*2 Upper is specified for the μ-law, lower for the A-law
*3 Input "0" code to PCMIN
*4 AVR is defined at VFRO output
*5 Minimum value of the group delay distortion

AC Characteristics (Continued)

(V_{DD} = +5 V ±5%, Ta = –30°C to +85°C, SYNC = 8 kHz)

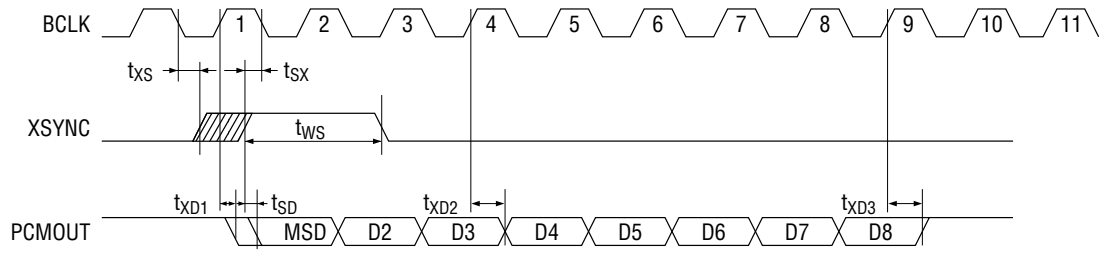
Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Discrimination	DIS	4.6 kHz to 72 kHz	0	0 to 4000 Hz	30	32	—	dB
Out-of-band Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz	—	–37.5	–35	dBm0
Intermodulation Distortion	IMD	fa = 470 fb = 320	–4	2fa – fb	—	–52	–35	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	50 mV_{PP}	*6	—	30	—	dB
	PSR R							
Digital Output Delay Time	t_{SD}	C_L = 100 pF + 1 LSTTL			20	—	200	ns
	t_{XD1}				20	—	200	
	t_{XD2}				20	—	200	
	t_{XD3}				20	—	200	

*6 The measurement under idle channel noise

TIMING DIAGRAM

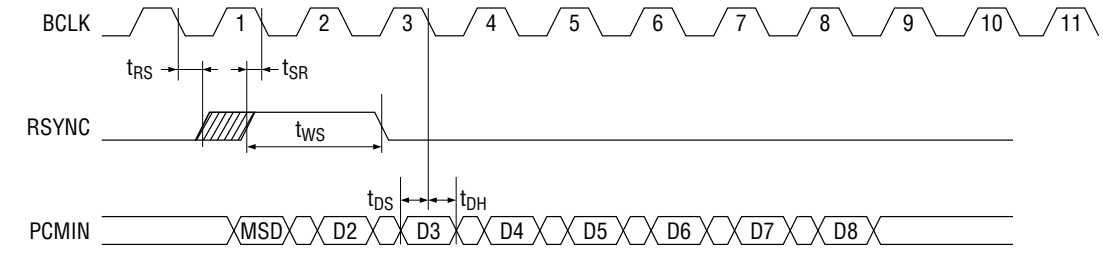
PCM Data Input/Output Timing

Transmit Timing

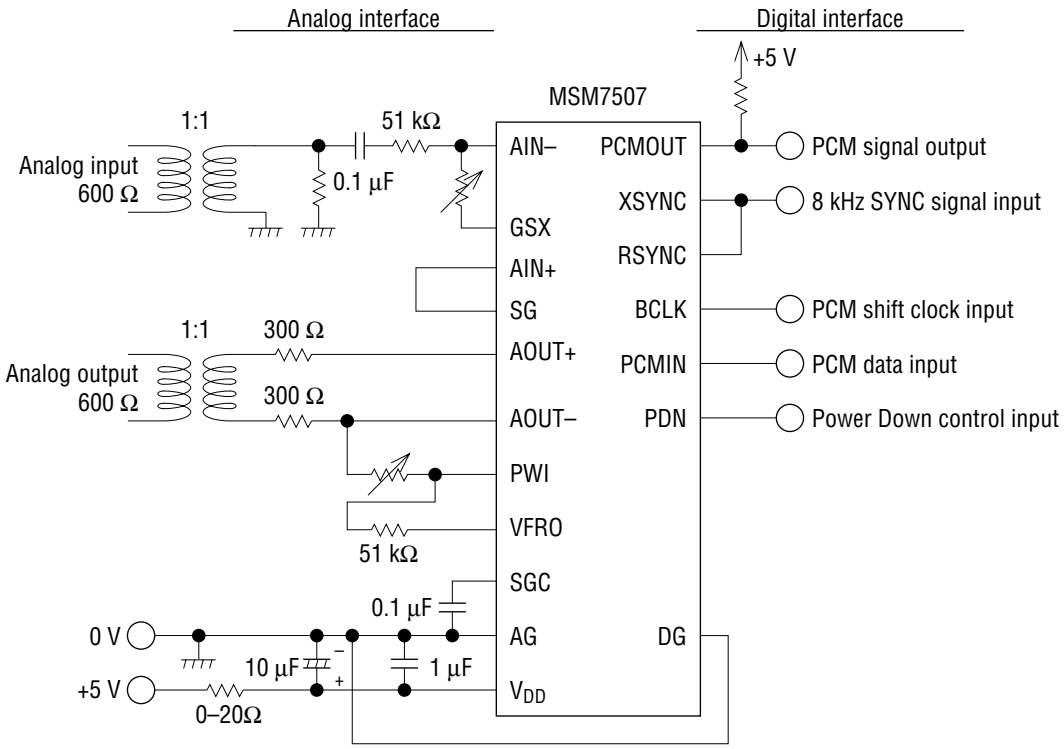


When $t_{XS} \leq 1/2 \bullet Fc$, the Delay of the MSD bit is defined as t_{XD1}.
When $t_{SX} \leq 1/2 \bullet Fc$, the Delay of the MSD bit is defined as t_{SD}.

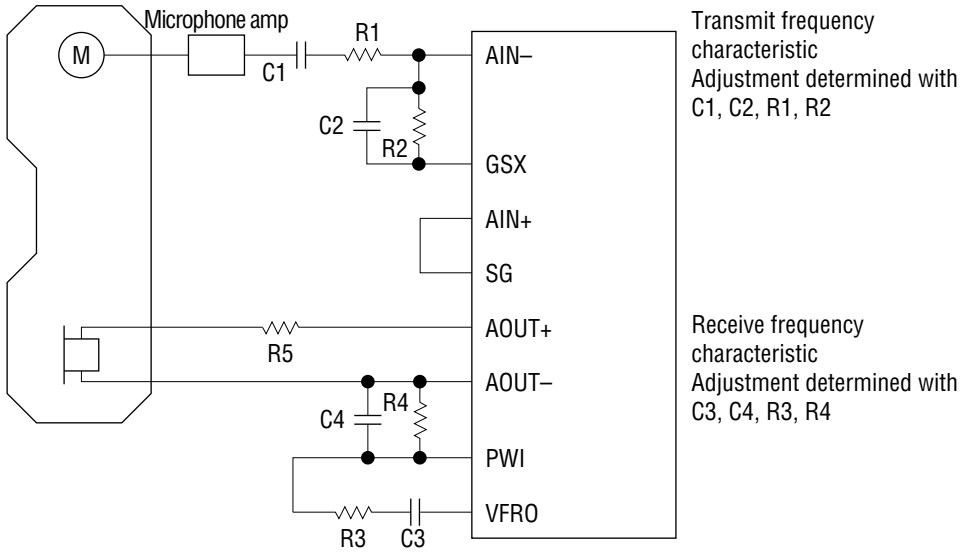
Receive Timing



APPLICATION CIRCUIT



FREQUENCY CHARACTERISTICS ADJUSTMENT CIRCUIT



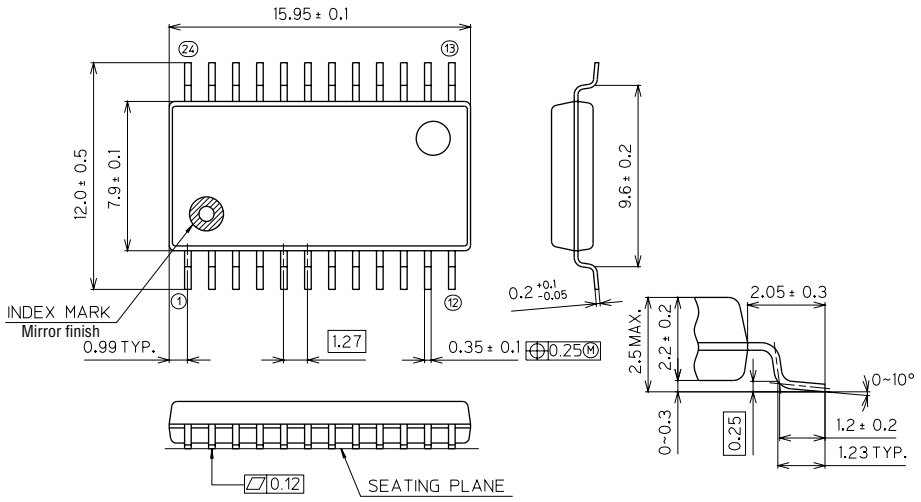
RECOMMENDATIONS FOR ACTUAL DESIGN

- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin each other as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If an IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.
- Keep the voltage on the V_{DD} pin not lower than –0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

PACKAGE DIMENSIONS

(Unit : mm)

SOP24-P-430-1.27-K



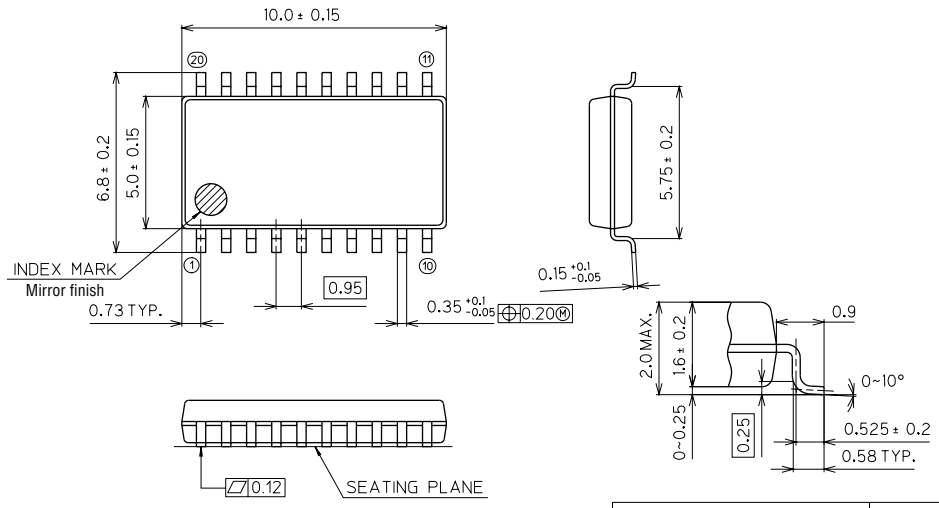
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

SSOP20-P-250-0.95-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.18 TYP.

Notes for Mounting the Surface Mount Type Package

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