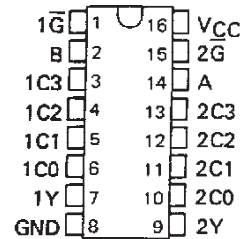


**SN54153, SN54LS153, SN54S153**  
**SN74153, SN74LS153, SN74S153**  
**DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**  
 SDLS055A – DECEMBER 1972 – REVISED MAY 2007

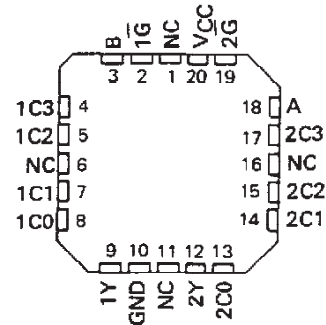
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL Circuits

SN54153, SN54LS153, SN54S153 . . . J OR W PACKAGE<sup>(1)</sup>  
 SN74153 . . . N PACKAGE  
 SN74LS153, SN74S153 . . . D OR N PACKAGE  
 (TOP VIEW)



TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES			TYPICAL POWER DISSIPATION
	FROM DATA	FROM STROBE	FROM SELECT	
'153	14 ns	17 ns	22 ns	180 mW
LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

SN54LS153, SN54S153 . . . FK PACKAGE<sup>(1)</sup>  
 (TOP VIEW)



NC - No internal connection

**description**

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.  
 H = high level, L = low level, X = irrelevant

<sup>(1)</sup> SN54S153, SN74153, and SN74S153 are obsolete.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, VCC (See Note 1)	7 V
Input voltage: '153, 'S153	5.5 V
LS153	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

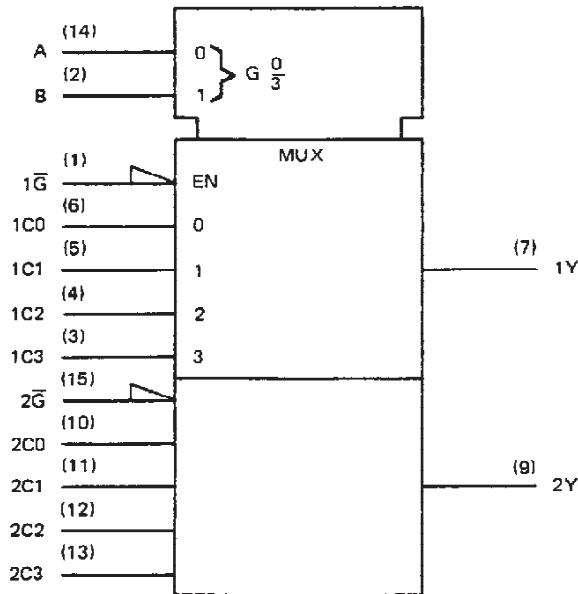
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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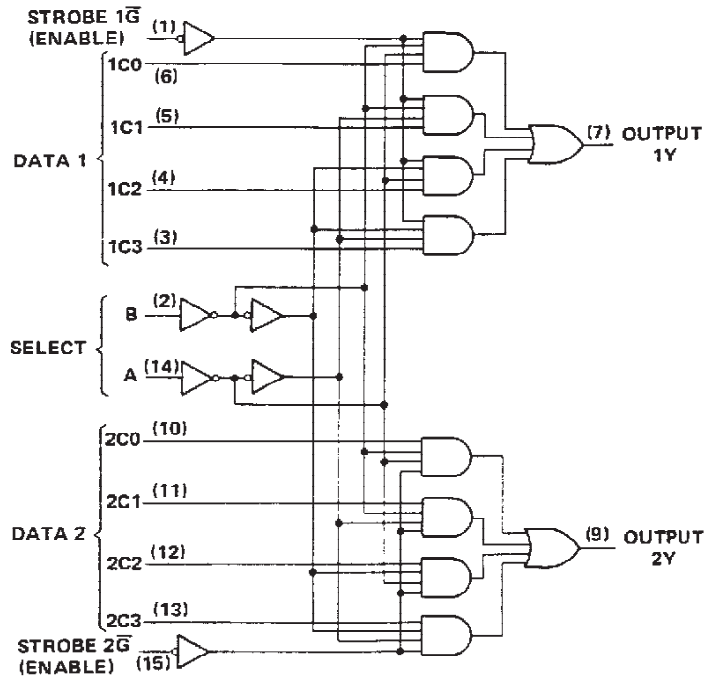
**SN54153, SN54LS153, SN54S153  
SN74153, SN74LS153, SN74S153  
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



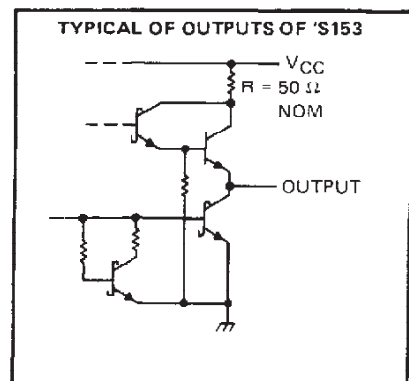
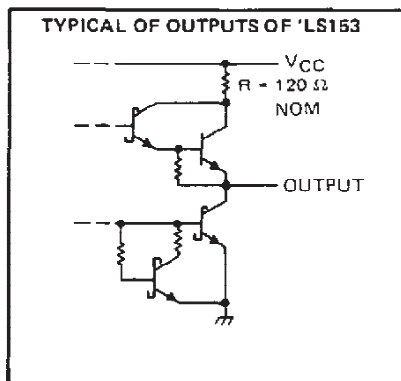
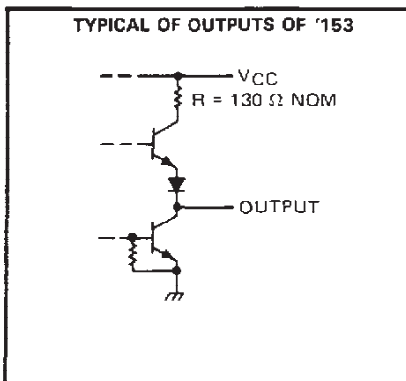
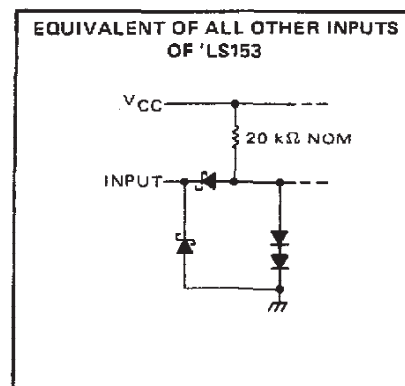
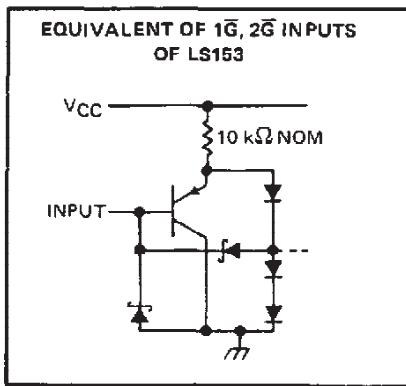
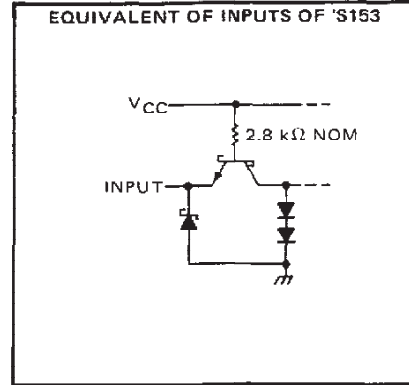
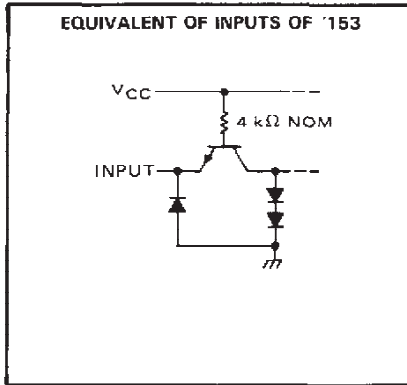
Pin numbers shown are for D, J, N, and W packages.

**TEXAS  
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**SN54153, SN54LS153, SN54S153  
SN74153, SN74LS153, SN74S153  
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

schematics of inputs and outputs



# SN54153, SN74153

## DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

### recommended operating conditions

	SN54153			SN74153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54153			SN74153			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.8			0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	$\mu$ A
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$	-20		-55	-18		-57	mA
$I_{CCL}$ Supply current, output low	$V_{CC} = \text{MAX}, \text{ See Note 2}$		36	52		36	60	mA

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

NOTE 2:  $I_{CCL}$  is measured with the outputs open and all inputs grounded.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER <sup>†</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Data	Y	$C_L = 30 \text{ pF}, R_L = 400 \Omega,$ See Note 3		12	18	ns
$t_{PHL}$	Data	Y			15	23	ns
$t_{PLH}$	Select	Y			22	34	ns
$t_{PHL}$	Select	Y			22	34	ns
$t_{PLH}$	Strobe $\bar{G}$	Y			19	30	ns
$t_{PHL}$	Strobe $\bar{G}$	Y			15	23	ns

<sup>†</sup> $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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# SN54LS153, SN74LS153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

## recommended operating conditions

	SN54LS153			SN74LS153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage	0.7			0.8			V
I <sub>OH</sub> High-level output current	-0.4			-0.4			mA
I <sub>OL</sub> Low-level output current	4			8			mA
T <sub>A</sub> Operating free-air temperature	-55			125			°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS153		SN74LS153		UNIT
		MIN	TYP ‡	MAX	MIN	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5		-1.5		V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX I <sub>OH</sub> = -0.4 mA	2.5	3.4	2.7	3.4	V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4	V
		I <sub>OL</sub> = 8 mA		0.35	0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V	0.1		0.1		mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	20		20		µA
I <sub>IL</sub>	1G, 2G	-0.2		-0.2		mA
	All other	-0.4		-0.4		
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-20	-100	-20	-100	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, See Note 2	6.2	10	6.2	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: I<sub>CCL</sub> is measured with the outputs open and all inputs grounded.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER †	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Data	Y	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Note 3	10	15	ns	
t <sub>PHL</sub>	Data	Y		17	26	ns	
t <sub>PLH</sub>	Select	Y		19	29	ns	
t <sub>PHL</sub>	Select	Y		25	38	ns	
t <sub>PLH</sub>	Strobe $\bar{G}$	Y		16	24	ns	
t <sub>PHL</sub>	Strobe $\bar{G}$	Y		21	32	ns	

† t<sub>PLH</sub> = propagation delay time, low-to-high-level output

t<sub>PHL</sub> = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

  
**TEXAS  
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# SN54S153, SN74S153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

## recommended operating conditions

	SN54S153			SN74S153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-1	mA
Low-level output current, $I_{OL}$			20			20	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$ High-level input voltage		2			V
$V_{IL}$ Low-level input voltage				0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -1 \text{ mA}$		2.5	3.4	V
	Series 54S		2.7	3.4	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 20 \text{ mA}$			0.5	V
	Series 74S			0.5	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.7 \text{ V}$			50	µA
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.5 \text{ V}$			-2	mA
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
$I_{CCL}$ Supply current, low-level output	$V_{CC} = \text{MAX}$ , See Note 2		45	70	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2:  $I_{CCL}$  is measured with the outputs open and all inputs grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Data	Y	$C_L = 15 \text{ pF}$ , $R_L = 280 \Omega$ , See Note 3		6	9	ns
$t_{PHL}$	Data	Y			6	9	ns
$t_{PLH}$	Select	Y			11.5	18	ns
$t_{PHL}$	Select	Y			12	18	ns
$t_{PLH}$	Strobe $\overline{G}$	Y			10	15	ns
$t_{PHL}$	Strobe $\overline{G}$	Y			9	13.5	ns

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
76011012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76011012A SNJ54LS 153FK	<a href="#">Samples</a>
7601101EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601101EA SNJ54LS153J	<a href="#">Samples</a>
7601101FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601101FA SNJ54LS153W	<a href="#">Samples</a>
JM38510/07902BEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
JM38510/07902BFA	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	-55 to 125		
JM38510/30902B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30902B2A	<a href="#">Samples</a>
JM38510/30902BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30902BEA	<a href="#">Samples</a>
M38510/30902B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30902B2A	<a href="#">Samples</a>
M38510/30902BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30902BEA	<a href="#">Samples</a>
SN54153J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54153J	<a href="#">Samples</a>
SN54LS153J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS153J	<a href="#">Samples</a>
SN54S153J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN74153N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS153D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS153	<a href="#">Samples</a>
SN74LS153DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS153	<a href="#">Samples</a>
SN74LS153DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS153	<a href="#">Samples</a>
SN74LS153DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS153	<a href="#">Samples</a>
SN74LS153DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS153	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS153DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS153	<a href="#">Samples</a>
SN74LS153J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	0 to 70		
SN74LS153N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS153N	<a href="#">Samples</a>
SN74LS153N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS153NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS153N	<a href="#">Samples</a>
SN74LS153NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS153	<a href="#">Samples</a>
SN74LS153NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS153	<a href="#">Samples</a>
SN74LS153NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS153	<a href="#">Samples</a>
SN74S153D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74S153N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S153N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SNJ54153J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54153J	<a href="#">Samples</a>
SNJ54153W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54153W	<a href="#">Samples</a>
SNJ54LS153FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76011012A SNJ54LS 153FK	<a href="#">Samples</a>
SNJ54LS153J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601101EA SNJ54LS153J	<a href="#">Samples</a>
SNJ54LS153W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7601101FA SNJ54LS153W	<a href="#">Samples</a>
SNJ54S153FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
SNJ54S153J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SNJ54S153W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.



**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54153, SN54LS153, SN54S153, SN74153, SN74LS153, SN74S153 :**

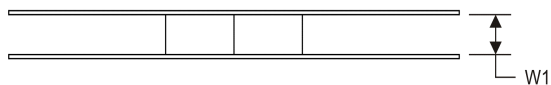
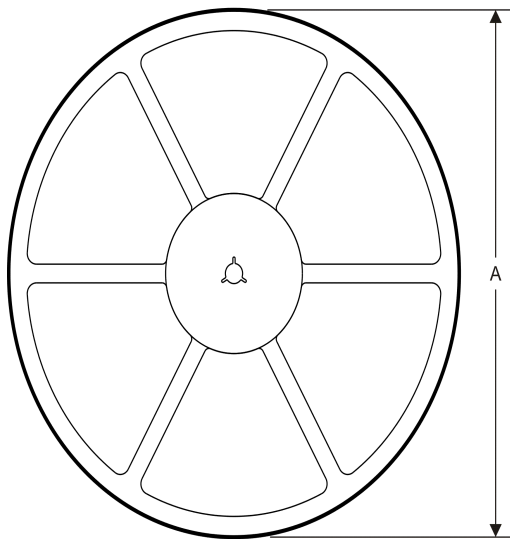
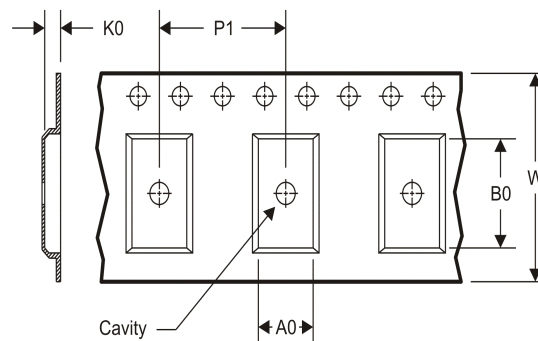
● Catalog: [SN74153](#), [SN74LS153](#), [SN74S153](#)

● Military: [SN54153](#), [SN54LS153](#), [SN54S153](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS153DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS153NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS153DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS153NSR	SO	NS	16	2000	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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