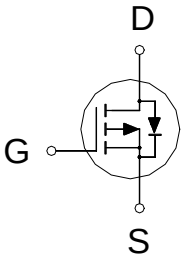
杰力科技股份有限公司
Excelliance MOS Corporation

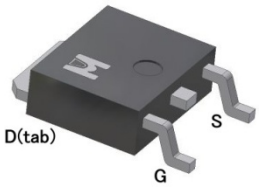
EMBB0P10A

P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-100V
$R_{DSON\ (MAX.)}$	205mΩ
I_D	-10A





UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

GP
GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	-10	A
	T_C = 100 °C		-7	
Pulsed Drain Current[1]		I_{DM}	-40	
Avalanche Current		I_{AS}	-12	
Avalanche Energy	L = 0.1mH, ID=-12A, RG=25Ω	E_{AS}	7.2	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	3.6	
Power Dissipation	T_C = 25 °C	P_D	29	W
	T_C = 100 °C		12	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		4.3	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-2.0	-3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80V, V_{GS} = 0V			-1	μA
		V_{DS} = -70V, V_{GS} = 0V, T_J = 125 °C			-25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-10			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -10A		182	205	mΩ
		V_{GS} = -7V, I_D = -5A		190	225	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -10A		7		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -25V, f = 1MHz		2018		pF
Output Capacitance	C_{oss}			82		
Reverse Transfer Capacitance	C_{rss}			61		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		4.5		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = -80V, V_{GS} = -10V, I_D = -10A		31		nC
Gate-Source Charge[1,2]	Q_{gs}			6.3		
Gate-Drain Charge[1,2]	Q_{gd}			4.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -10V, R_{GS} = 6Ω		12		nS
Rise Time[1,2]	t_r			55		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			40		
Fall Time[1,2]	t_f			40		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-10	A
Pulsed Current[3]	I_{SM}				-40	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = -5A, dI_F/dt = 100A / μS		70		nS
Reverse Recovery Charge	Q_{rr}			420		nC

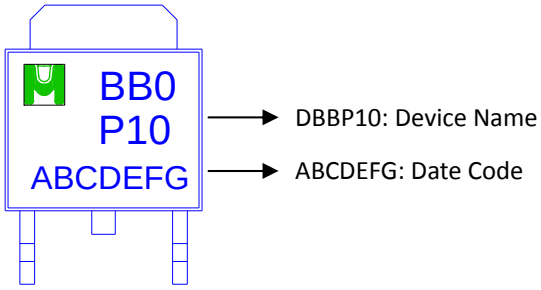
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

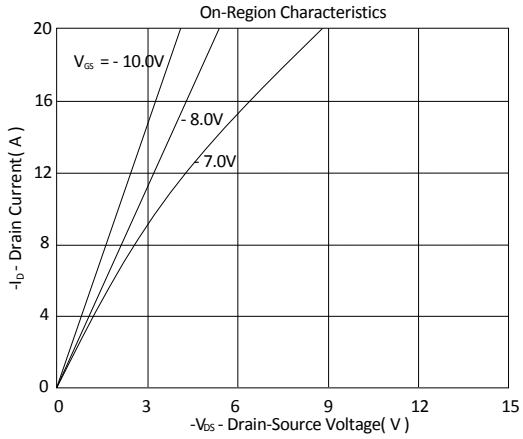
[3]Pulse width limited by maximum junction temperature.

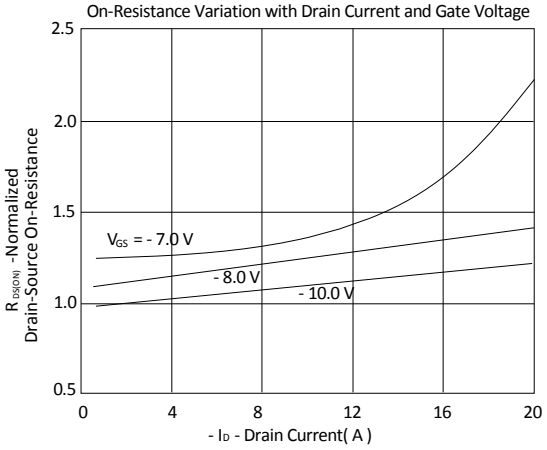
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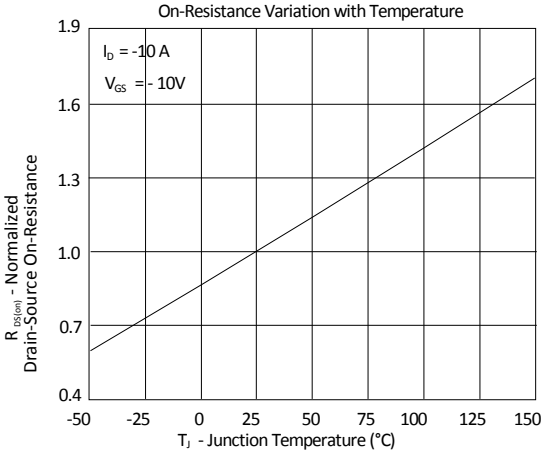
Device Name: EMBB0P10A for DPAK (TO-252)

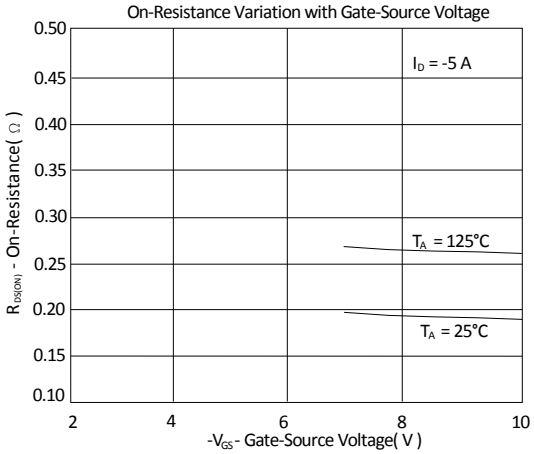


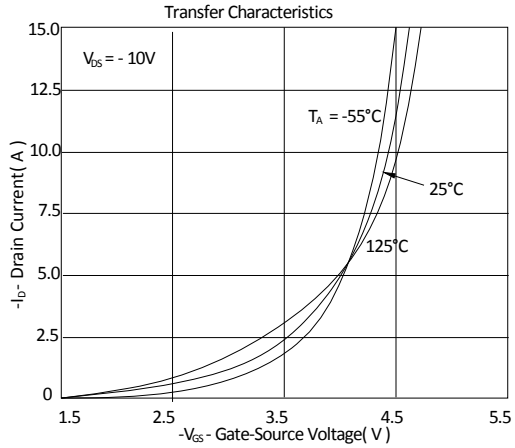
TYPICAL CHARACTERISTICS

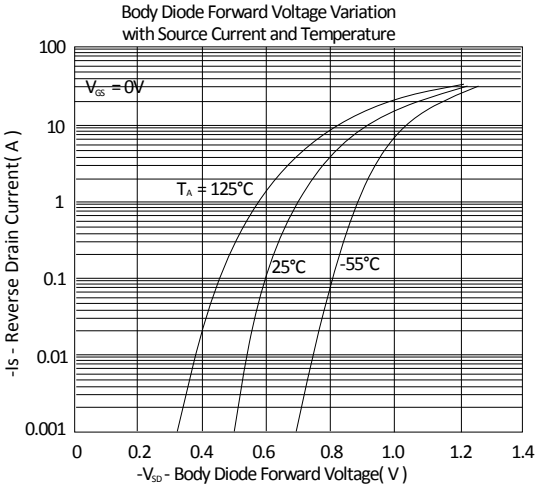




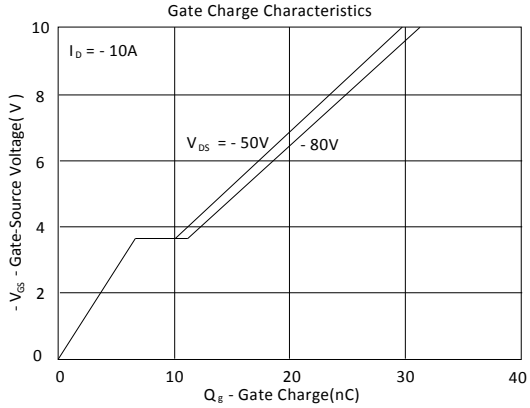




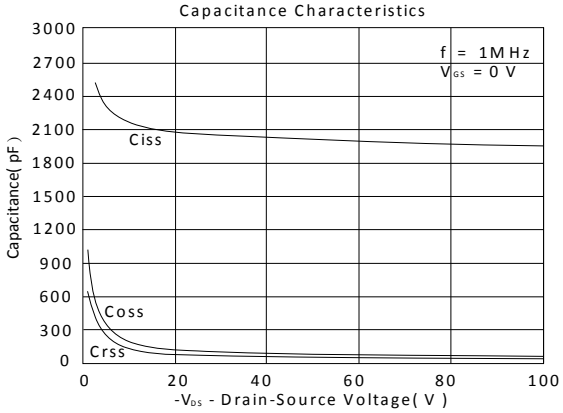




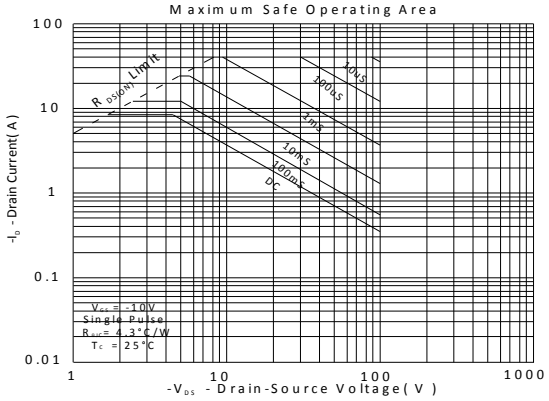
Gate Charge Characteristics



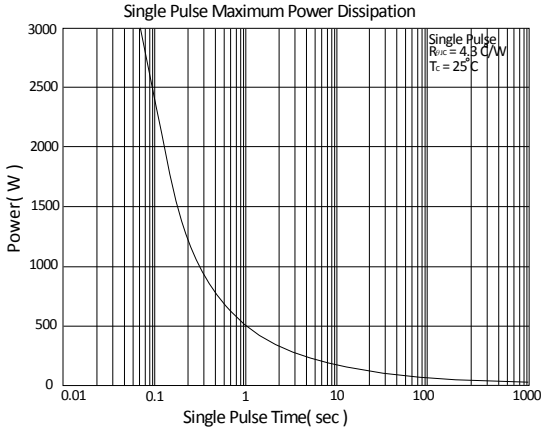
Capacitance Characteristics



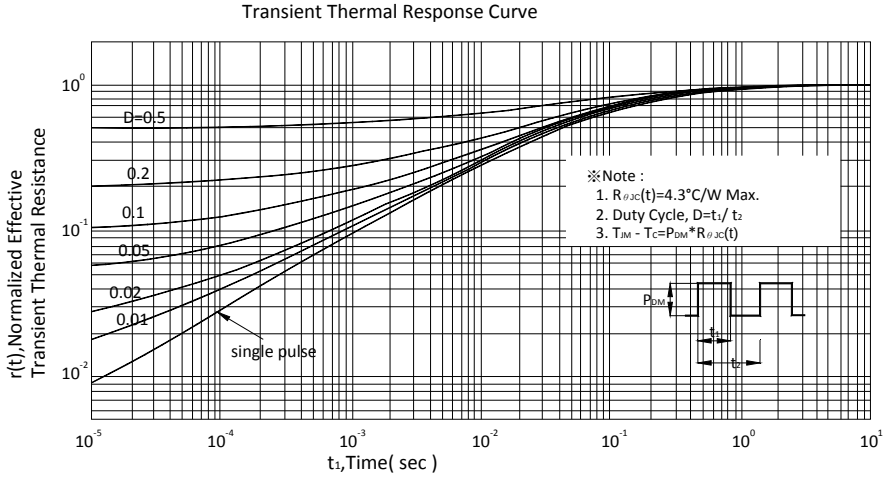
Maximum Safe Operating Area



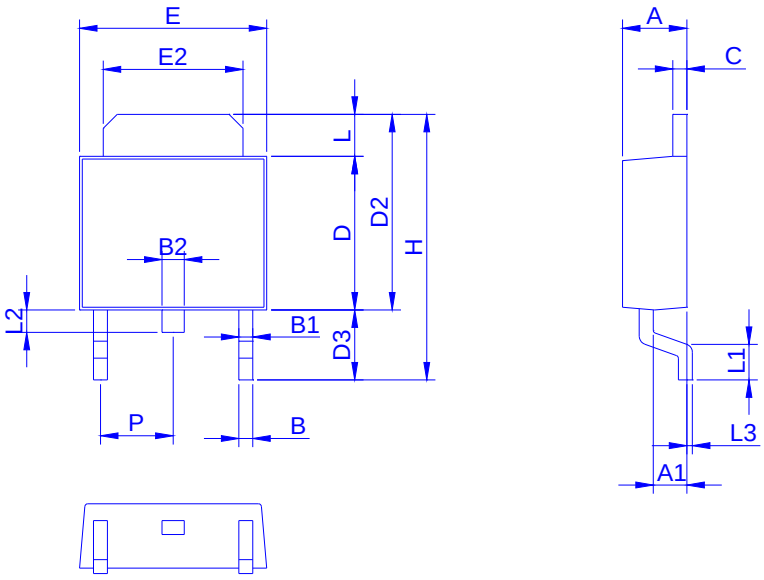
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

