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MITSUBISHI LSI's

MH16M40AJD -6
Proto-2

FAST PAGE MODE (16,777,216-WORD BY 40-BIT) DYNAMIC RAM

DESCRIPTION

The MH16M40AJD is a 16M word by 40-bit dynamic RAM module and consists of 10 industry standard 16M X 4 dynamic RAMs in a TSOP package.

The ICs are mounted on both sides of two small PC boards (Ceramcom) with the flash gold plating and form a convenient 69-pin WDIP package.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH16M40AJD-6	60	15	30	15	110	2500

- Utilizes industry standard 16M X 4 DRAMs in TSOP package
- Low stand-by power dissipation
13mW (Max) CMOS Input level
- Low operating power dissipation
MH16M40AJD - 6 3242 mW (Max)
- Fast-page mode , Read-modify-write, RAS-only refresh
CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms ($A_0 - A_{12}$) (CbR only)
- Includes (0.22uF x 12) decoupling capacitors
- 5.0V $\pm$ 5% Vcc
- 3.3V Vdd by onboard mounted regulators
- TTL input converted to LVTTTL by onboard mounted level shifters.

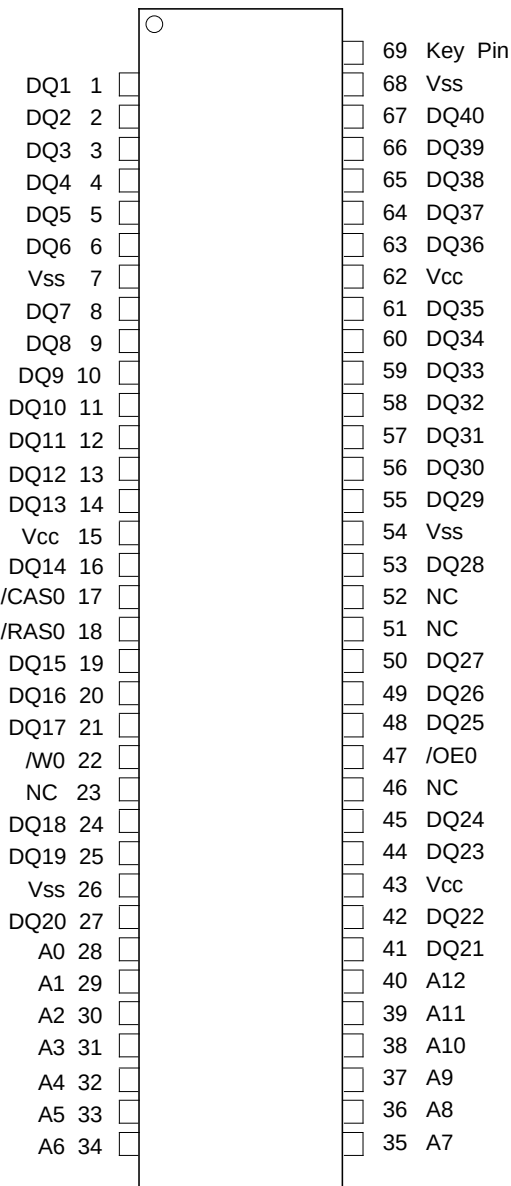
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin Name	Function
A0-A12	Address Inputs
DQ1-DQ40	Data Inputs / Outputs
RAS 0	Row Address Strobe Input
CAS 0	Column Address Strobe Input
$\overline{W}$ 0	Write Control Input
$\overline{OE}$ 0	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



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FUNCTION

The MH16M40AJD provide, in addition to normal read, write, and read-modify-write operations,

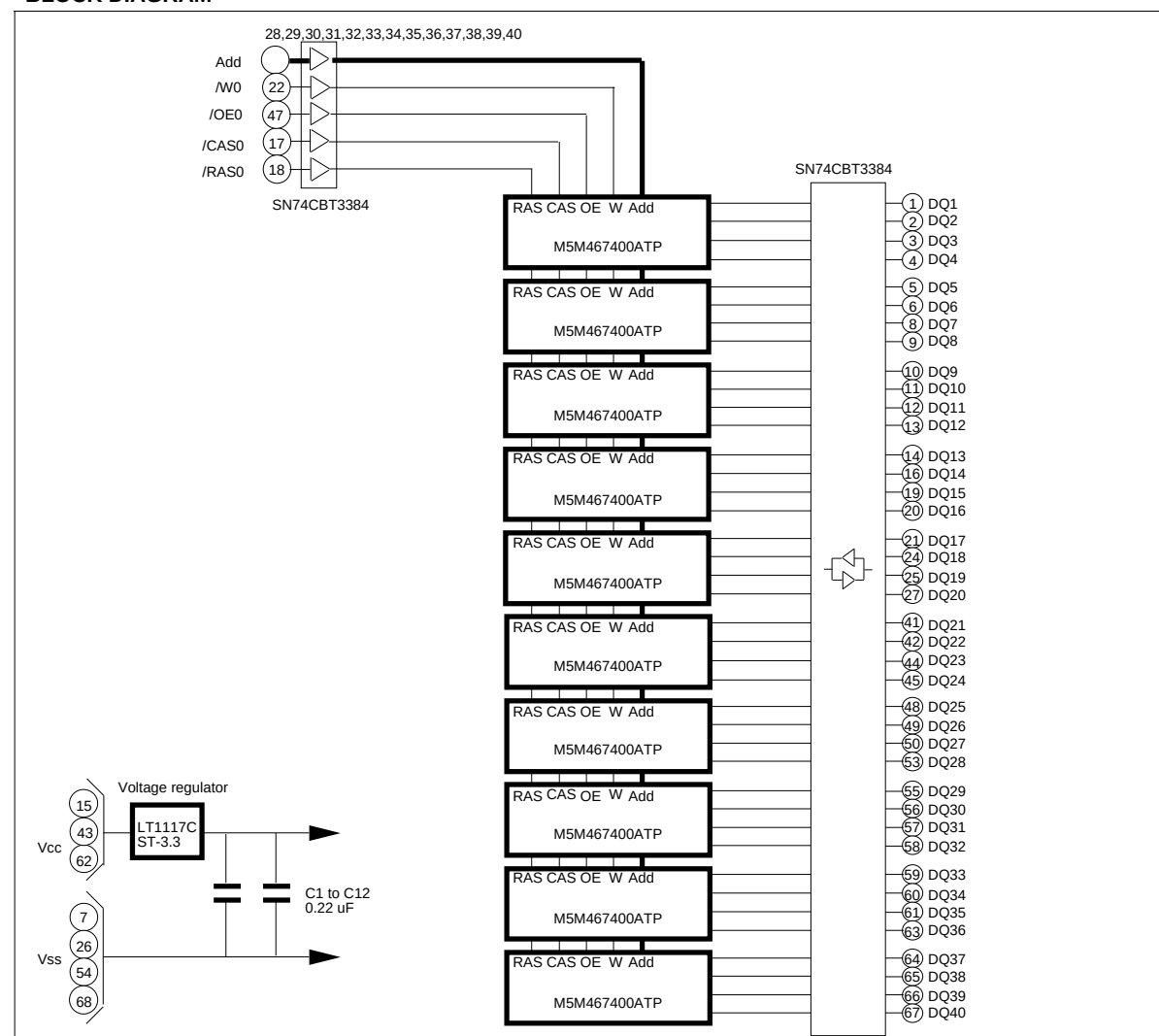
a number of other functions, e.g., fast page mode, $\overline{\text{CAS}}$ before RAS refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	RAS	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
Hidden refresh	ACT	ACT	NAC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to V _{ss}	-0.5 ~ 7	V
V _I	Input voltage		-0.5 ~ 6	V
V _O	Output voltage		-0.5 ~ 6	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25 °C	15	W
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-40 ~ 100	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{cc}	Supply voltage	4.75	5	5.25	V
V _{ss}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.0		5.5	V
V _{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{ss}

ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{cc}=5V ± 5%, V_{ss}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} =-2mA	2.4		3.6	V
V _{OL}	Low-level output voltage	I _{OL} =2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating 0V ≤ V _{OUT} ≤ 3.6V	-10		10	μA
I _I	Input current	0V ≤ V _{IN} ≤ 5.25V, Other inputs pins=0V	-5		5	μA
I _{CC1 (AV)}	Average supply current from V _{cc} operating (Note 3,4)	RAS, CAS cycling t _{rc} =t _{wc} =min. output open			900	mA
I _{CC2}	Supply current from V _{cc} , stand-by	RAS= $\overline{\text{CAS}}$ =V _{IH} , output open			10	mA
		RAS= $\overline{\text{CAS}}$ ≥ V _{cc} -0.2			5.4	
I _{CC4 (AV)}	Average supply current from V _{cc} Fast-Page-Mode (Note 3,4)	RAS=V _{IL} , CAS cycling t _{pc} =min. output open			800	mA
I _{CC6 (AV)}	Average supply current from V _{cc} CAS before RAS refresh mode (Note 3)	CAS before RAS refresh cycling t _{rc} =min. output open			1200	mA

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (T_a=0 ~ 70°C, V_{cc}=5V ± 5%, V_{ss}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I (A)}	Input capacitance, address inputs	V _I =V _{ss} f=1MHz V _i =25mV _{rms}			20	pF
C _{I (OE)}	Input capacitance, $\overline{\text{OE}}$ input				20	pF
C _{I (W)}	Input capacitance, write control input				20	pF
C _{I (RAS)}	Input capacitance, RAS input				20	pF
C _{I (CAS)}	Input capacitance, $\overline{\text{CAS}}$ input				20	pF
C _{I/O}	Input/Output capacitance, data ports				20	pF

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SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=5V ± 5%, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
t _{CAC}	Access time from $\overline{\text{CAS}}$ (Note 6,7)		15	ns
t _{RAC}	Access time from $\overline{\text{RAS}}$ (Note 6,8)		60	ns
t _{AA}	Column address access time (Note 6,9)		30	ns
t _{CPA}	Access time from $\overline{\text{CAS}}$ precharge (Note 6,10)		35	ns
t _{OE}	Access time from $\overline{\text{OE}}$ (Note 6)		15	ns
t _{CLZ}	Output low impedance time from $\overline{\text{CAS}}$ low (Note 6)	5		ns
t _{OFF}	Output disable time after $\overline{\text{CAS}}$ high (Note 11)	0	15	ns
t _{OEZ}	Output disable time after $\overline{\text{OE}}$ high (Note 11)	0	15	ns

Note 5: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 1TTL loads and 100pF. The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

7: Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.

8: Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

9: Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{ASC}}(\text{max})$.

10: Assumes that $t_{\text{CP}} \leq t_{\text{CP}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.

11: $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ defines the time at which the output achieves the high impedance state ($I_{\text{out}} \leq I \pm 10 \mu\text{A}$) and is not reference to $V_{\text{OH}}(\text{min})$ or $V_{\text{OL}}(\text{max})$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc=5V ± 5%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
tREF	Refresh cycle time		64	ms
trP	RAS high pulse width	40		ns
trCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note14)	20	45	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	10		ns
trPC	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		ns
tCPN	$\overline{\text{CAS}}$ high pulse width	10		ns
trAD	Column address delay time from $\overline{\text{RAS}}$ low (Note15)	15	30	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low	0		ns
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note16)	0	10	ns
trAH	Row address hold time after $\overline{\text{RAS}}$ low	10		ns
tCAH	Column address hold time after $\overline{\text{CAS}}$ low	15		ns
tdZC	Delay time, data to $\overline{\text{CAS}}$ low (Note17)	0		ns
tdZO	Delay time, data to $\overline{\text{OE}}$ low (Note17)	0		ns
tcDD	Delay time, $\overline{\text{CAS}}$ high to data (Note18)	15		ns
tODD	Delay time, $\overline{\text{OE}}$ high to data (Note18)	15		ns
tr	Transition time (Note19)	1	50	ns

Note 12: The timing requirements are assumed $t_{\text{r}} = 5\text{ns}$.

13: $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals.

14: $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is less than $t_{\text{RCD}}(\text{max})$, access time is t_{RAC} . If t_{RCD} is greater than $t_{\text{RCD}}(\text{max})$, access time is controlled exclusively by t_{CAC} or t_{AA} . $t_{\text{RCD}}(\text{min})$ is specified as $t_{\text{RCD}}(\text{min}) = t_{\text{RAH}}(\text{min}) + 2t_{\text{H}} + t_{\text{ASC}}(\text{min})$.

15: $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{ASC}}(\text{max})$, access time is controlled exclusively by t_{AA} .

16: $t_{\text{ASC}}(\text{max})$ is specified as a reference point only. If $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$, access time is controlled exclusively by t_{CAC} .

17: Either t_{DZC} or t_{DZO} must be satisfied.

18: Either t_{CDD} or t_{ODD} must be satisfied.

19: t_{tr} is measured between $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$.

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Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
trc	Read cycle time	110		ns
trAS	RAS iow pulse width	60	10000	ns
tcAS	CAS iow pulse width	15	10000	ns
tCSH	CAS hold time after RAS iow	60		ns
trSH	RAS hold time after CAS iow	15		ns
trCS	Read Setup time after CAS high	0		ns
trCH	Read hold time after CAS iow (Note 20)	0		ns
trRH	Read hold time after RAS iow (Note 20)	10		ns
trAL	Column address to RAS hold time	30		ns
toCH	CAS hold time after OE iow	15		ns
toRH	RAS hold time after OE iow	15		ns

Note 20: Either trCH or trRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
tWC	Write cycle time	110		ns
tRAS	RAS iow pulse width	60	10000	ns
tCAS	CAS iow pulse width	15	10000	ns
tCSH	CAS hold time after RAS iow	60		ns
tRSH	RAS hold time after CAS iow	15		ns
tWCS	Write setup time before CAS iow (Note 22)	0		ns
tWCH	Write hold time after CAS iow	10		ns
tCWL	CAS hold time after W iow	15		ns
tRWL	RAS hold time after W iow	15		ns
tWP	Write pulse width	10		ns
tDS	Data setup time before CAS iow or W iow	0		ns
tDH	Data hold time after CAS iow or W iow	10		ns
tOEH	OE hold time after W iow	15		ns

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Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
trWC	Read write/read modify write cycle time (Note21)	150		ns
trAS	RAS low pulse width	95	10000	ns
tcAS	CAS low pulse width	50	10000	ns
tCSH	CAS hold time after RAS low	95		ns
trSH	RAS hold time after CAS low	50		ns
trCS	Read setup time before CAS low	0		ns
tcWD	Delay time, CAS low to W low (Note22)	30		ns
trWD	Delay time, RAS low to W low (Note22)	75		ns
tAWD	Delay time, address to W low (Note22)	45		ns
tcWL	CAS hold time after W low	15		ns
trWL	RAS hold time after W low	15		ns
tWP	Write pulse width	10		ns
tDS	Data setup time before W low	0		ns
tDH	Data hold time after W low	10		ns
toEH	OE hold time after W low	15		ns

Note 21: trwc is specified as $\text{trwc}(\text{min}) = \text{trac}(\text{max}) + \text{todd}(\text{min}) + \text{trwl}(\text{min}) + \text{trp}(\text{min}) + 4\text{t}$.

Note 22: twcs, tcwd, trwd and tawd and tcpwd are specified as reference points only. If $\text{twcs} \geq \text{twcs}(\text{min})$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $\text{tcwd} \geq \text{tcwd}(\text{min})$, $\text{trwd} \geq \text{trwd}(\text{min})$, $\text{tawd} \geq \text{tawd}(\text{min})$ and $\text{tcpwd} \geq \text{tcpwd}(\text{min})$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
tPC	Fast page mode read/write cycle time	40		ns
tPRWC	Fast page mode read write/read modify write cycle time	75		ns
tRAS	RAS low pulse width for read write cycle (Note24)	100	102400	ns
tCP	CAS high pulse width (Note25)	10	15	ns
tCPRH	RAS hold time after CAS precharge	35		ns
tCPWD	Delay time, CAS precharge to W low (Note22)	35		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: tr $\overline{\text{AS}}$ (min) is specified as two cycles of CAS input are performed.

25: t $\overline{\text{CP}}$ (max) is specified as a reference point only. If $\text{tcp} \geq \text{tcp}(\text{max})$, access time is controlled exclusively by t $\overline{\text{CAC}}$.

CAS before RAS Refresh Cycle (Note 26)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
tCSR	CAS setup time before RAS low	10		ns
tCHR	CAS hold time after RAS low	10		ns
trSR	Read setup time before RAS low	10		ns
trHR	Read hold time after RAS low	10		ns

Note 26: Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles instead of eight $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

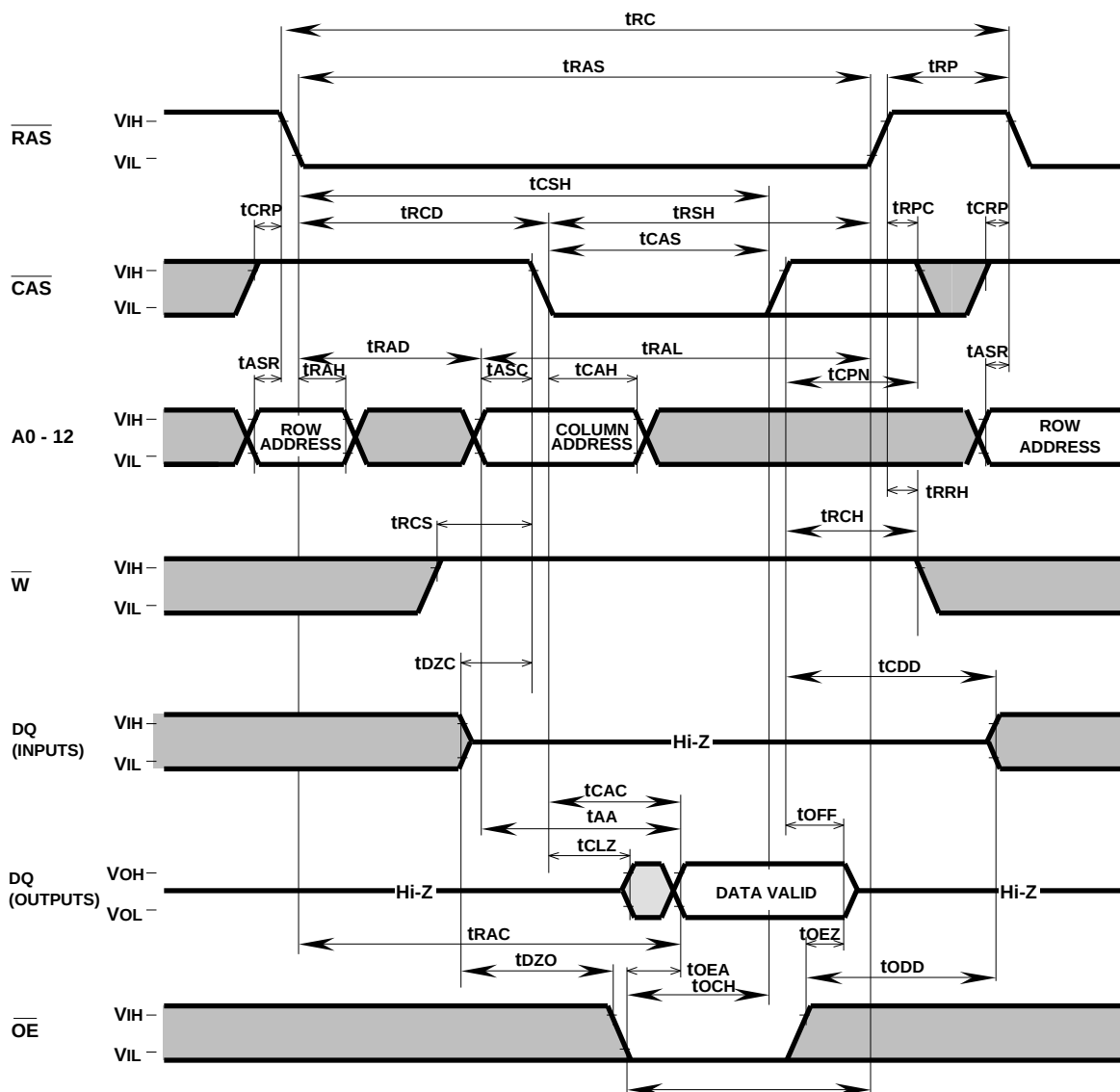
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Timing Diagrams (Note 27)

Read Cycle



Note 27



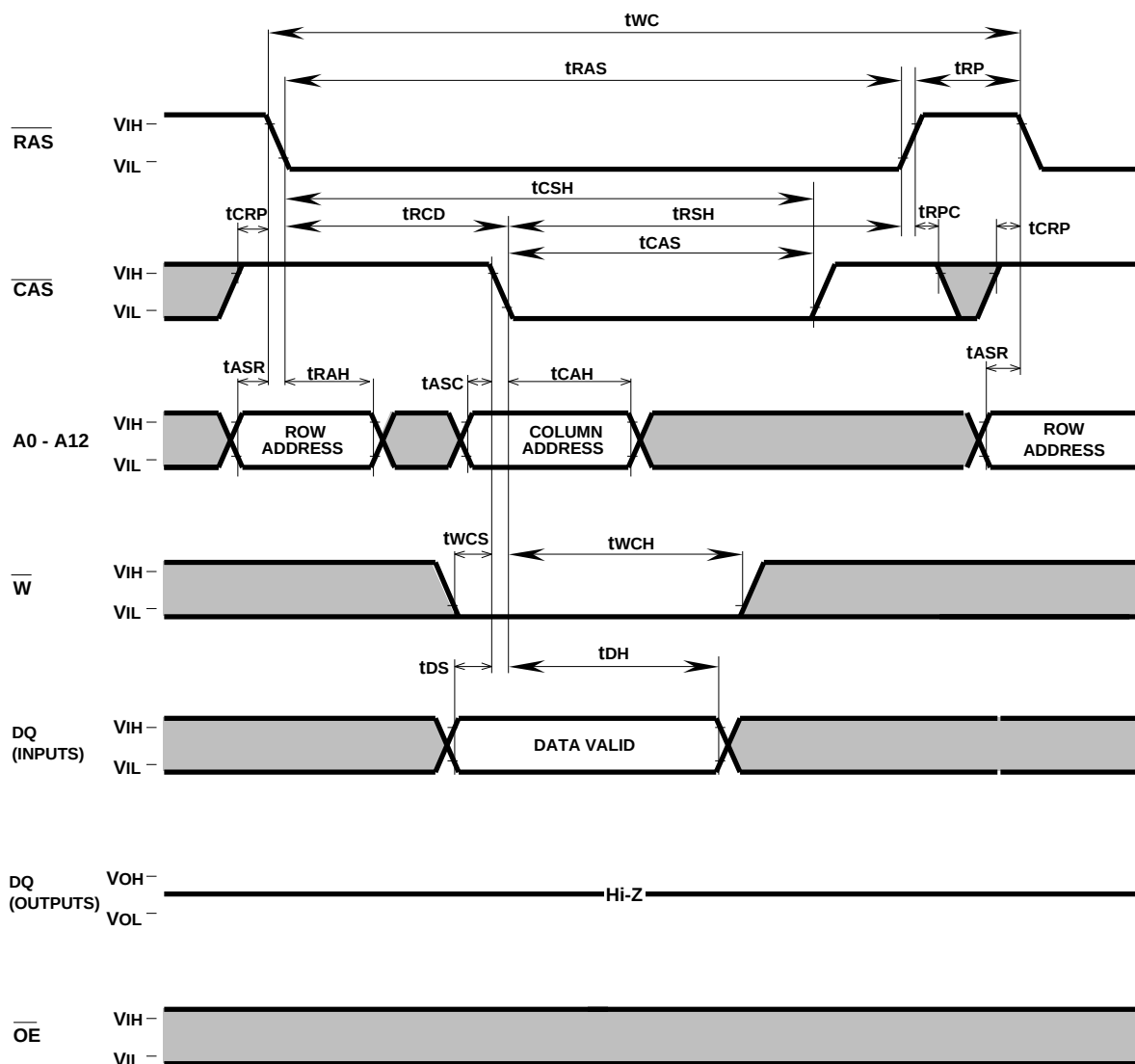
Indicates the don't care input.
 $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ or
 $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$
 Indicates the invalid output.

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Write Cycle (Early write)

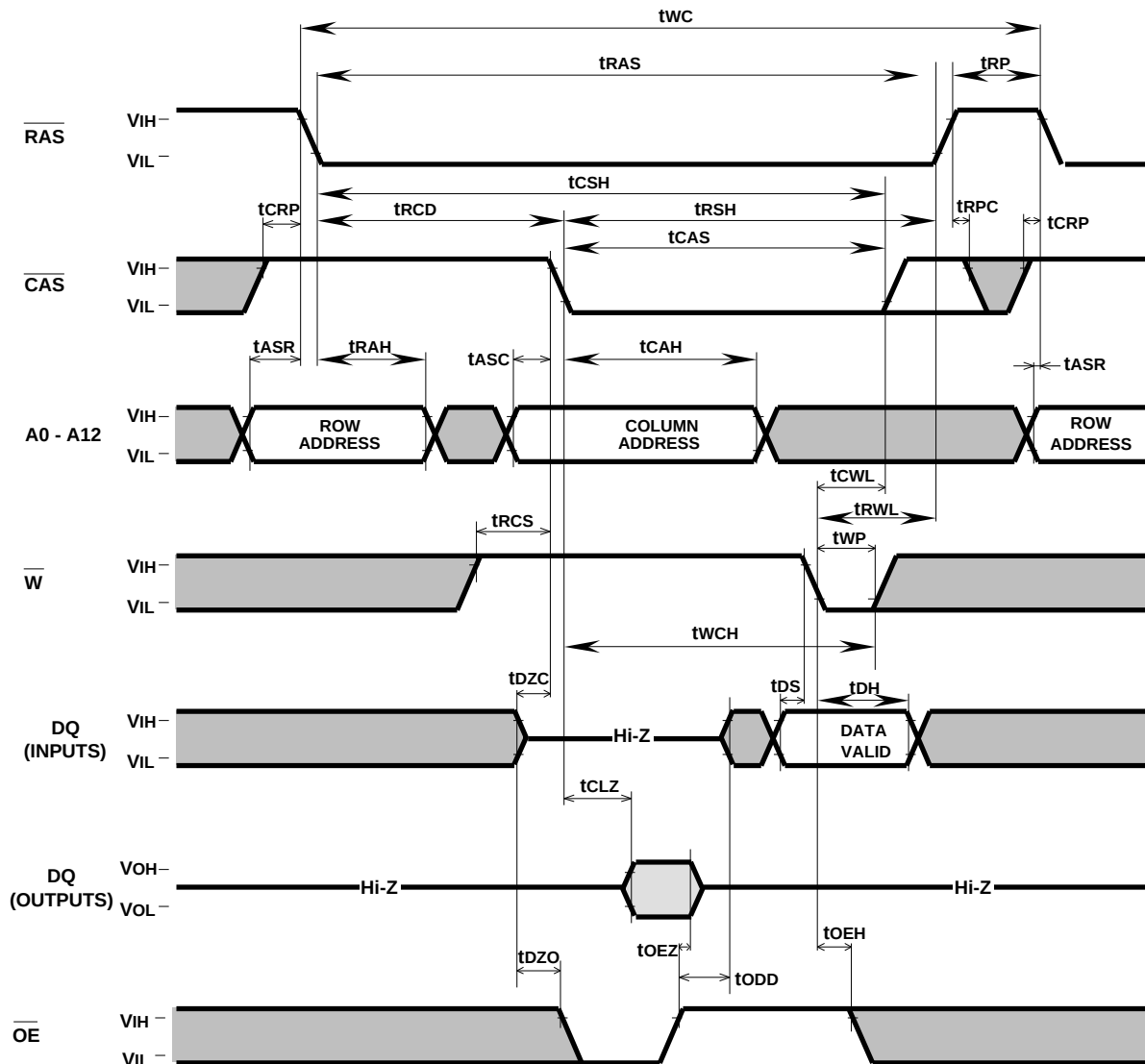


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Write Cycle (Delayed write)

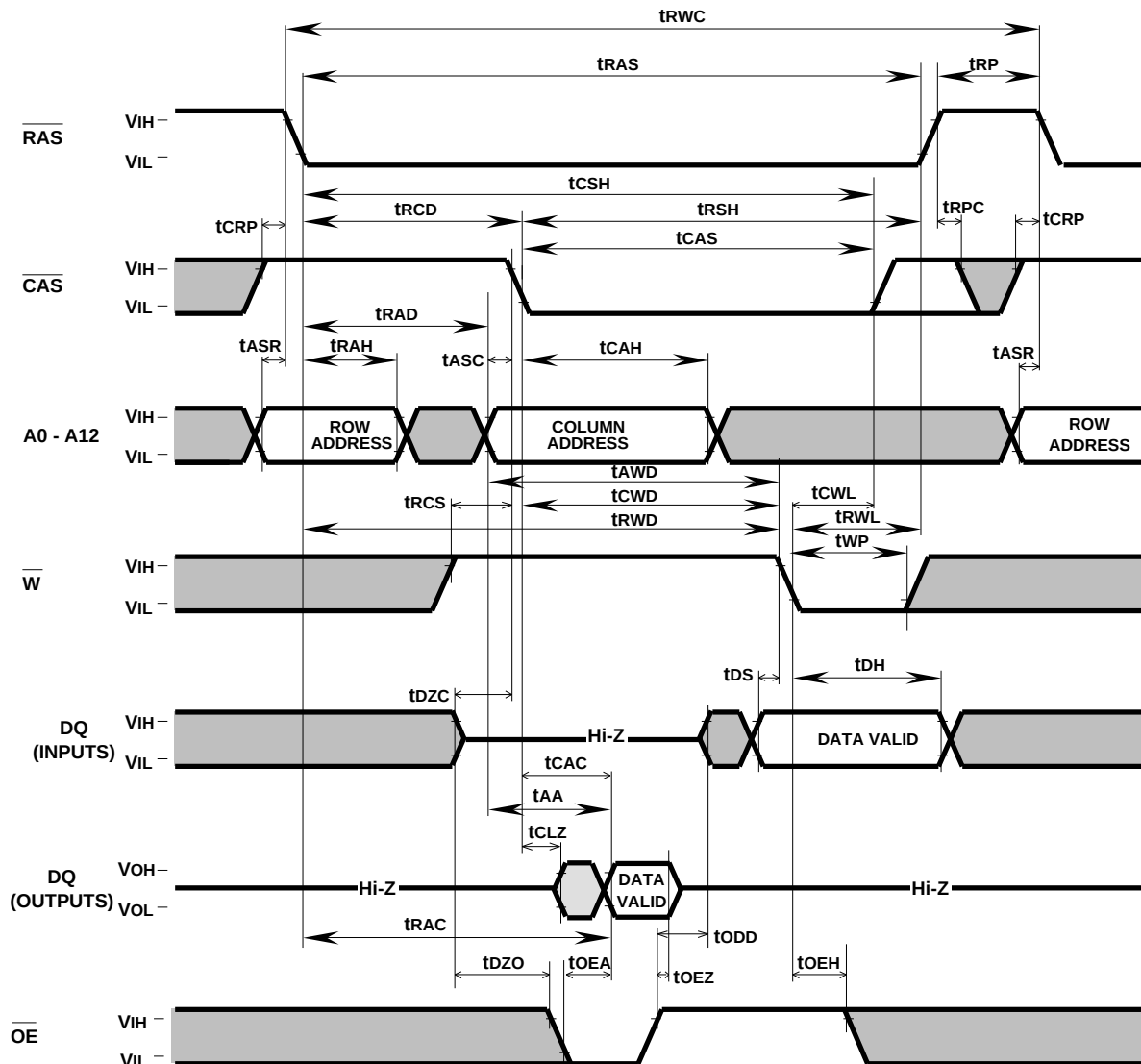


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Read-Write, Read-Modify-Write Cycle

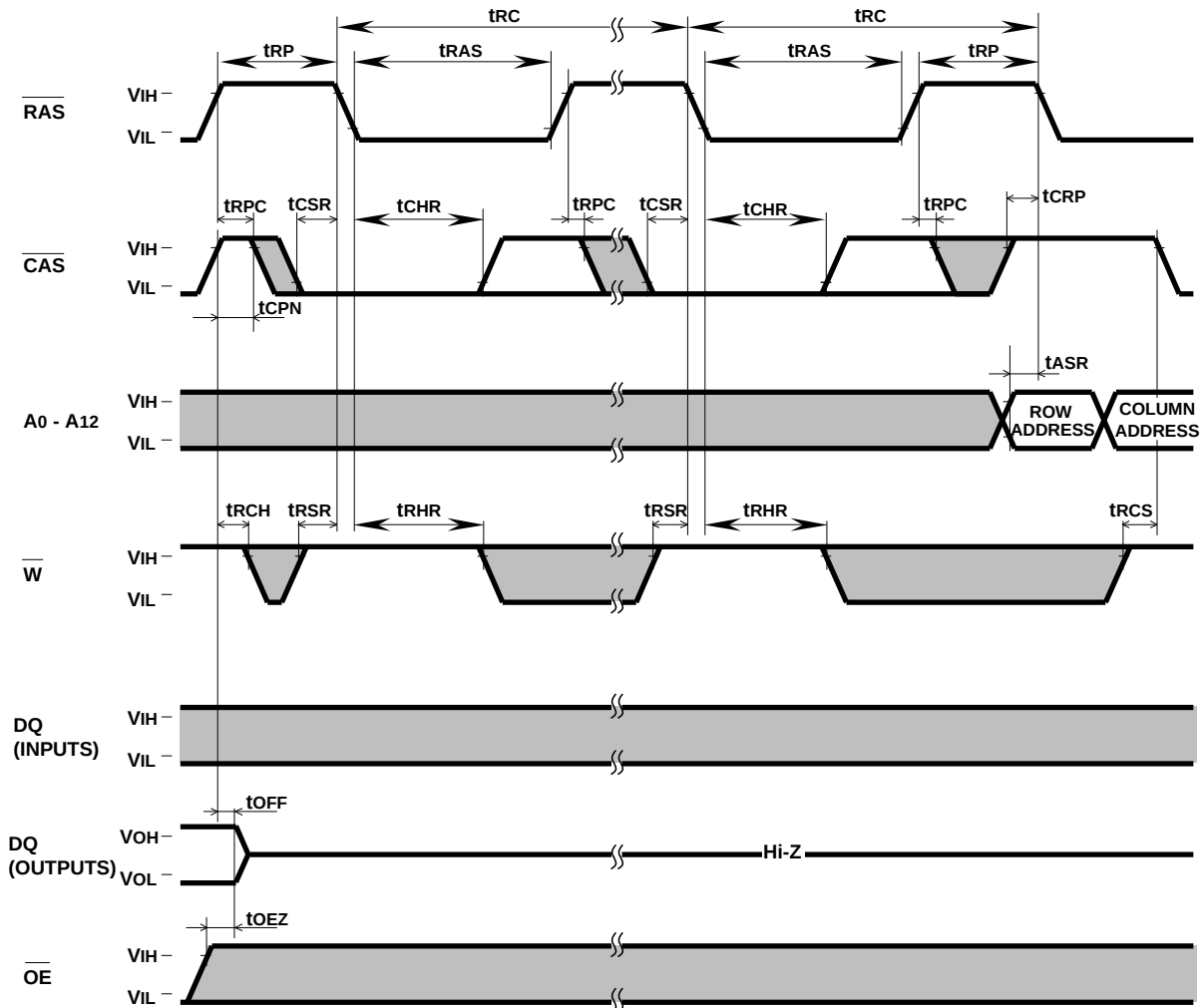


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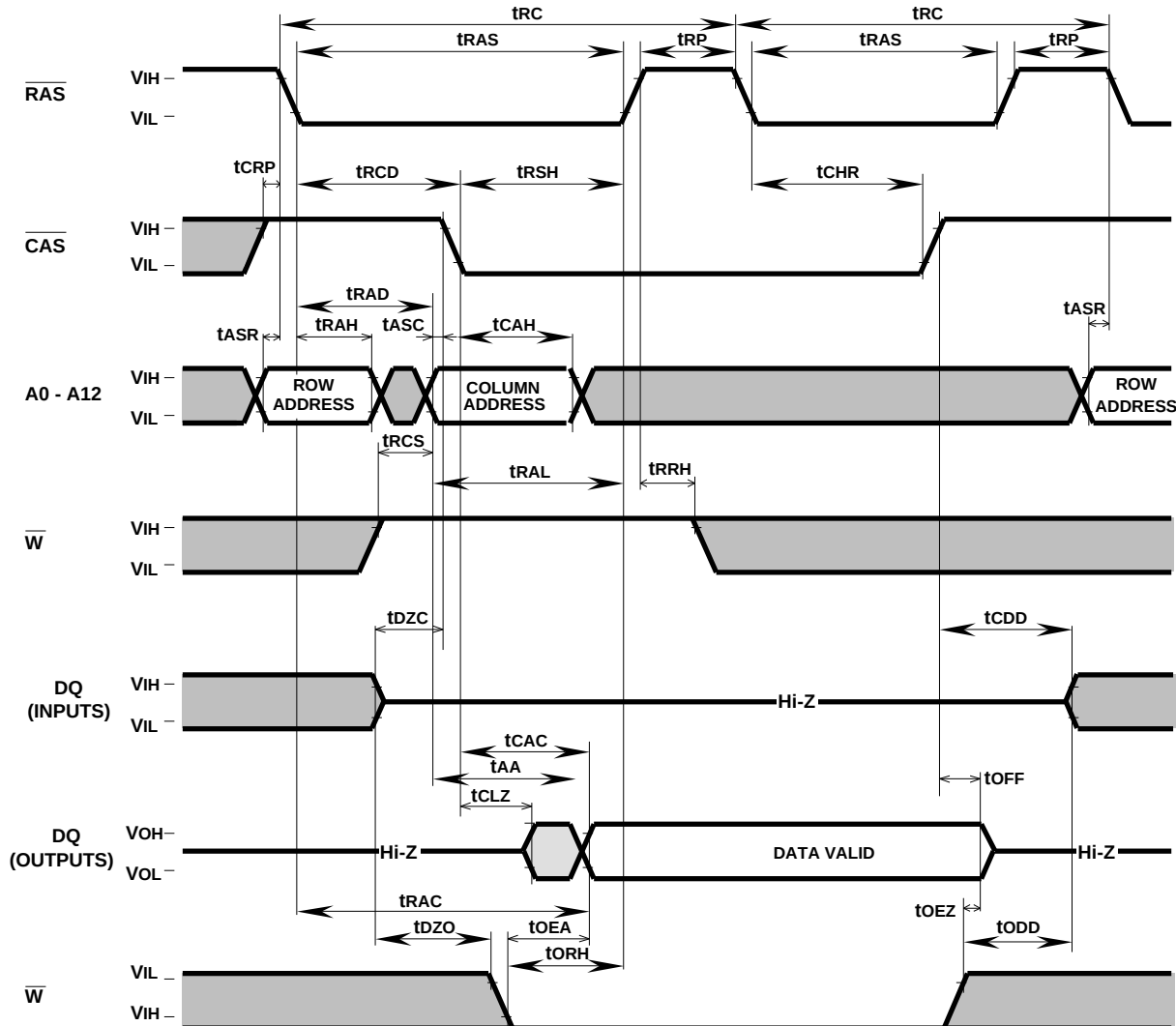
CAS before RAS Refresh Cycle



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Hidden Refresh Cycle (Read) (Note 28)



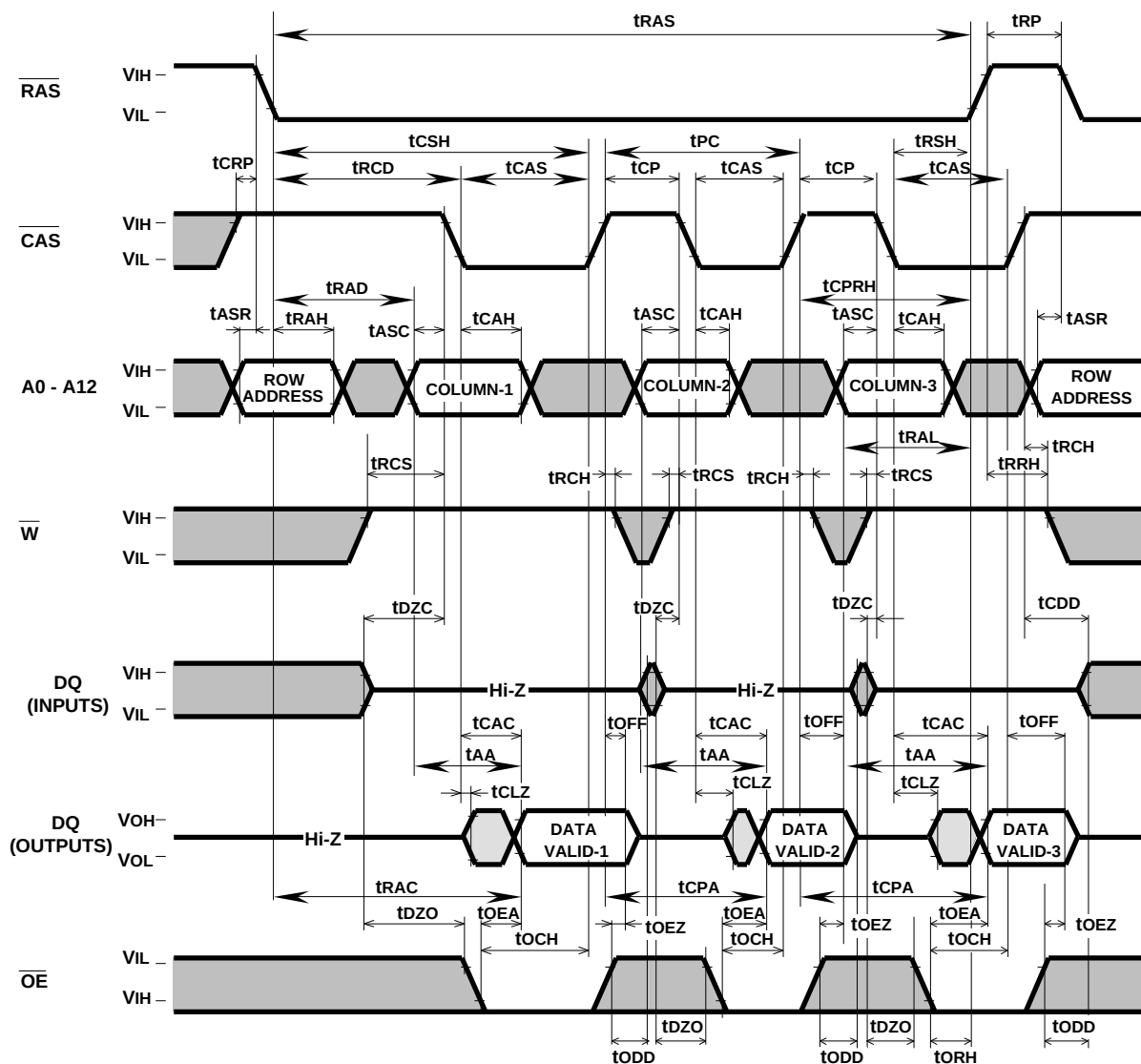
Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

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Fast Page Mode Read Cycle

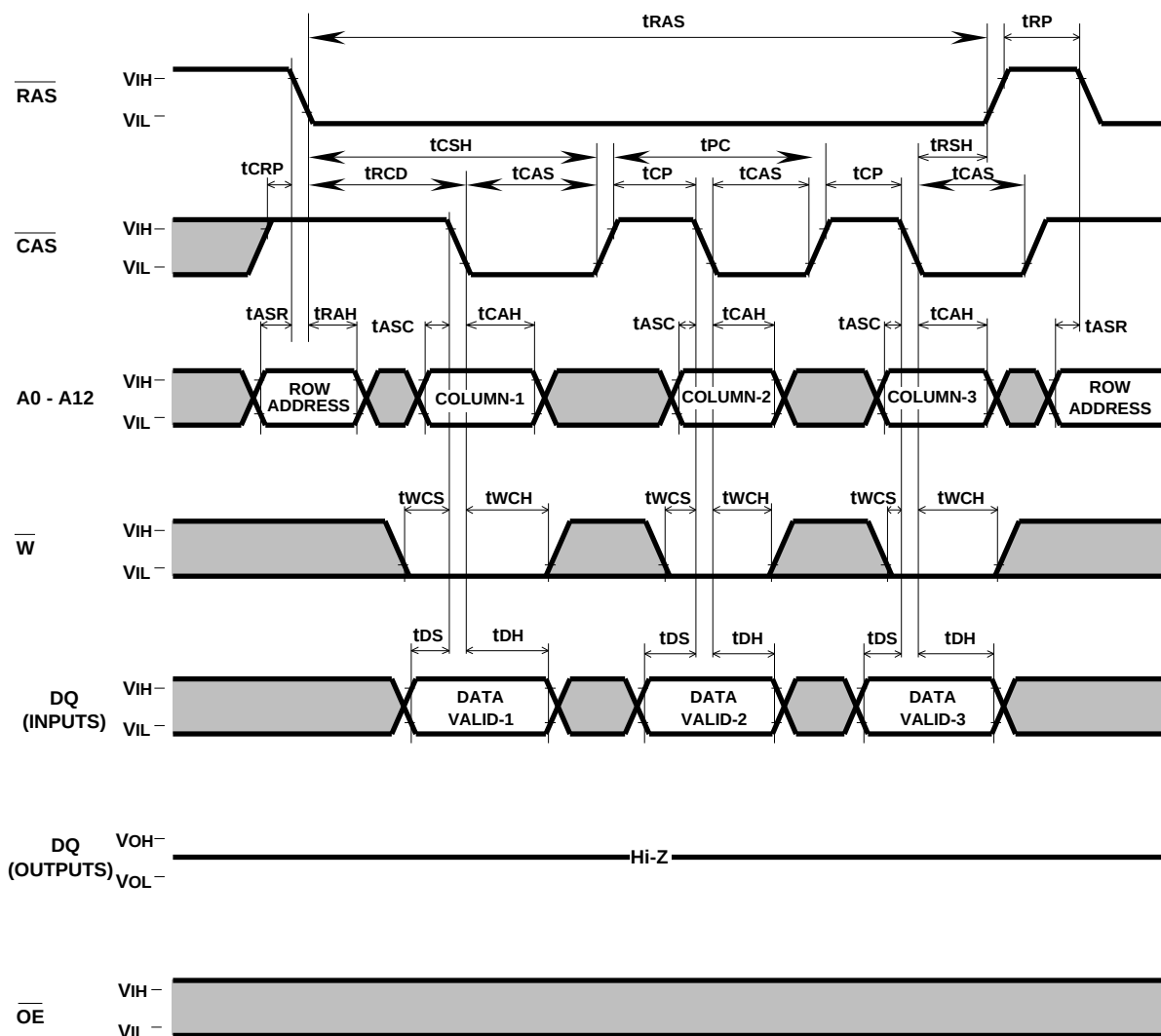


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Fast Page Mode Write Cycle (Early Write)

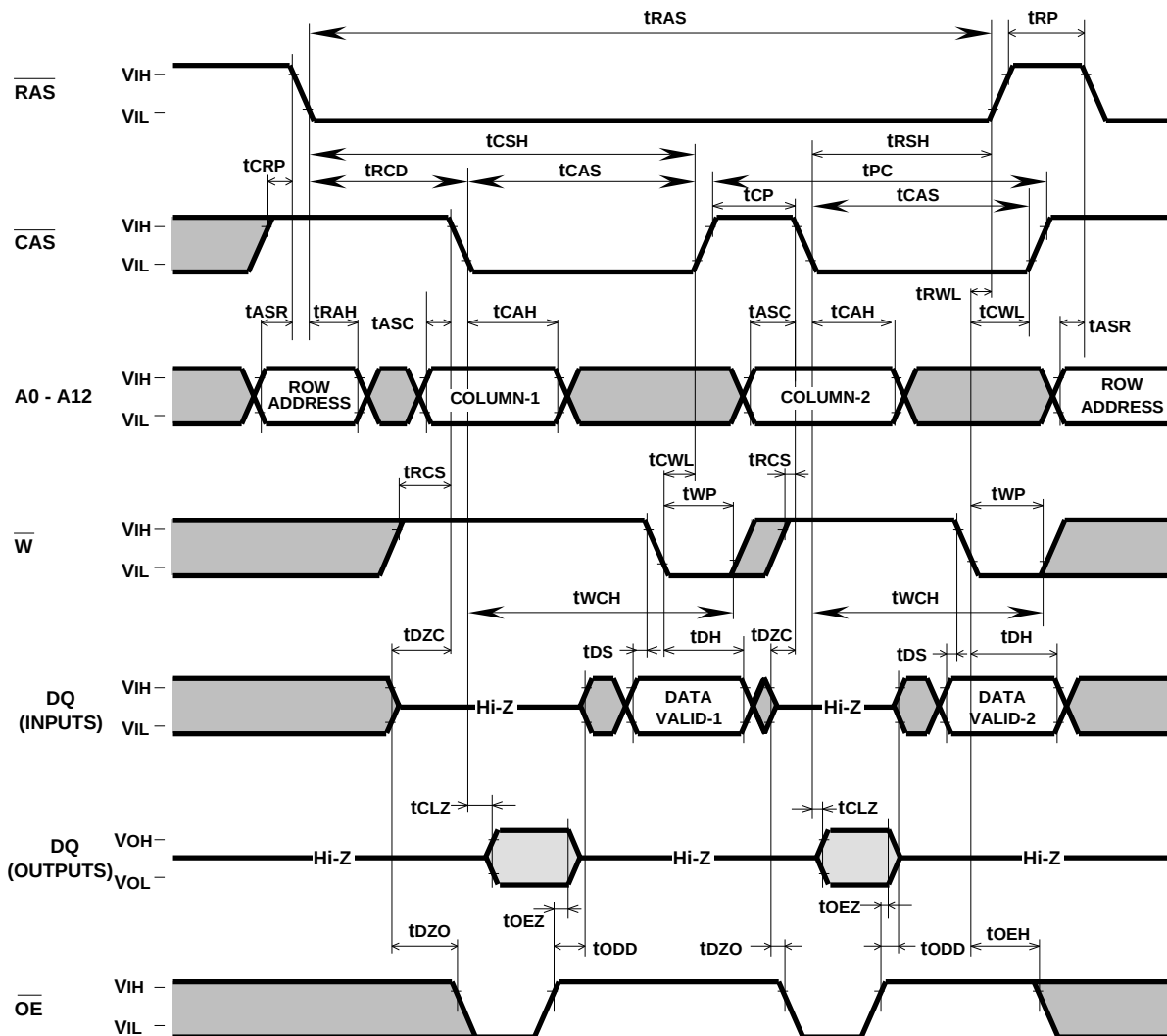


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Fast-Page Mode Write Cycle (Delayed Write)

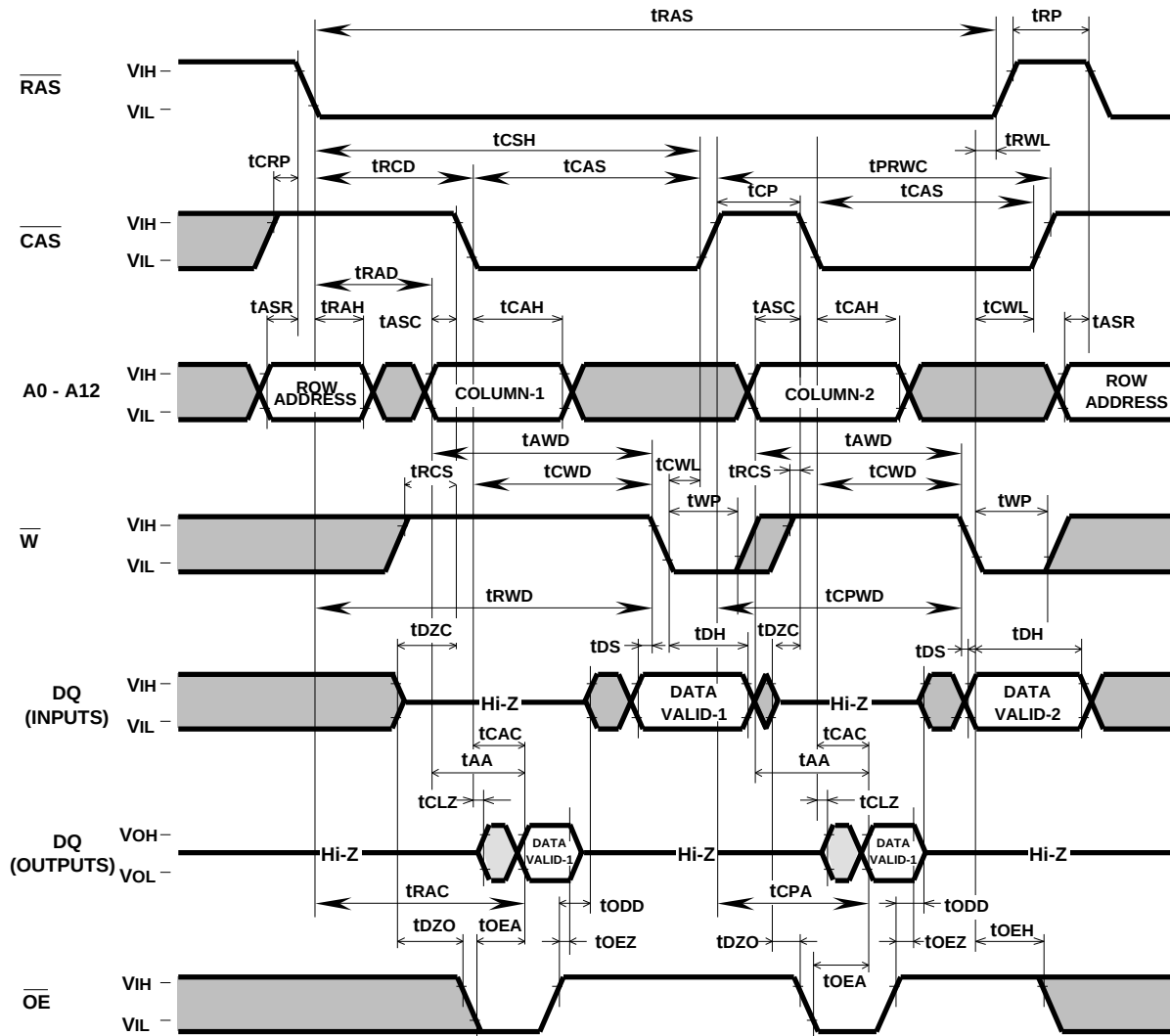


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Fast Page Mode Read-Write,Read-Modify-Write Cycle



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