DATA SHEET

GP326813A

Multimedia Processor

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Version 1.3

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Table of Contents

PAGE

1. GENERAL DESCRIPTION 4

2. FEATURES 4

3. BLOCK DIAGRAM 5

4. SIGNAL DESCRIPTIONS 6

4.1. PACKAGE PIN SEQUENCE - SLQFP 128 PACKAGE TOP VIEW 10

5. FUNCTION DESCRIPTIONS 11

5.1. CPU 11

5.2. MEMORY 11

5.2.1. Internal SRAM 11

5.2.2. External memory 11

5.3. PLL, CLOCK, POWER MODE 11

5.3.1. PLL (Phase Lock Loop) 11

5.3.2. System clock 11

5.4. POWER SAVINGS MODE 11

5.5. VIDEO INPUT INTERFACE 11

5.6. SOUND PROCESS UNIT (SPU) 11

5.7. VIDEO OUTPUT INTERFACE 11

5.7.1. STN-LCD interface 11

5.7.2. TFT-LCD interface 11

5.7.3. TV encoder 11

5.7.4. Scaling engine 12

5.8. MPEG4 DECODER 12

5.9. JPEG CODEC 12

5.10. INTERRUPT 12

5.11. I/O 12

5.11.1. GPIO 12

5.11.2. Key scan function 12

5.12. TIMER / COUNTER 12

5.13. WATCHDOG 13

5.14. SERIAL INTERFACE 13

5.14.1. Serial Peripheral Interface (SPI) 13

5.14.2. UART/IrDA function 13

5.14.3. USB2.0 Mini-host/Device function 14

5.15. DMA CONTROLLER 14

5.16. SECURE DIGITAL / MULTI-MEDIA CARD CONTROLLER 14

5.17. MEMORY STICK CONTROLLER 14

5.18. BOOST DC-DC CONTROL LOGIC 14

5.19. REAL TIME CLOCK (RTC) 14

5.20. MIPI FUNCTION 14

5.21. ANALOG CONTROL 14

5.21.1. DAC control 14

5.21.2. ADC control 14

6. ELECTRICAL SPECIFICATIONS 15
6.1. ABSOLUTE MAXIMUM RATING 15
6.2. DC CHARACTERISTICS 15
6.3. VIDEO DAC CHARACTERISTICS 15
6.4. AUDIO DAC CHARACTERISTICS 16
6.5. ADC CHARACTERISTICS 16
6.6. REGULATOR CHARACTERISTICS 16
6.7. DC-DC CHARACTERISTICS 16
7. RECOMMENDED BOARD LAYOUT 17
7.1. POWER AND GROUND 17
7.2. CRYSTAL AND PLL 17
8. PACKAGE/PAD LOCATIONS 18
8.1. ORDERING INFORMATION 18
8.2. PACKAGE INFORMATION 18
9. DISCLAIMER 20
10. REVISION HISTORY 21

MULTIMEDIA PROCESSOR

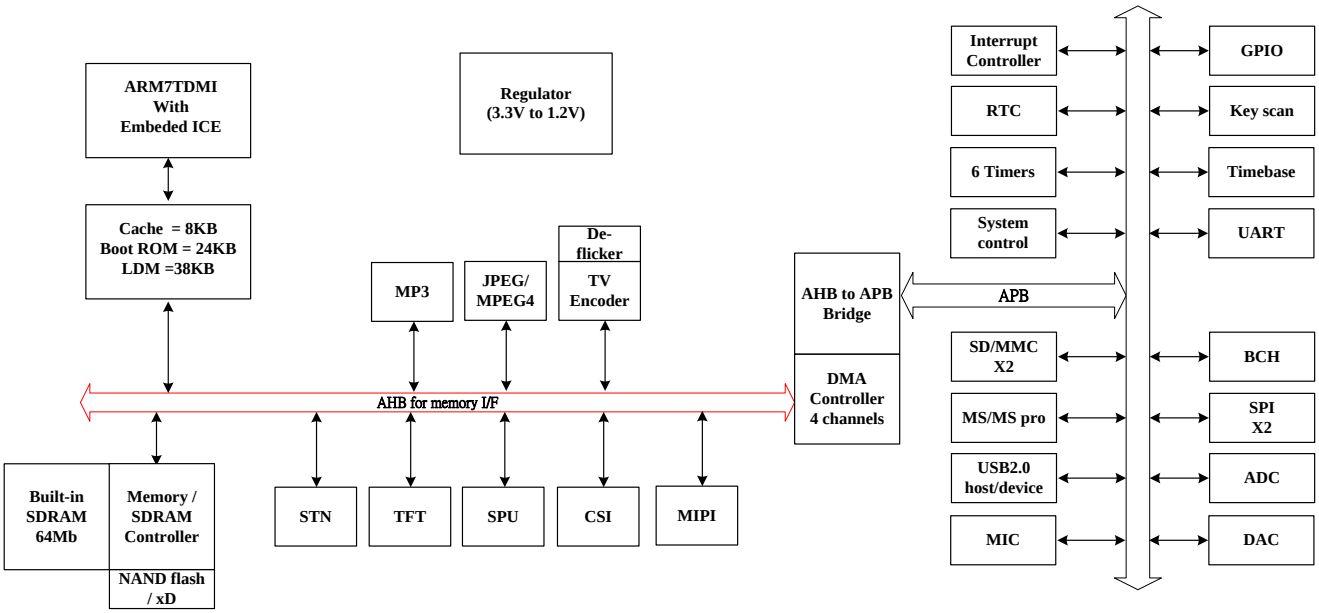
1. GENERAL DESCRIPTION

The GPL326813A multimedia processor, based on a high performance and power-efficient ARM7TDMI core operating at up to 96MHz, is enhanced with image, video processing, power saving, and system peripherals. The high-speed JPEG CODEC supports image resolution up to 64M pixels and features thumbnail decoding, image clipping and image sub-sampling functions. The face detection is able to detect multiple faces in an image. The GPL326813A processor is designed to connect with various types of memory card interfaces such as SD, SDHC, SDIO, MMC, MS, and MS pro, etc. To work with other devices or components easily and conveniently, GPL326813A supports the industrial standard USB 2.0 (compatible with USB 1.1 and 2.0) for mini-host and device function. These fully featured peripherals and functions make GPL326813A one of the best multimedia-processor SoC solutions in the industry- making your products more competitive in today's market.

2. FEATURES

- ARM7TDMI CPU with 8KB unified ID-cache, write buffer, embedded JTAG ICE, and working frequency up to 96MHz.
- 38KB SRAM for local data buffer.
- Sound Process Unit. (SPU)
  - 16 hardware PCM/ADPCM channels.
  - Built-in dynamic volume compressor.
  - MP3/WMA decoder.
- JPEG CODEC.
  - ISO/IEC 10918-1 baseline JPEG.
  - High-speed Decoding and Encoding with resolution up to 64MPixel.
  - Hardware Motion JPEG Decoding and Encoding (up to VGA@30fps) for real-time video record and playback application.
- MPEG4 decoder.
  - H.263 baseline profile level30, MPEG4 simple profile level3 Decoder (up to 30 fps @ 640 x 480 resolution).
  - Built-in de-blocking filter.
- Binary transformation engine for sensor input
- MIPI Function
  - Up to 450M bit rate
- Video-in & CMOS sensor interface and CCIR601/CCIR656 standard supported.
- Embedded 4Mx16 Bits SDRAM
- Static memory controller. (NAND FLASH with ECC and 4/ 8/ 12/ 16/ 24/ 40/ 60 -bit BCH)
- Four-channel DMA controller.
- Mono and 16 gray levels STN-LCD controller.
- TFT-LCD controller.
  - UPS051. (serial RGB)
  - UPS052. (serial RGB dummy)
  - Parallel RGB (6-6-6/8-8-8).
  - I80 (8-bit/16-bit/18-bit system bus) I/F type.
  - CCIR601/CCIR656.
  - Scaling engine inside with programmable up-scaling and down-scaling factor.
- Image Processing Unit.
  - Histogram statistics for auto brightness and contrast.
  - Programmable RGB gamma correction.
  - Color convert matrix for various post-image processing.
- 2-channel DC-DC Boost control circuit for LED Backlight and VGH/VGL voltage generator of TFT-LCD drivers.
- Interrupt Controller.
- Universal Serial Bus (USB) 2.0 high/full speed compliance device and USB mini-host with built-in transceiver.
- Watchdog timer.
- Six 16-bit timers/counters.
- Two sets of SD/ SDHC/ SDIO/ MMC card interface.
- MS/MS pro card interface.
- xD card interface.
- Two sets of SPI (master/slave) interface with data rate up to 24Mbps.
- UART (asynchronous serial I/O) or IrDA interface with baud rate up to 1.8432Mbps and 115.2Kbps.
- 81 Programmable general I/O ports (GPIO) with pull-high/low control.
- 64/88 keys scan controller.
- Power manager.
- Built-in 3.3V to 1.2V Regulator.
- Low voltage reset.
- One data lane MIPI
- Real-time clock (RTC) with independent power supply.
- 96MHz, 27MHz and 12MHz PLL.
- 16-bit stereo DAC (2-channel) for audio playback.
- 12-bit ADC with 6 line-in channels.
- MIC with PGAC. (program gain control)
- TV encoder supporting NTSC/PAL and de-flicker and scaling function.

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Package No	Name	Group	Type	Normal Function Description	GPIO Group
128	V12_REG	REG	P	Regulator 1.2V output	
128	V12_REG	REG	P	Regulator 1.2V output	
1	V12_FB	REG	P	Regulator 1.2V feedback pin	
2	VSS_REG	REG	P	Regulator ground	
3	V33_REG	REG	P	3.3V Regulator power	
3	V33_REG	REG	P	3.3V Regulator power	
3	V33_IO	PWM	P	3.3V PWM power	
4	FB1	PWM	AI,I/O	PWM1 feedback pin	IOG14
5	FB0	PWM	AI,I/O	PWM0 feedback pin	IOG11
6	VSS_IO	PWM	P	PWM ground	
7	PWM1	PWM	AO,I/O	PWM1 switch control pin	IOG13
8	VC1	PWM	AO,I/O	PWM1 frequency compensation pin	IOG15
9	PWM0	PWM	AO,I/O	PWM0 switch control pin	IOG10
10	AVSSRX	USB20PHY	P	USB20phy RX ground	
10	AVSSTX	USB20PHY	P	USB20phy TX ground	
11	DM	USB20PHY	AI/O	USB20phy DM signal	
12	DP	USB20PHY	AI/O	USB20phy DP signal	
13	AVDDRX	USB20PHY	P	USB20phy RX power	
13	AVDDTX	USB20PHY	P	USB20phy TX power	
13	VDD33	Digital PWR	P	3.3V digital power	
14	BKWEB	SDRAM I/F	I/O	SDRAM write enable pin	
	XA16	SDRAM I/F	I/O	SDRAM address pin 16:CAS	
	XA15	SDRAM I/F	I/O	SDRAM address pin 15:RAS	
	SDRAM_CSB	SDRAM I/F	I/O	SDRAM Chip select	IOF4
	XA13	SDRAM I/F	I/O	SDRAM address pin 13:BANK0	IOG8
	XA14	SDRAM I/F	I/O	SDRAM address pin 14:BANK1	IOG7
	XA10	SDRAM I/F	I/O	SDRAM address pin 10	
	XA0	SDRAM I/F	I/O	SDRAM address pin 0	
	XA1	SDRAM I/F	I/O	SDRAM address pin 1	
	XA2	SDRAM I/F	I/O	SDRAM address pin 2	
	XA3	SDRAM I/F	I/O	SDRAM address pin 3	
14	VDD33	Digital PWR	P	3.3V digital power	
	VDD33	Digital PWR	P	3.3V digital power	
15	IOB2	TFT/LCD	I/O	TFT VSYNC; TFT CKV	
16	IOB3	TFT/LCD	I/O	TFT DCLK	
17	IOC11	NAND IF	I/O	Nand flash ready	
18	BKCSB2	Memory I/F	I/O	SDRAM chip select 2	IOF2
19	BKCSB1	Memory I/F	I/O	SDRAM chip select 1	IOF1
	VSS	Digital GND	G	Digital ground	
20	VSS	Digital GND	G	Digital ground	
	XA4	SDRAM I/F	I/O	SDRAM address pin 4	
	XA5	SDRAM I/F	I/O	SDRAM address pin 5	
	XA6	SDRAM I/F	I/O	SDRAM address pin 6	
	XA7	SDRAM I/F	I/O	SDRAM address pin 7	
	XA8	SDRAM I/F	I/O	SDRAM address pin 8	

Package No	Name	Group	Type	Normal Function Description	GPIO Group
	XA9	SDRAM I/F	I/O	SDRAM address pin 9	
	XA11	SDRAM I/F	I/O	SDRAM address pin 11	
	XA12	SDRAM I/F	I/O	SDRAM address pin 12	IOG9
	SDRAM_CKE	SDRAM I/F	I/O	SDRAM CKE	IOH1
	SDRAM_CLK	SDRAM I/F	I/O	SDARAM CLK	
20	VSS	Digital GND	G	Digital ground	
21	V33_RTC	PLL	P	3.3V RTC power	
22	X32KI	PLL	I	32768Hz crystal input pin	
23	X32KO	PLL	O	32768Hz crystal output pin	
24	ALM	PLL	P	RTC Alarm	
25	VSS_CLKGEN	PLL	O	PLL Ground	
26	X12MI	PLL	I	12MHz crystal input pin	
27	X12MO	PLL	O	12MHz crystal output pin	
28	V33_CLKGEN	PLL	P	3.3V PLL power	
29	V33_VDAC	VDAC	P	3.3V VDAC power	
30	AOUT	VDAC	AO, I/O	Video DAC output	
31	CBU	VDAC	AO	Video DAC reference voltage	
32	VSS_VDAC	VDAC	G	3.3V VDAC ground	
33	IOA15	TFT/LCD	I/O	TFT-LCD's D15 / Key-scan's input 7	
34	IOA14	TFT/LCD	I/O	TFT-LCD's D14 / Key-scan's input 6	
35	IOA13	TFT/LCD	I/O	TFT-LCD's D13 / Key-scan's input 5	
36	IOA12	TFT/LCD	I/O	TFT-LCD's D12 / Key-scan's input 4	
37	IOA11	TFT/LCD	I/O	TFT-LCD's D11 / Key-scan's input 3	
38	IOA10	TFT/LCD	I/O	TFT-LCD's D10 / Key-scan's input 2	
39	IOA9	TFT/LCD	I/O	TFT-LCD's D9 / Key-scan's input 1	
40	IOA8	TFT/LCD	I/O	TFT-LCD's D8 / Key-scan's input 0	
41	IOA7	TFT/LCD	I/O	TFT-LCD's D7 / Key-scan's output 7	
42	IOA6	TFT/LCD	I/O	TFT-LCD's D6 / Key-scan's output 6	
43	IOA5	TFT/LCD	I/O	TFT-LCD's D5 / Key-scan's output 5	
44	IOA4	TFT/LCD	I/O	TFT-LCD's D4 / Key-scan's output 4	
45	IOA3	TFT/LCD	I/O	TFT-LCD's D3 / Key-scan's output 3	
46	IOA2	TFT/LCD	I/O	TFT-LCD's D2 / Key-scan's output 2	
47	IOA1	TFT/LCD	I/O	TFT-LCD's D1 / Key-scan's output 1	
	XA18	SDRAM I/F	I/O	SDRAM address pin 18	
48	IOA0	TFT/LCD	I/O	TFT-LCD's D0 / Key-scan's output 0	
49	VSS	Digital GND	G	Digital ground	
50	VDD12	Digital PWR	P	1.2V digital power	
51	VDD33	Digital PWR	P	3.3V digital power	
52	IOI0	NAND IF	I/O	Nand Data0	
53	IOI1	NAND IF	I/O	Nand Data1	
54	IOI2	NAND IF	I/O	Nand Data2	
55	IOI3	NAND IF	I/O	Nand Data3	
56	IOI4	NAND IF	I/O	Nand Data4	
57	IOI5	NAND IF	I/O	Nand Data5	
58	IOI6	NAND IF	I/O	Nand Data6	
59	IOI7	NAND IF	I/O	Nand Data7	

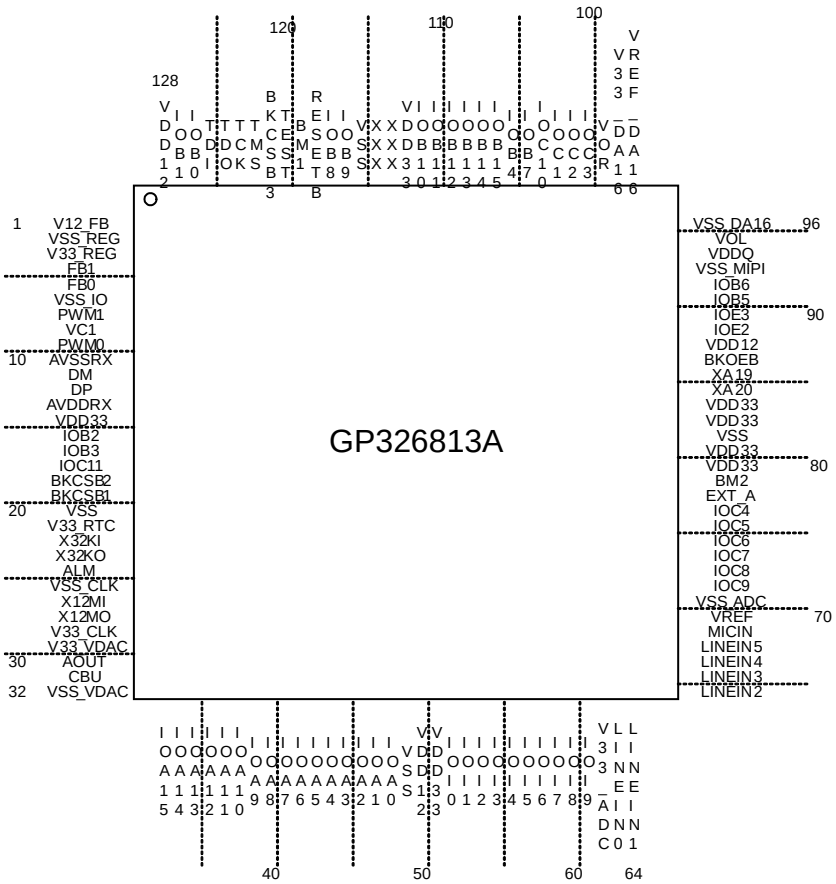
Package No	Name	Group	Type	Normal Function Description	GPIO Group
60	IOI8	NAND IF	I/O	Nand ALE	
61	IOI9	NAND IF	I/O	Nand CLE	
62	V33_ADC	ADC	P	3.3V ADC Power	
63	LINEIN0	ADC	A/I	LINEIN0 of 12-bit ADC	IOF6
64	LINEIN1	ADC	A/I	LINEIN1 of 12-bit ADC	IOF7
65	LINEIN2	ADC	A/I	LINEIN2 of 12-bit ADC	IOF8
66	LINEIN3	ADC	A/I	LINEIN3 of 12-bit ADC	IOF9
67	LINEIN4	ADC	A/I	LINEIN4 of 12-bit ADC	IOH6
68	LINEIN5	ADC	A/I	LINEIN5 of 12-bit ADC	IOH7
69	MICIN	ADC	I/O	MIC	IOH8
70	VREF	ADC	I/O	MIC	IOH9
71	VSS_ADC	ADC	P	ADC ground	
72	IOC9	SD/MS I/F	I/O	SD DATA2 / MS DATA2	
73	IOC8	SD/MS I/F	I/O	SD DATA1 / MS DATA1	
74	IOC7	SD/MS I/F	I/O	SD DATA0 / MS DATA0	
75	IOC6	SD/MS I/F	I/O	SD DATA3 / MS DATA3	
76	IOC5	SD/MS IF	I/O	SD CLK / MS CLK	
77	IOC4	SD/MS IF	I/O	SD CMD / MS BS	
78	EXT_A	EXT	I/O	External INT0	IOF5
79	BM2	MODE	I/O	Boot mode select pin 2, default input floating	IOF15
	XD8	SDRAM I/F	I/O	SDRAM data pin 8	
80	VDD33	Digital PWR	P	3.3V digital power	
	VDD33	Digital PWR	P	3.3V digital power	
	XD9	SDRAM I/F	I/O	SDRAM data pin 9	
	XD10	SDRAM I/F	I/O	SDRAM data pin 10	
	VSS	Digital GND	G	Digital ground	
	VSS	Digital GND	G	Digital ground	
	XD11	SDRAM I/F	I/O	SDRAM data pin 11	
	XD12	SDRAM I/F	I/O	SDRAM data pin 12	
81	VDD33	Digital PWR	P	3.3V digital power	
	VDD33	Digital PWR	P	3.3V digital power	
	XD13	SDRAM I/F	I/O	SDRAM data pin 13	
	XD14	SDRAM I/F	I/O	SDRAM data pin 14	
	VSS	Digital GND	G	Digital ground	
	VSS	Digital GND	G	Digital ground	
	XD15	SDRAM I/F	I/O	SDRAM data pin 15	
	VSS	Digital GND	G	Digital ground	
82	VSS	Digital GND	G	Digital ground	
	VDD33	Digital PWR	P	3.3V digital power	
83	VDD33	Digital PWR	P	3.3V digital power	
	XD0	SDRAM I/F	I/O	SDRAM data pin 0	
83	VDD33	Digital PWR	P	3.3V digital power	
	VDD33	Digital PWR	P	3.3V digital power	
	XD1	SDRAM I/F	I/O	SDRAM data pin 1	
	XD2	SDRAM I/F	I/O	SDRAM data pin 2	
	VSS	Digital GND	G	Digital ground	

Package No	Name	Group	Type	Normal Function Description	GPIO Group
	VSS	Digital GND	G	Digital ground	
	XD3	SDRAM I/F	I/O	SDRAM data pin 3	
	XD4	SDRAM I/F	I/O	SDRAM data pin 4	
84	VDD33	Digital PWR	P	3.3V digital power	
	VDD33	Digital PWR	P	3.3V digital power	
	XD5	SDRAM I/F	I/O	SDRAM data pin 5	
	XD6	SDRAM I/F	I/O	SDRAM data pin 6	
	VSS	Digital GND	G	Digital ground	
	VSS	Digital GND	G	Digital ground	
85	XA20	Memory I/F	I/O	External memory address pin 20	IOG5
	XD7	SDRAM I/F	I/O	SDRAM data pin 7	
86	XA19	Memory I/F	I/O	External memory address pin 19	IOG6
87	BKOEB	Memory I/F	I/O	External memory output enable pin	IOH0
88	VDD12	Digital PWR	P	1.2V digital power	
88	V12_MIPI	MIPI	P	MIPI 1.2V power	
89	IOE2	UART	I/O	UART/IrDA transmit data pin	MIPI CLKP
90	IOE3	UART	I/O	UART/IrDA receive data pin	MIPI CLKN
91	IOB5	TFT/LCD	I/O	TFT vertical start pulse	MIPI DP
92	IOB6	TFT/LCD	I/O	TFT horizontal start pulse	MIPI DN
93	VSS_MIPI	MIPI	G	MIPI Ground	
94	NC				
95	VOL	ADAC	AO	Left channel audio output	
96	VSS_DA16	ADAC	P	ADAC ground	
97	VREF_DA16	ADAC	AO	ADAC reference voltage	
98	V33_DA16	ADAC	P	3.3V ADAC power	
99	VOR	ADAC	AO	Right channel audio output	
100	IOC3	SPI	I/O	SPIRX: SPI data input	
101	IOC2	SPI	I/O	SPITX: SPI data output	
102	IOC1	SPI	I/O	SPICLK: SPI clock	
103	IOC10	EXT	I/O	External INT B	
104	IOB7	GPIO	I/O	GPIO	
105	IOB4	GPIO	I/O	GPIO	
106	IOB15	TFT/LCD	I/O	TFT-LCD's D23	
107	IOB14	TFT/LCD	I/O	TFT-LCD's D22	
108	IOB13	TFT/LCD	I/O	TFT-LCD's D21	
109	IOB12	TFT/LCD	I/O	TFT-LCD's D20	
110	IOB11	TFT/LCD	I/O	TFT-LCD's D19	
111	IOB10	TFT/LCD	I/O	TFT-LCD's D18	
112	VDD33	Digital PWR	P	3.3V digital power	
	XA17	SDRAM I/F	I/O	SDRAM address pin 17	
115	VSS	Digital GND	G	Digital ground	
116	IOB9	TFT/LCD	I/O	TFT-LCD's D17	
117	IOB8	TFT/LCD	I/O	TFT-LCD's D16	
118	RESETB	SYSTEM	I	Reset input pin. (Low active)	
119	BM1	MODE	I/O	Boot mode select pin 1, default input floating	IOF14
120	TEST	MODE	I	Test mode control signal, connect to ground for	

Package No	Name	Group	Type	Normal Function Description	GPIO Group
				normal operation.	
121	BKCSB3	Memory I/F	I/O	External memory chip select 3	IOF3
122	TMS	ICE	I/O	Embedded ICE input in	IOH5
123	TCK	ICE	I/O	Embedded ICE clock input pin	IOH4
124	TDO	ICE	I/O	Embedded ICE output pin	IOH3
125	TDI	ICE	I/O	Embedded ICE input pin	IOH2
126	IOB0	TFT/LCD	I/O	TFT DE; TFT OEV	
127	IOB1	TFT/LCD	I/O	TFT HSYNC; TFT LD	
128	VDD12	Digital PWR	P	1.2V digital power	

Note: AO: Analog Output, AI: Analog Input

4.1. Package Pin Sequence - SLQFP 128 Package Top View



5. FUNCTION DESCRIPTIONS

5.1. CPU

The GP326813A, capable of running up to 96MHz, integrates the ARM7TDMI CPU with Embedded JTAG ICE and Cache Controller, which supports 8K-byte unified ID-cache, 8-entry write buffer and 38K-byte internal SRAM. When Cache is enabled, any CPU's R/W will be fetched to the cache instead of external memory to enhance CPU performance. In addition, the internal SRAM bus, I/O bus and cache bus are separated to maximize CPU bus bandwidth.

5.2. Memory

5.2.1. Internal SRAM

The 38K-byte internal SRAM is generally treated as program's stack. It can also be accessed by other masters, for example, DMA, USB, SPU, or NAND Flash controller to reduce bandwidth of external memory.

5.2.2. External memory

The 8-bit NAND flash data bus is supported with an embedded 4/ 8/ 12/ 16/ 24/ 40/ 60-bit ECC/ BCH calculation circuit which can realize the error correction mechanism on SLC/MLC NAND flash.

5.3. PLL, Clock, Power Mode

5.3.1. PLL (Phase Lock Loop)

There are three PLLs embedded in GP326813A, the 1st PLL capable of pumping up to 96MHz, the 2nd PLL for 27MHz, and the 3rd PLL for 12MHz. The output frequency of fast PLL is programmable and is ranged from 12MHz ~ 129MHz. (3MHz per step)

5.3.2. System clock

One of the following system clocks can be selected via register configuration: 32768Hz, 12MHz or 96MHz (determined by fast PLL's output frequency). Furthermore, a clock divider is provided to reduce power consumption. (The divisor is up to 128).

5.4. Power Savings Mode

The GP326813A features four power saving modes to extend power life - Normal, Wait, Halt, and Sleep.

Mode	CPU	System	RTC	After wakeup
Normal	ON	ON	ON	-
Wait	OFF	ON	ON	Next Instruction
Halt	OFF	OFF	ON	Reset CPU or not
Sleep	OFF	OFF	OFF	Reset System

Entering the Wait/Halt/Sleep mode is done by writing specific value to designated port. The wake-up source can be interrupt, Time Base, Key Change, RTC, EXT INT, UART RX or ADC.

5.5. Video Input Interface

The GP326813A supports video input from sensor or TV decoder. The maximum input resolution is 4095 x 4095. A built-in scaling unit can be used to scale input data from arbitrary resolution to VGA or QVGA mode. A motion detecting engine is able to recognize the interactive game with sensor input. The video-in interface supports CCIR601/CCIR656 format with YUV or RGB format. The output format is frame-based and the input frame rate does not need to synchronize with GP326813A system clock.

5.6. Sound Process Unit (SPU)

The GP326813A equips a 16-channel SPU. Each channel of SPU can support PCM8/ PCM16/ ADPCM36 and a dynamic volume compressor is also embedded to enlarge the overall volume. For software application, GP326813A is also available for MP3/ WMA decode and other wide-band (sample rate >= 16KHz) low bit-rate algorithm.

5.7. Video Output Interface

5.7.1. STN-LCD interface

The STN-LCD driver interface supports up to 320X240 LCD panel and 1-bit or 4-bit data bus for monochrome/gray-scale STN, as well as the Memory interface (i80 interface) type CSTN.

5.7.2. TFT-LCD interface

The GP326813A supports TFT-LCD controller with resolution up to 1024x768. The LCD/LCM interface includes parallel RGB, serial delta RGB, serial stripe RGB, CPU (MPU / i80) type, CCIR601/CCIR656, as well as the built-in Timing Controller. The TFT-LCD controller mainly provides four to seven timing control pins and 8, 16, or 18 data pins to control external TFT panel and they are VSYNC, HSYNC, DE, DCLK, POL, STV, STH and DATA. It also supports image clipping, sliding windows and the following image processing: histogram statistics for auto brightness and contrast, programmable RGB gamma correction and color convert matrix for various post-image processing.

5.7.3. TV encoder

The GP326813A also supports TV composite output with both NTSC and PAL mode. The output resolution can be up to 720x480. A 10-bit video DAC is embedded in GP326813A and it can utilize minimum system cost and best performance. The

de-flicker function is also featured to reduce the flicker effect under TV interlace mode.

5.7.4. Scaling engine

A powerful scaling engine is built to support both up-scaling and down-scaling image and video to fit the screen resolution of TV or TFT.

5.8. MPEG4 Decoder

The MPEG4 decoder supports MPEG4 simple profile and H.263 video decoding, which supports video resolution up to 720x480. Besides, it also includes built-in de-blocking filter to remove blocking artifacts in low bit-rate block-based video coding. The De-blocking filtering is considered as an important task due to improvement of visual quality in low bit-rate video coding. The MPEG4 decoder has real-time decoding up to VGA@30fps.

5.9. JPEG CODEC

The JPEG CODEC is a high speed hard-wired engine, which supports image resolution up to 64M pixels (8000x8000) and is compatible with ISO/IEC 10918-1 baseline. It supports 2 AC/DC programmable Huffman table and programmable luminance/chrominance quantization table. The JPEG Decoder engine supports the following formats: YUV444, YUV422, YUV420, YUV411 and YUV400 (gray mode). It also features thumbnail decoding, image clipping and image sub-sampling. The JPEG Encoder engine supports two formats: YUV422 and YUV420. It also supports CMOS Sensor data format encoding. For Motion JPEG application, the JPEG CODEC has both real-time decoding and encoding with up to VGA@30fps.

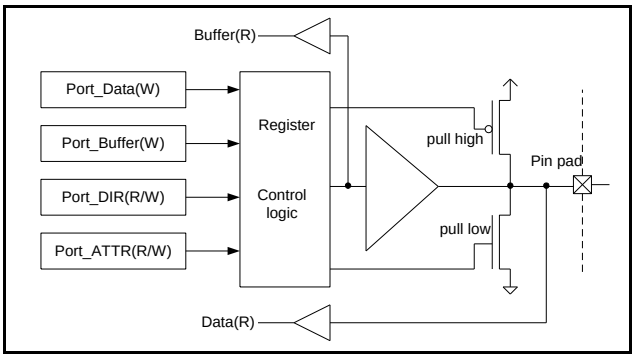
5.10. Interrupt

The GP326813A has 32 IRQ (Interrupt request) sources and 10 FIQ (Fast Interrupt request) sources. FIQ is the high-priority interrupt and IRQ is the low-priority. Hence, an IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. The priorities of 32 IRQ sources can be configured by programmers.

5.11. I/O

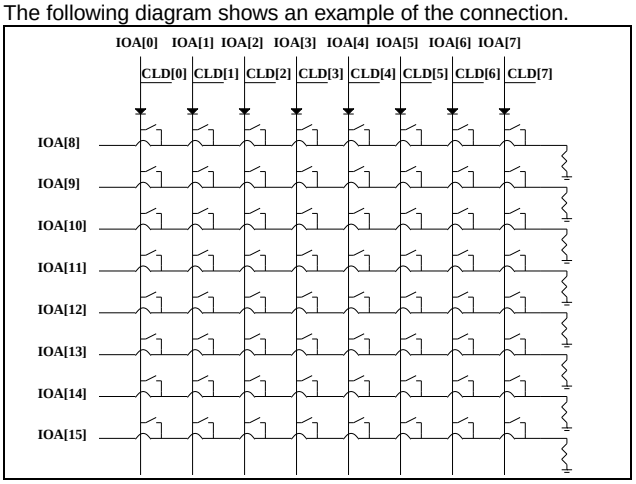
5.11.1. GPIO

GP326813A has eight I/O ports - IOA, IOB, IOC, IOE, IOF, IOG, IOH and IOI. Each I/O pin has its normal function and is described in the signal description section. When the normal function of the I/O is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.



5.11.2. Key scan function

The Key Scan function is output at IOA[7:0] and input with IOA[15:8] under 64 keys mode. Additional three outputs IOB[2:0] are required under 88 keys mode. The IOA [7:0] are shared with LCD data [7:0], which means the Key Scan function can still work even when 8-bit-data-bus LCD Display is turned on. However, when 16-bit data bus TFT-LCD panel is connected, the Key Scan function cannot work. Note that when Key Scan function IOA is shared with LCD panel, each output must connect a diode serially to the key pad which prevents possible LCD glitch caused by contention when more than one key is pressed at the same time. The following diagram shows an example of the connection.



5.12. Timer / Counter

Six 16-bit timers/counters are designed in GP326813A: TimerA, TimerB, TimerC, TimerD, TimerE, and TimerF. The clock source of each timer can be set individually. For TimerA to TimerD, an INT will be sent to CPU when timer overflow occurs. Besides, Capture, Comparison and PWM functions are also provided by TimerA/TimerB/TimerC.

Clock Source A	Clock Source B
Fosc/2	2048Hz
Fosc/256	1024Hz
32768Hz	256Hz
8192Hz	Time Base B

Clock Source A	Clock Source B
4096Hz	Time Base A
1	0
Another Timer	1
INT1	INT2

The GP326813A also features a Time Base controller to generate slow and precise interrupts form 32768Hz crystal. The following table shows the available Time Base.

TimeBase A	TimeBase B	TimeBase C
--	8Hz	128Hz
1Hz	16Hz	256Hz
2Hz	32Hz	512Hz
4Hz	64Hz	1024Hz

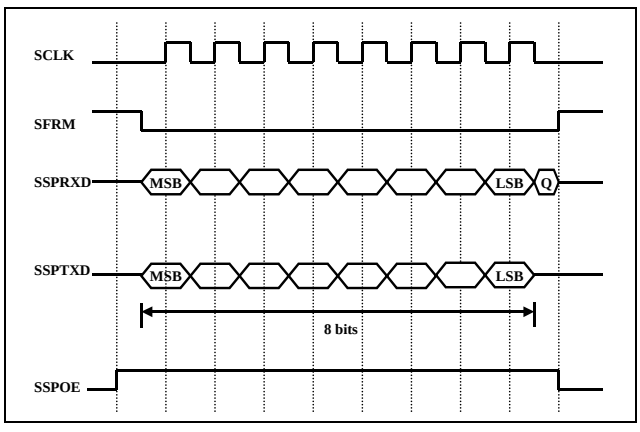
5.13. Watchdog

The purpose of watchdog is to monitor whether or not the system is operating normally. Within a certain period, watchdog must be cleared; otherwise, CPU assumes the program has been running in an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GP326813A, the clear period is software programmable. If watchdog is cleared before the period expires, the system will not be reset.

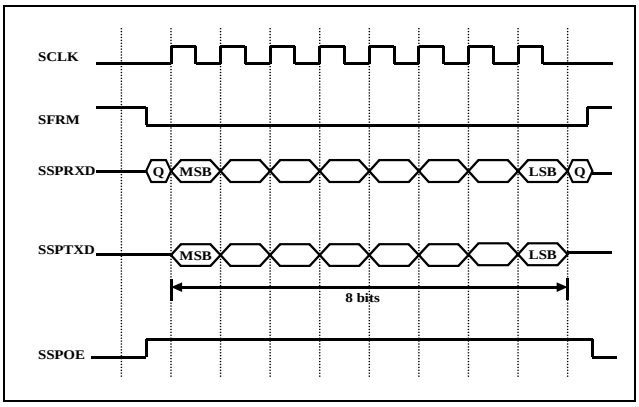
5.14. Serial Interface

5.14.1. Serial Peripheral Interface (SPI)

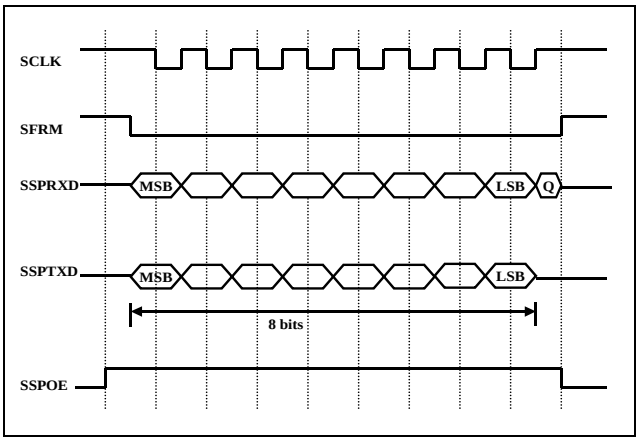
The SPI interface is a master/slave interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving functions. Four types of timings are supported and shown in the following diagram.



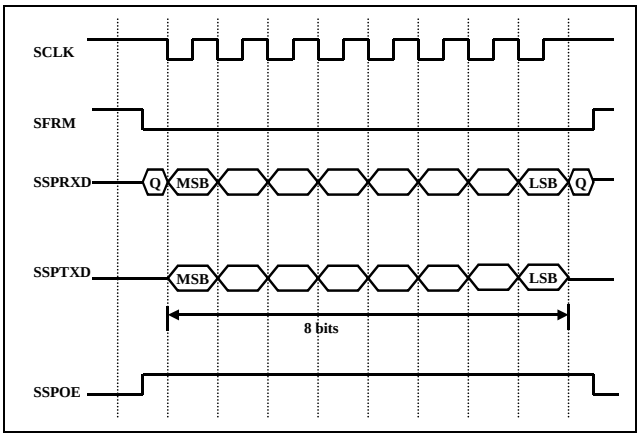
SPO = 0, SPH = 0, only this mode is supported in SPI slave mode.



SPO = 0, SPH = 1



SPO = 1, SPH = 0



SPO = 1, SPH = 1

5.14.2. UART/IrDA function

The UART/IrDA controller inside the GP326813A supports baud rate up to 1.8432MHz (UART). There are two dedicated 16-byte FIFOs. One is to prevent the data loss when receiving data and the other is to transmit data. DMA transfer is available for both transmitting and receiving operations.

5.14.3. USB2.0 Mini-host/Device function

The GP326813A has USB2.0 mini-host and device function, compatible with USB 1.1 and USB 2.0 high speed standards. The mini-host and device function are not allowed to be active at the same time. An USB transceiver is built-in for both host and devices function. A FIFO with size of 1024x8 is used for bulk-in and bulk-out transfer and a 64-byte FIFO is used for control pipe transfer. Interrupt IN/OUT pipes are also supported. The DMA transfer is enabled for bulk-in/out to maximize the transfer performance.

5.15. DMA Controller

The GP326813A provides four DMA channels and each channel can be individually configured in I/O to MEM, MEM to I/O or MEM to MEM mode.

5.16. Secure Digital / Multi-Media Card Controller

The SD/MMC controller is compatible with MMC system specification version 2.3, SD Memory Card specification 2.0, SDHC and SDIO card interface. The controller supports automatically CRC generation and check, 1-bit and 4-bit transfer, interrupt generation when buffer empty/full, DMA transfer for page read/write.

5.17. Memory Stick Controller

The GP326813A supports Memory Stick/Memory Stick PRO controller, which is compatible with Memory Stick PRO Spec ver.1.02. It provides one data signal in serial mode or four data signals in parallel mode and it uses CRC16 as a transaction protection code. An 8x32 bits bi-direction FIFO is featured when using page read/write TPC command. Multi-bytes register read/write and a page read/write by DMA are available.

5.18. Boost DC-DC Control Logic

The GP326813A supports 2-channel DC-DC Boost control circuit for LED Backlight and VGH/VGL voltage generator of TFT-LCD drivers to reduce the cost of application circuit.

5.19. Real Time Clock (RTC)

The RTC block supports independent power supply, and also offers the alarm function, schedule function, and day/ hour/ minute/ second/ half-second interrupt function.

5.20. MIPI Function

The GP326813A supports a mobile industry processor interface(MIPI) controller. It can support one data lane and output CCIR601 interface.

5.21. Analog Control

5.21.1. DAC control

A 16-bit stereo DAC (2-channel) is embedded for both left and right channels. A 16x16 FIFO is used to prevent the sound glitch when CPU is busy. The left and right channels do not need to have the same sample rate. A single DMA channel can utilize the stereo playback.

5.21.2. ADC control

A 12-bit ADC is embedded in GP326813A for general purpose application. The ADC has eight inputs which can be selected by software programming with max. 62.5KHz sample rate for total of eight channels. It also provides an independent MIC channel with PGAC function (Program Gain Control) for voice recording application, and Touch Panel interrupt function when Touch Panel application is applied.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	VDD33	-0.3 to 4.0	V
Supply Voltage 2	AVDD[3]	-0.3 to 4.0	V
Supply Voltage 3	VDD12 V12_MIPI	-0.3 to 1.32	V
Supply Voltage 4	V33_RTC	-0.3 to 4.0	V
Input Voltage	V_{IN}	-0.3 to 4.0	V
Operating Temperature	T_A	-40~85	℃

6.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	VDD33 AVDD[3]	3.0 3.0	3.3	3.6	V	-
Operating Voltage 2	VDD12 V12_MIPI	1.08	1.2	1.32	V	-
Operating Voltage 3	V33_RTC[4]	1.3~1.6	-	3.6	V	-
Operating Current	I_{OP}	-	120	-	mA	@96MHz, 3.3V, all clocks on Operating current may vary by different applications.
Power Down Current	I_{PD}	-	2	-	mA	Sleep Mode@3.3V
Power Off Current	-	-	-	10	uA	Independent RTC module power only@V33_RTC=3.0V
High Input Voltage	V_{IH}	0.7DVDD33	-	DVDD33	V	-
Low Input Voltage	V_{IL}	VSS	-	0.8	V	-
Crystal Frequency 1	-	-	32768	-	Hz	-
Crystal Frequency 2	$F_{CRYSTAL}$	-	12.0[1]	-	MHz	-
System Clock	F_{SYS}	256Hz[2]	48	96	MHz	-

Note1: 12M Crystal is needed when USB function or TV function is enabled.

Note2: By setting clock divider and changing system clock to 32768 mode.

Note3: AVDD includes V33_REG, V33_IO, AVDDRX, AVDDTX, V33_CLKGEN, V33_VDAC, V33_ADC, V33_DA16.

Note4: V33_RTC Min. operation voltage default 1.6V and can adjust by register setting.

6.3. Video DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	10	-	Bit	-
INL	±2	±1	-	LSB	-
DNL	±1	±0.5	-	LSB	-
Gain Error	4	2	-	LSB	-
Conversion Rate	-	16	-	ns	-

6.4. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	16	-	16	Bit	-
Full Scale Output Voltage	0.5*V33_DA	0.6*V33_DA	-	Vp-p	-
THD+N	-50db	-60dB	-	dB	-
Dynamic Range	75	90	-	dB	Fin=0.997KHz w/ -60dB output loading=125 ohm
Output Loading	100	100-	-	ohm	

6.5. ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range	V33_AD	2.7	-	3.6	V
Resolution of ADC	RESO	-	12	-	bits
Integral Non-Linearity of ADC	INL	±4	±2	-	LSB
Differential Non-Linearity of ADC	DNL	±2	±1	-	LSB
ENOB		9	9.4	-	bits
No Missing Code		10	11	-	bits
AD Conversion Rate=ADCCLK/16	F_{CONV}	-	-	64K	Hz

6.6. Regulator Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.3	3.3	3.6	V
Maximum Current Output	IREGO	-	150	250	mA
Output Voltage	VREGO	-	1.2	-	V

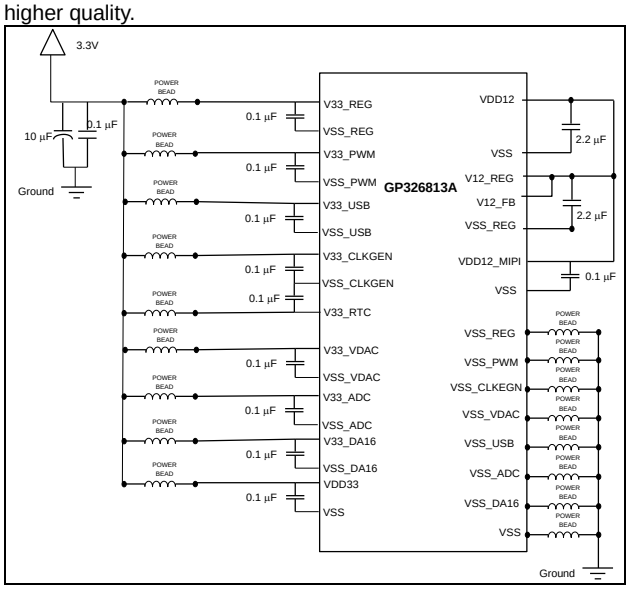
6.7. DC-DC Characteristics

Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
V_{33_IO} Operating Current		PWM0, PWM1	0.3	0.45	-	mA
V_{33_AD} Operating Current		FB0, FB1, VC1	0.1	0.15	-	mA
PWM0 Switching Frequency		fPWM0	-	600	-	kHz
PWM1 Switching Frequency		fPWM1	-	600	-	kHz
PWM0 Internal Reference Voltage		-	1.173	1.235	-	V
PWM1 Internal Reference Voltage	VSET[2:0]=000	-	94	99	-	mV
	VSET[2:0]=001	-	94	99	-	mV
	VSET[2:0]=010	-	141	148	-	mV
	VSET[2:0]=011	-	188	198	-	mV
	VSET[2:0]=100	-	235	247	-	mV
	VSET[2:0]=101	-	281	296	-	mV
	VSET[2:0]=110	-	329	346	-	mV
	VSET[2:0]=111	-	375	395	-	mV

7. RECOMMENDED BOARD LAYOUT

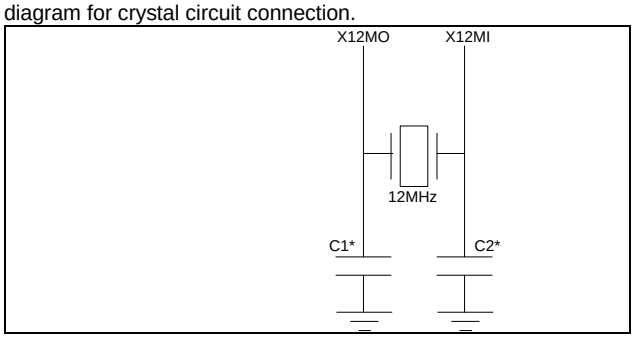
7.1. Power and Ground

All power and ground pins are connected as in the following diagram for general application. The decoupling capacitor of 0.1μF and 10μF should be connected to each corresponding power pin of the IC and 0.1uF capacitor must be as close as possible to the power pin. The POWER BEAD is optional for higher quality.



7.2. Crystal and PLL

When the 12MHz crystal is utilized in the system, normally for USB application, no additional circuit is required. For TV application requiring precise 12M clocks, please refer the follow diagram for crystal circuit connection.



Note*: C1 and C2 suggest values by follow rules:

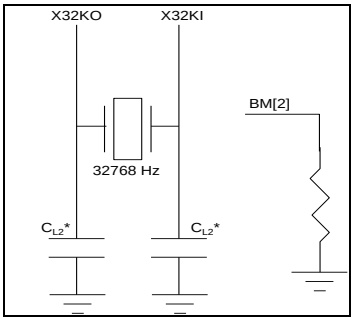
$C_1 = C_2 = (C_L - C_{stray})x2 - C_{ic}$

C_{ic} : IC internal capacitance is equal 15p ± 10%

C_{stray} : Stray capacitance in the circuit and PCB board get by measurement.

C_L : Load capacitance of 12M crystal get by crystal spec.

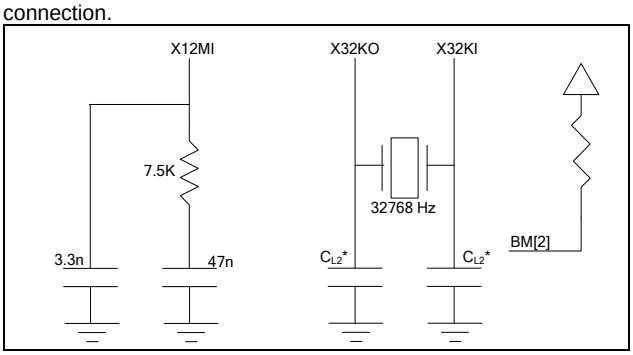
Note2: If Vpp, min = 1.2V @VDD =3.3V or Vpp, min = 1V @VDD =2.6V, the 12MHz crystal can normal work.



A Crystal (32768Hz) may be used for applications requiring precise time clocks. See the above diagram for details.

Note*: Please refer to the crystal's application circuit.

If 12MHz crystal is disabled to reduce cost of system BOM (Bill of Materials), please refer to the following diagram for crystal circuit connection.



Note1: If 12M crystal is not applied on the system, the system will not support USB and TV function.

8. PACKAGE/PAD LOCATIONS

8.1. Ordering Information

Product Number	Package Type
GP326813A-001A-QLMxx	SLQFP 128

Note1: Code number is assigned for customer.

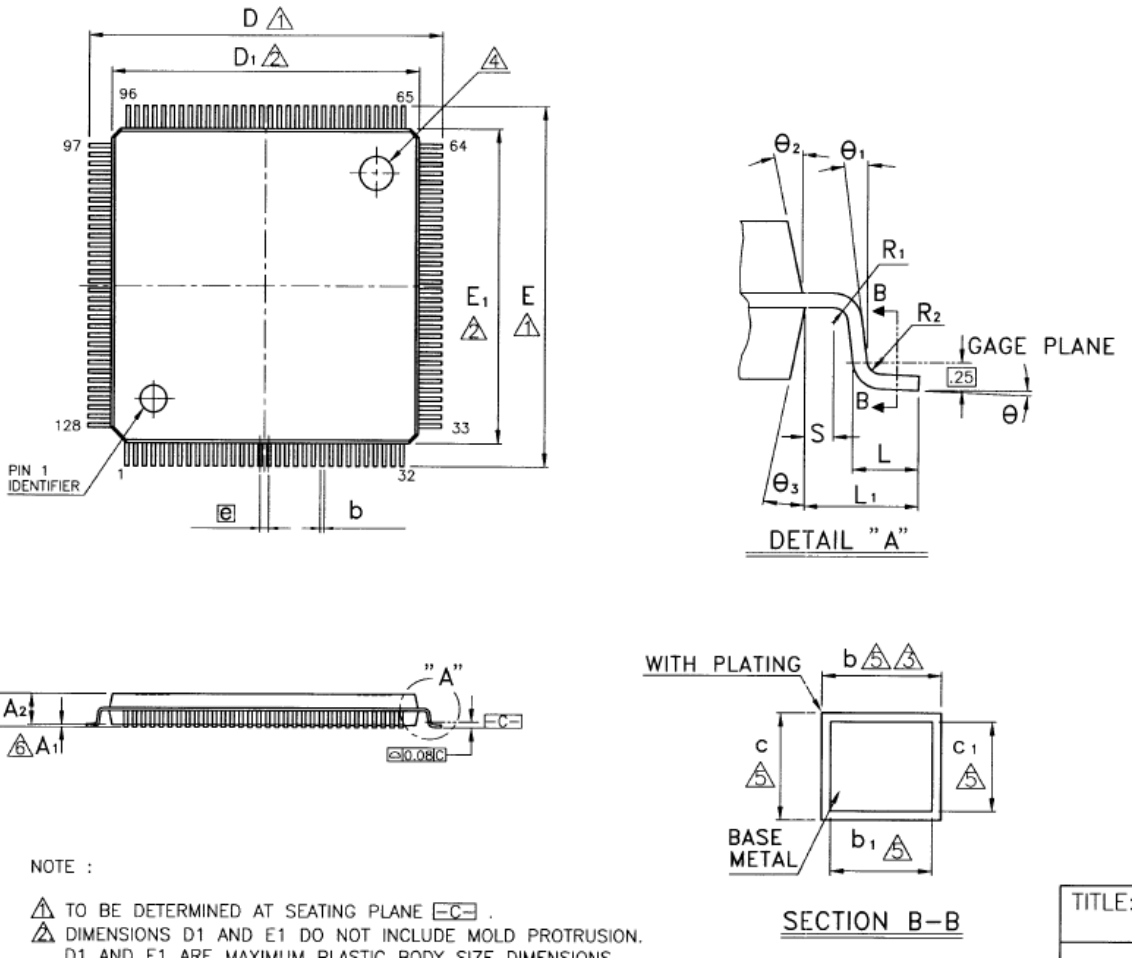
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

Note4: PartNumber_XXXX where "XXXX" is a 4-digit code, managed by Generalplus, to indicate additional software algorithm(s) or royalty type(s) applied to the product. Same part numbers bearing different codes make no differences in hardware specification.

8.2. Package Information

SLQFP 128



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	-	0.002	-	-
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	-	0.20	0.004	-	0.008
c_1	0.09	-	0.16	0.004	-	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	-	-	0.003	-	-
R_2	0.08	-	0.20	0.003	-	0.008
S	0.20	-	-	0.008	-	-
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	-	-	0°	-	-
θ_2	12° TYP			12° TYP		
θ_3	12° TYP			12° TYP		

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10. REVISION HISTORY

Date	Revision #	Description	Page
Oct. 01, 2018	1.3	Add Note 4 to chapter 8.1.	18
Oct 03, 2016	1.2	1. Replace VDAC Characteristics Table. 2. Replace ADC Characteristics. 3. Replace DAC Characteristics. 4. Replace DC2DC Characteristics. 5. Add note1 about using 32K or 12M Crystal: Note1: If 12M crystal is not applied on the system, the system will not support USB and TV function. 6. Add note2 about 12M Crystal: Note2: If Vpp, min = 1.2V @VDD =3.3V or Vpp, min = 1V @VDD =2.6V, the 12MHz crystal can normal work.	15 16 16 16 17 17
Jul 29, 2015	1.1	Remove Note3 from 6.2 DC Characteristics Table	15
Apr 14, 2015	1.0	Modify DC Characteristics.	15
Oct 20, 2014	0.5	Modify Ordering Information.	18
May 22, 2014	0.4	Modify the crystal from 6MHz to 12MHz in the content of Crystal and PLL chapter	17
Nov. 22, 2013	0.3	1. Modify Block Diagram add Embedded SDRAM Size and LDO Function 2. Modify 4.SIGNAL DESCRIPTION 3. Modify 6.2 DC Characteristic	
Apr. 02, 2013	0.2	The Min Operation Voltage(VDD33) 3.0V.	15
Mar. 12, 2013	0.1	Preliminary version.	21