



TGA2975-SM

2.7 to 3.5 GHz, 12 W GaN Power Amplifier

General Description

Qorvo's TGA2975-SM is a packaged MMIC power amplifier which operates from 2.7 to 3.5 GHz. The TGA2975-SM is designed using Qorvo's TQGaN25 0.25- μm GaN on SiC process.

The TGA2975-SM typically provides more than 41 dBm of saturated output power, 52% power-added efficiency, and 31 dB small signal gain. It can operate under both pulse and CW conditions.

The TGA2975-SM is available in a low-cost, surface mount 24 lead 5 mm x 5 mm overmold QFN. It is ideally suited to support both commercial and defense related radar applications.

Both RF ports have integrated DC blocking capacitors and are fully matched to 50 ohms.

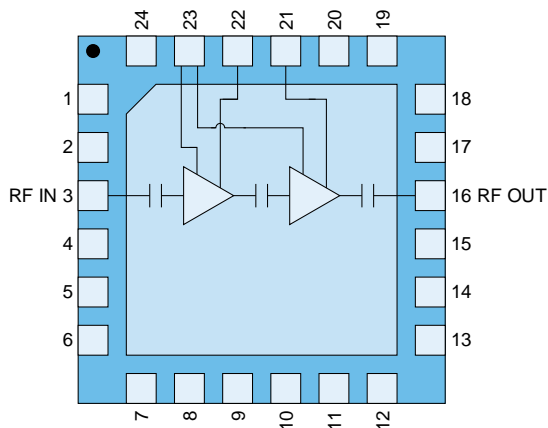
Lead-free and RoHS compliant

Evaluation Boards are available upon request.



QFN 5 x 5 mm 24 L

Functional Block Diagram



Product Features

- Frequency Range: 2.7-3.5 GHz
- P_{SAT} : >41 dBm (at $P_{IN} = 16$ dBm)
- PAE: >52 % (at $P_{IN} = 16$ dBm)
- Small Signal Gain: 31 dB
- Return Loss: > 9 dB
- Bias: $V_D = 28$ V, $I_{DQ} = 175$ mA
- Pulsed V_D : PW = 100 μs , DC = 10 %
- Package Dimensions: 5.0 x 5.0 x 0.85 mm

Applications

- Commercial and Military Radar

Pad Configuration

Pad no.	Symbol
1, 2, 4-15, 17-20, 24	NC
3	RF IN
16	RF OUT
21	DRAIN 2
22	DRAIN 1
23	GATE

Ordering Information

Part	Description
TGA2975-SM	2.7-3.5 GHz, 12 W GaN Power Amplifier
TGA2975-SM_EVB	TGA2975-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current (I_{D1})	225 mA
Drain Current (I_{D2})	1250 mA
Gate Current (I_G)	See Graph (page 12)
Power Dissipation (P_{DISS}), 85 °C	27 W
Input Power (P_{IN}), CW, 50 Ω , 85 °C	30 dBm
Input Power (P_{IN}), CW, VSWR 10:1, $V_D = 28$ V, 85 °C	23 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	28 V
Drain Current (I_{DQ})	175 mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

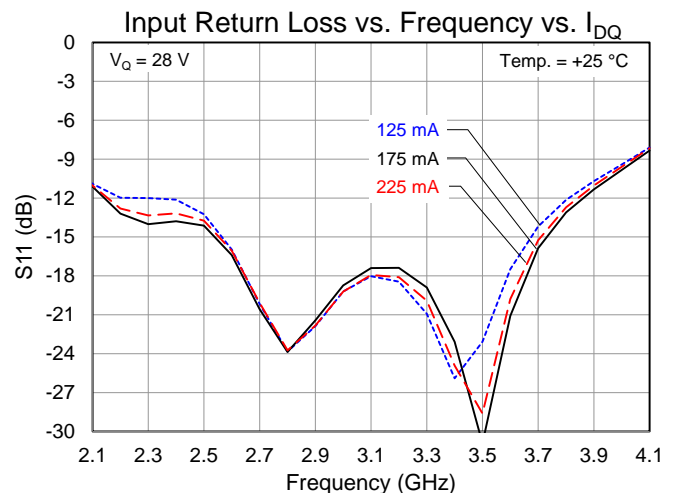
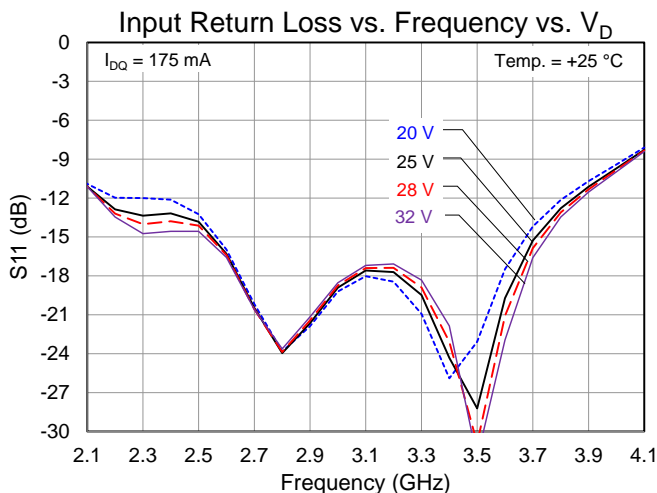
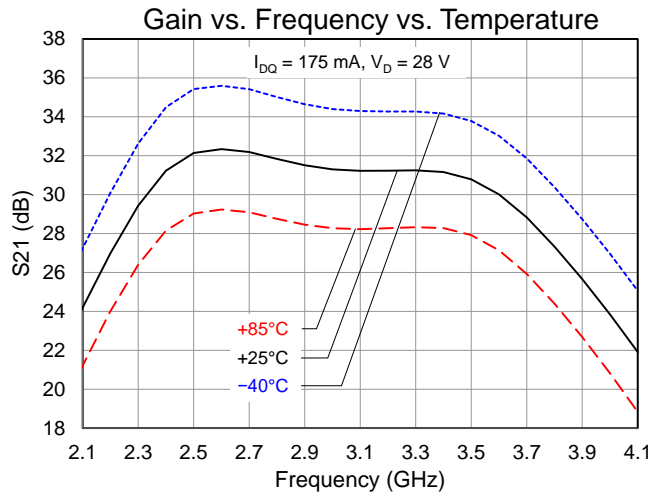
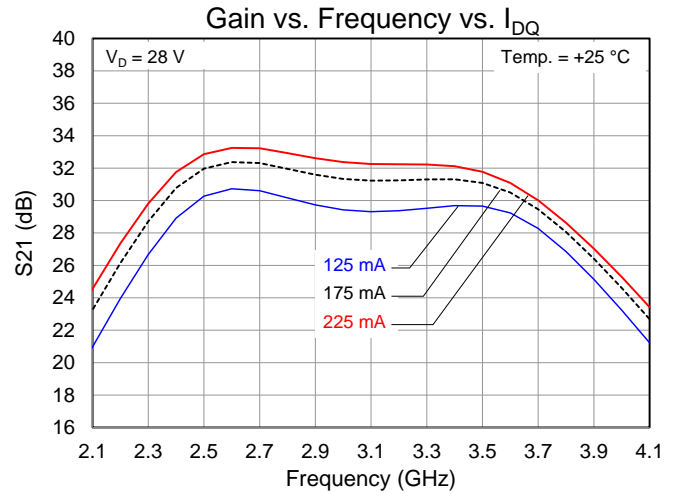
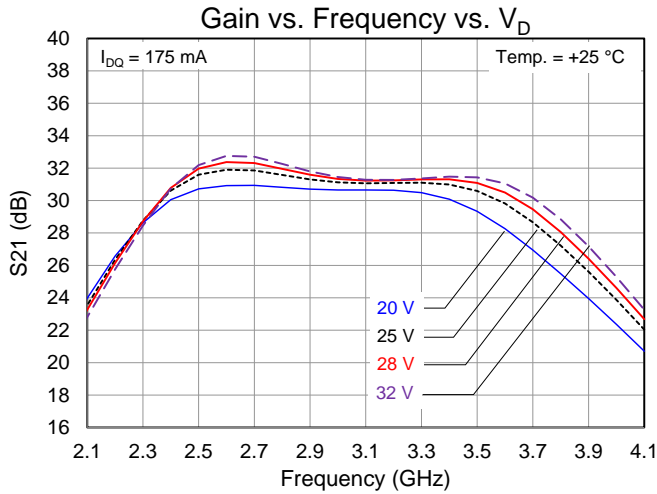
Electrical Specifications

Test conditions unless otherwise noted: 25 °C, $V_D = 28$ V, $I_{DQ} = 175$ mA, Pulsed V_D : PW = 100 μ s, DC = 10 %

Parameter	Min	Typical	Max	Units
Operational Frequency Range	2.7		3.5	GHz
Small Signal Gain		31		dB
Input Return Loss		> 15		dB
Output Return Loss		> 9		dB
Output Power at Saturation ($P_{IN} = 16$ dBm)	40	> 41		dBm
Power-Added Efficiency ($P_{IN} = 16$ dBm)	45	> 52		%
Gain Temperature Coefficient		-0.05		dB/°C
Power Temperature Coefficient		-0.007		dBm/°C

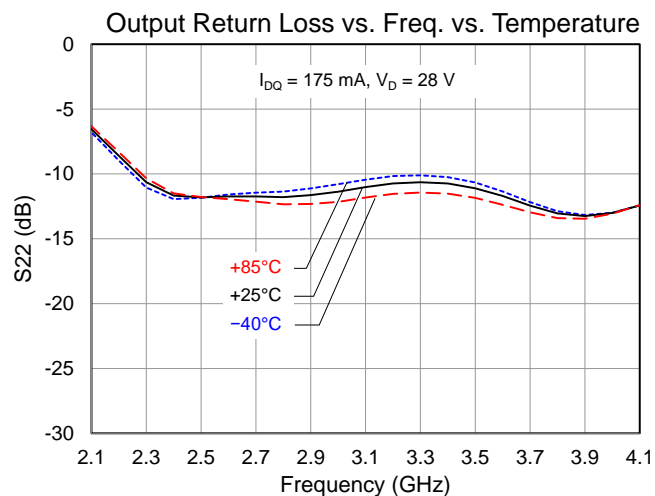
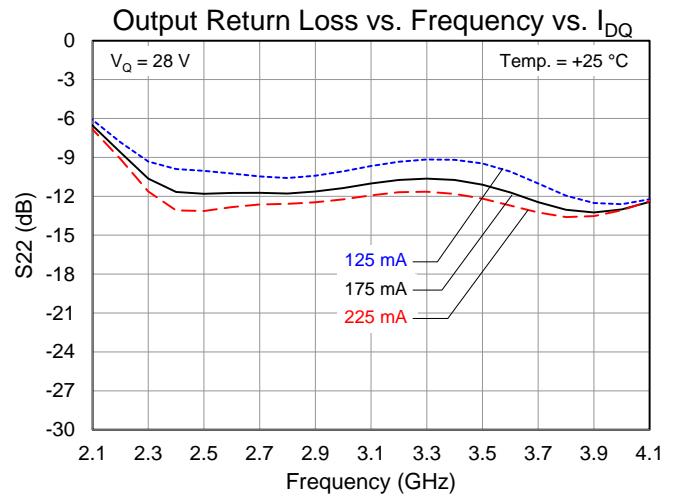
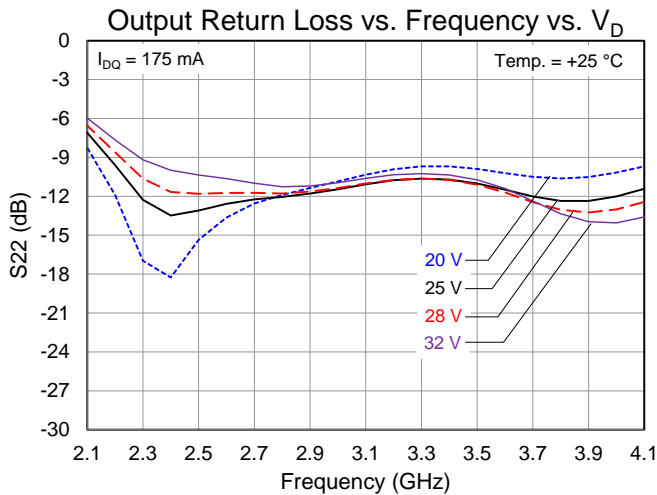
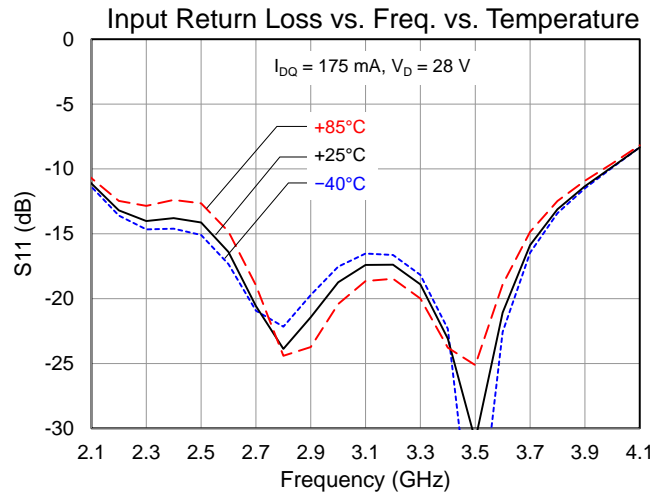
Typical Performance: Small Signal

Condition: CW



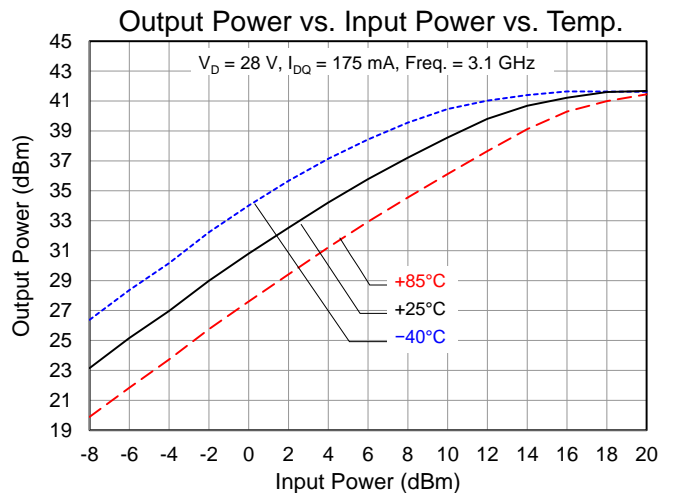
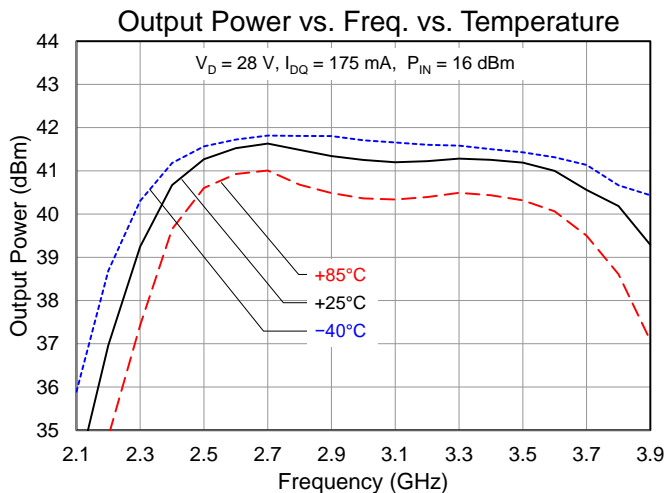
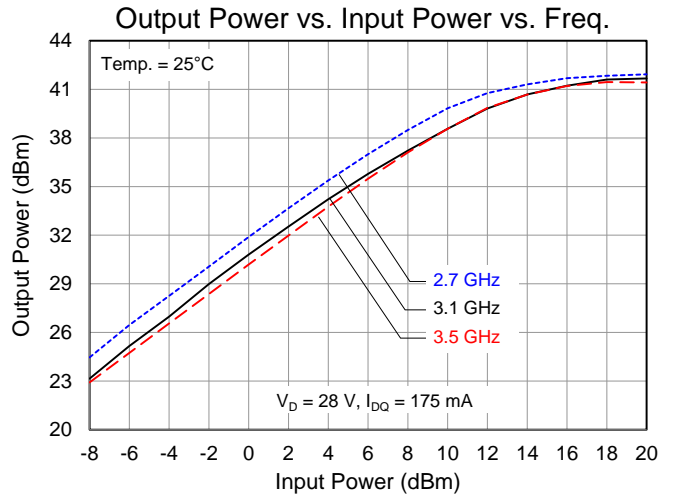
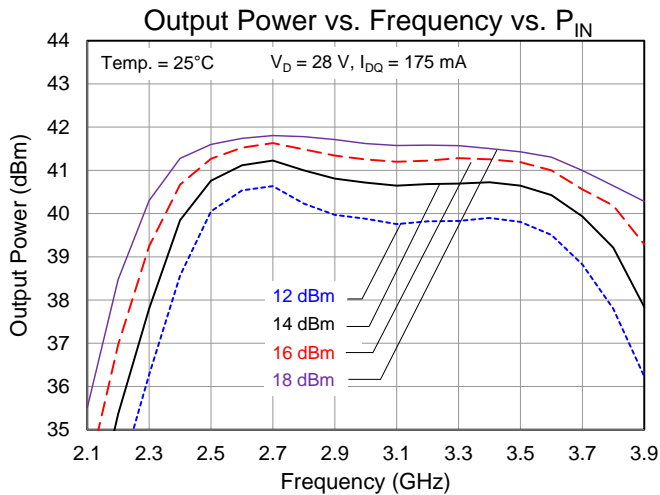
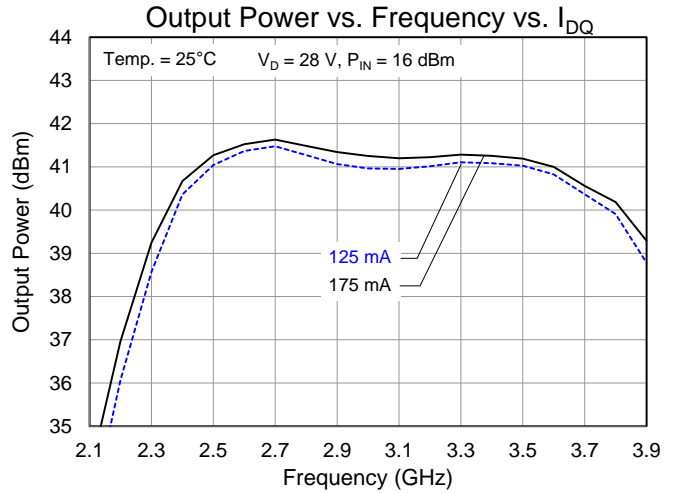
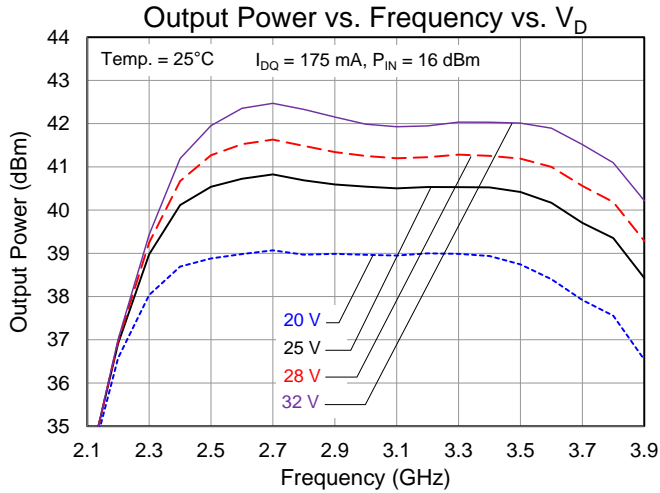
Typical Performance: Small Signal

Condition: CW



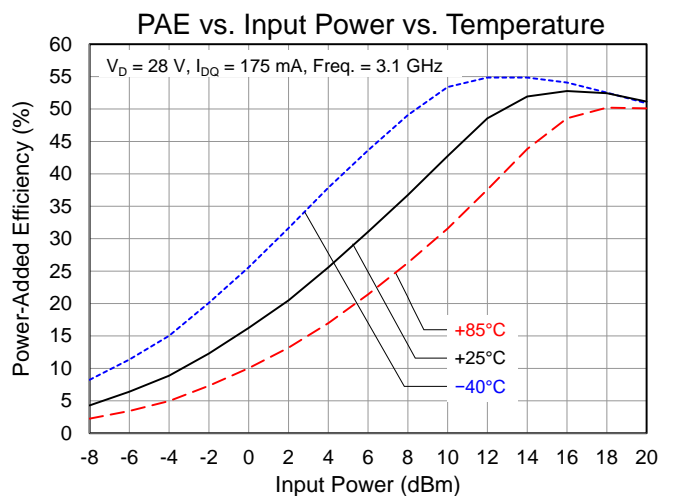
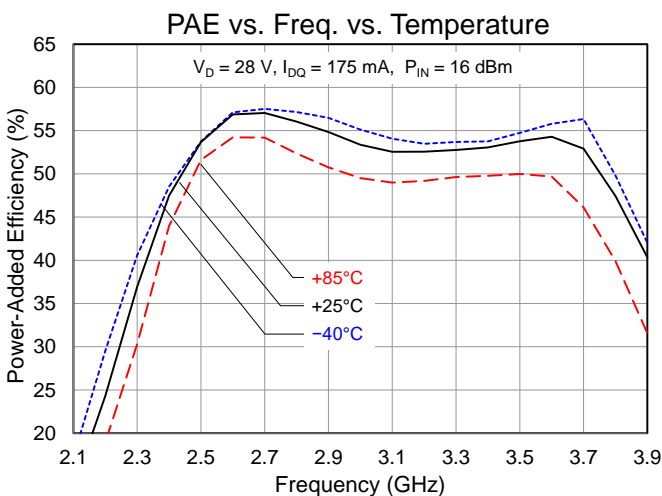
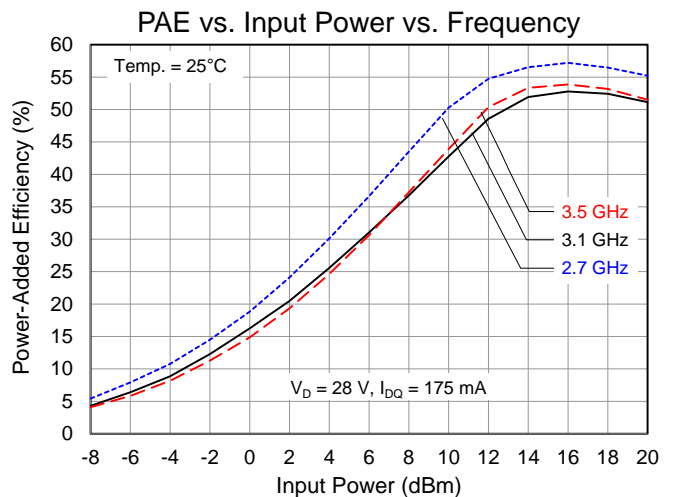
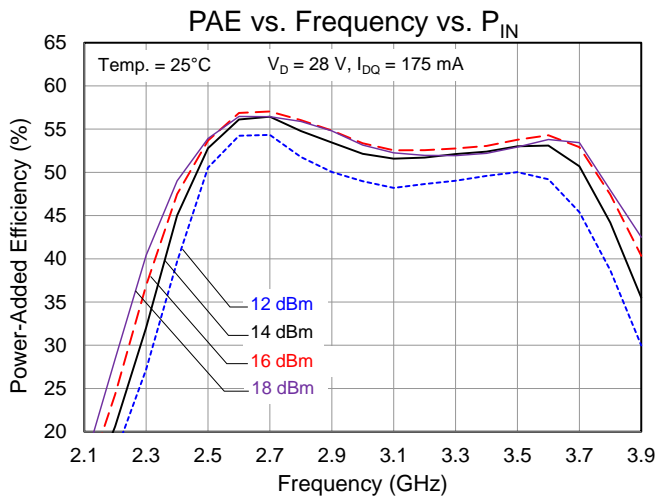
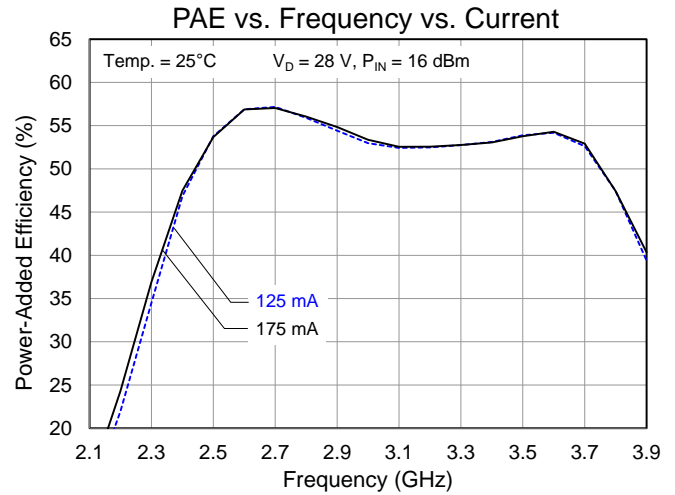
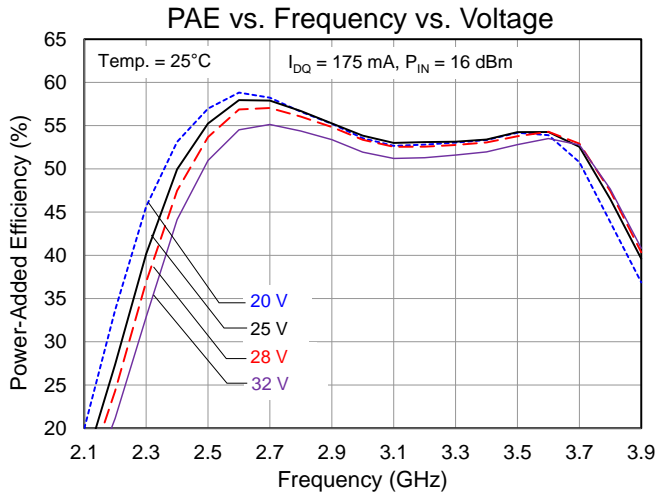
Typical Performance: Large Signal

Condition: Pulsed V_D , Pulse Width = 100 us, Duty Cycle = 10%



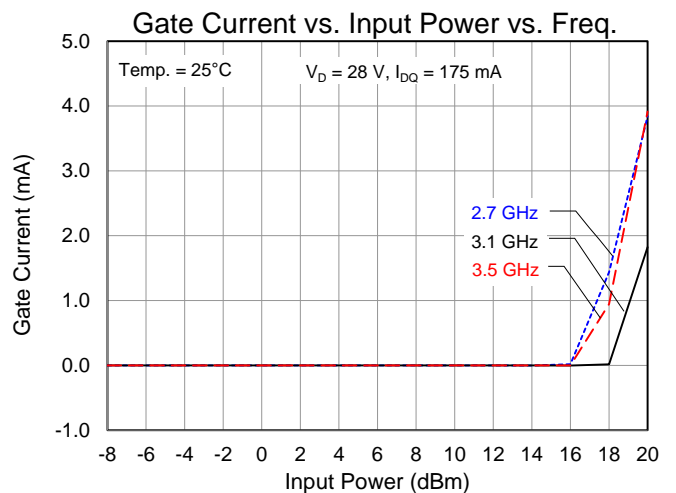
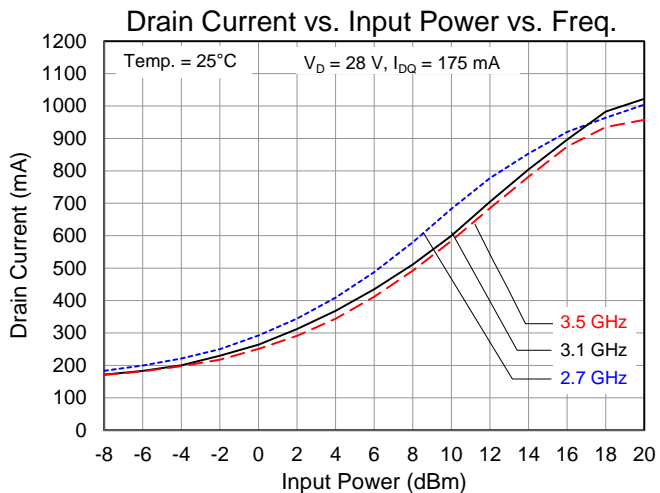
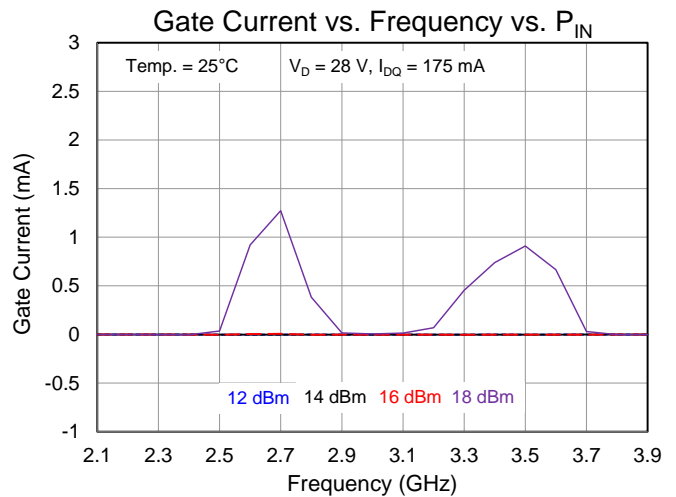
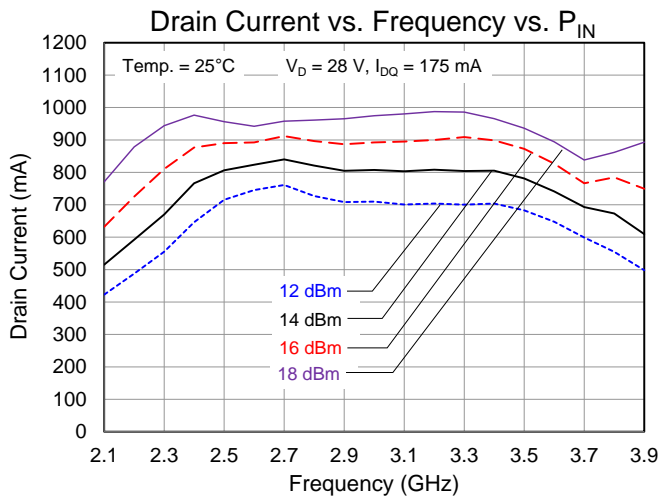
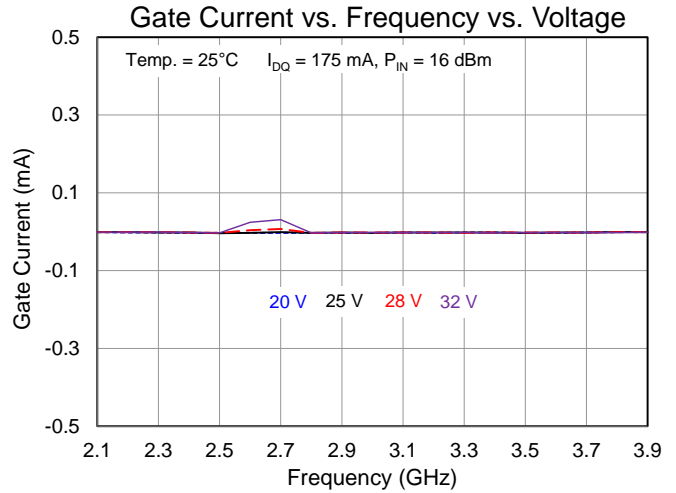
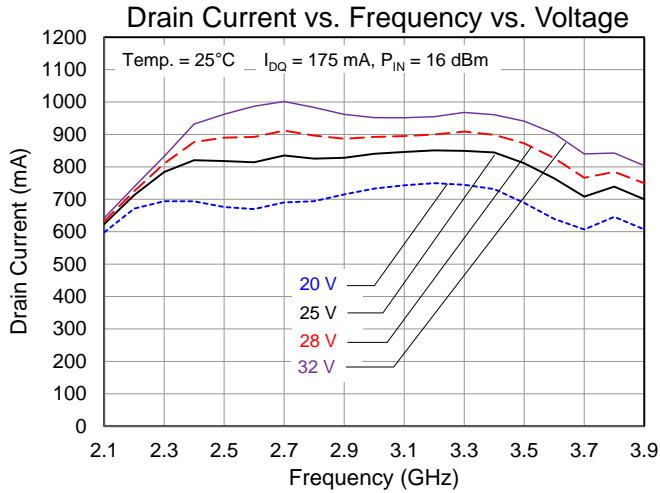
Typical Performance: Large Signal

Condition: Pulsed V_D , Pulse Width = 100 μ s, Duty Cycle = 10%



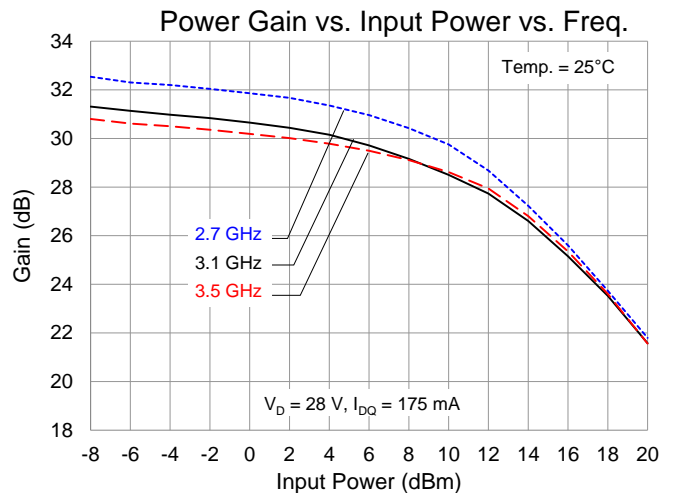
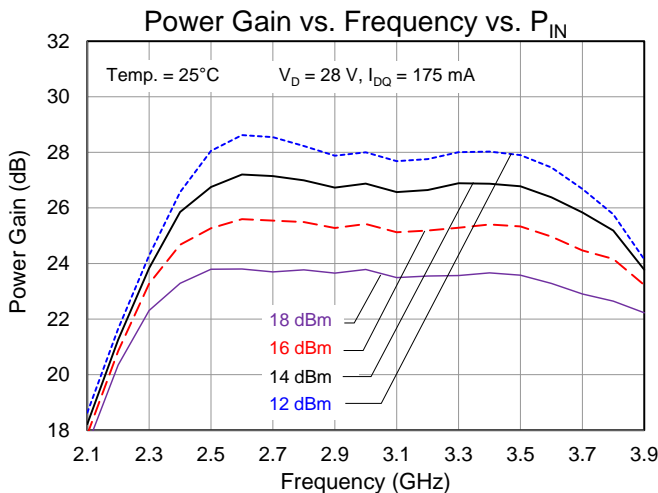
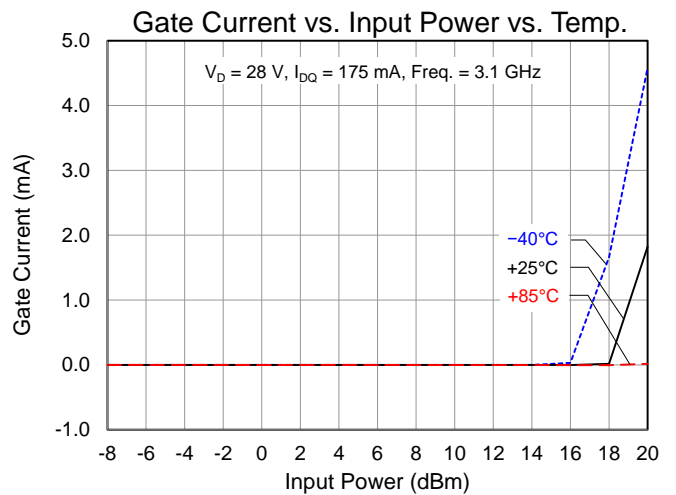
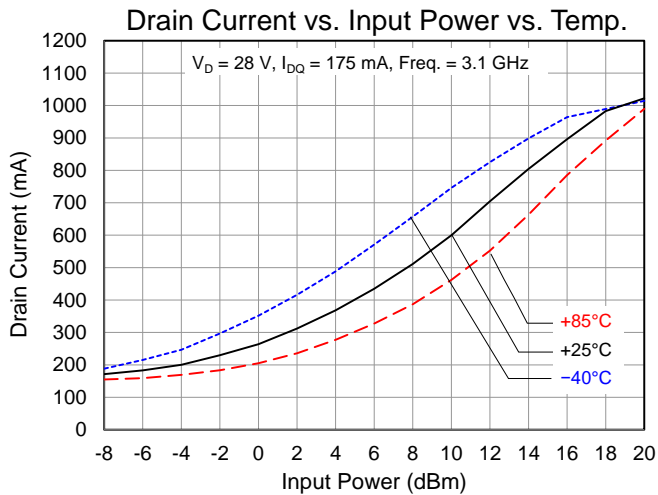
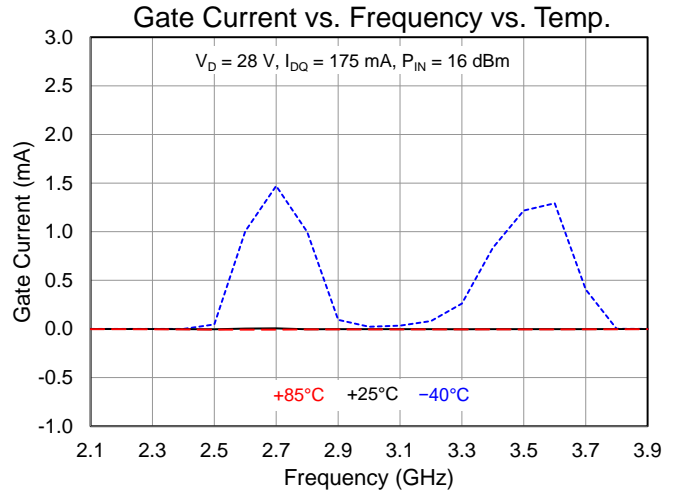
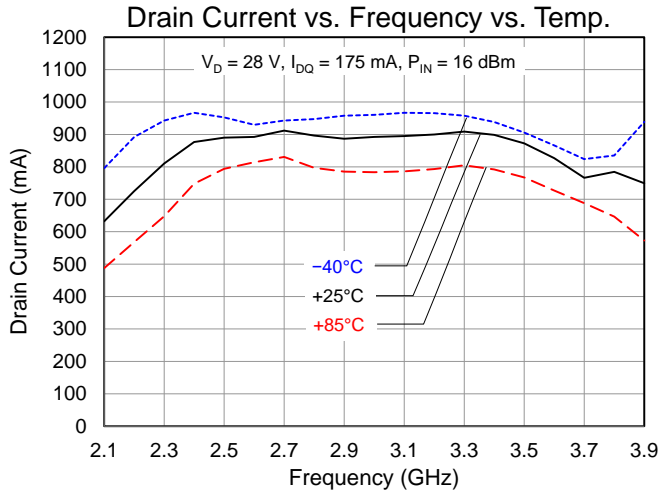
Typical Performance: Large Signal

Condition: Pulsed V_D , Pulse Width = 100 us, Duty Cycle = 10%



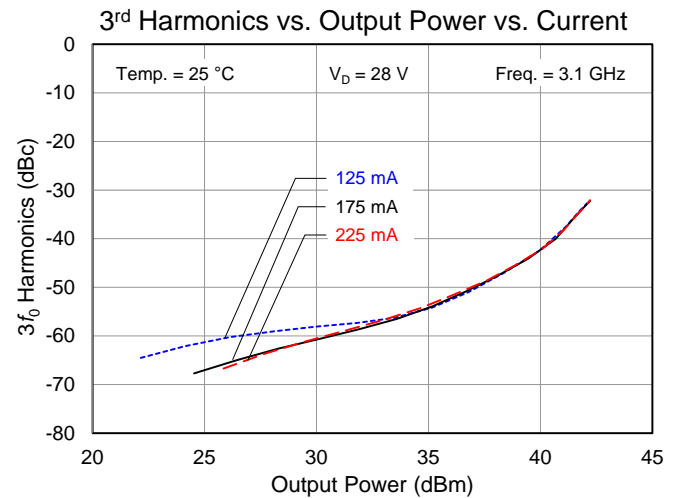
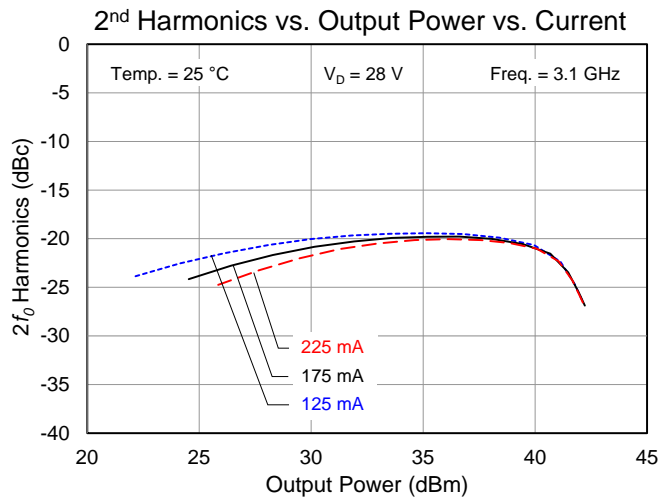
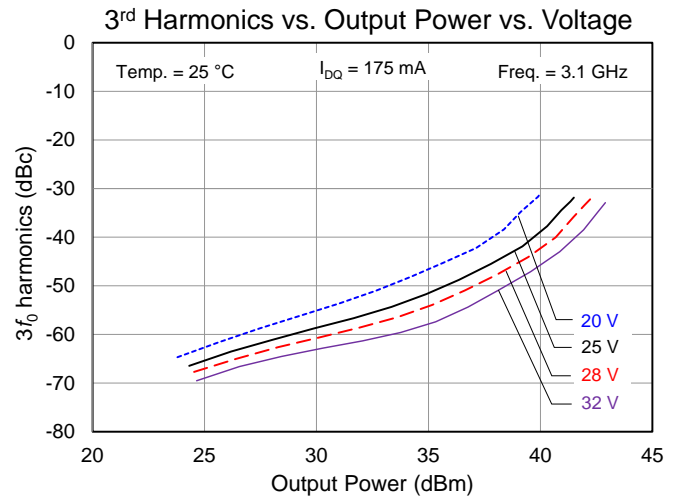
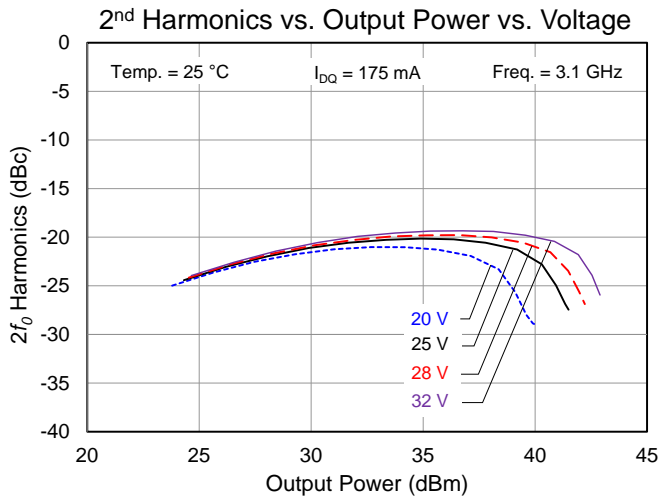
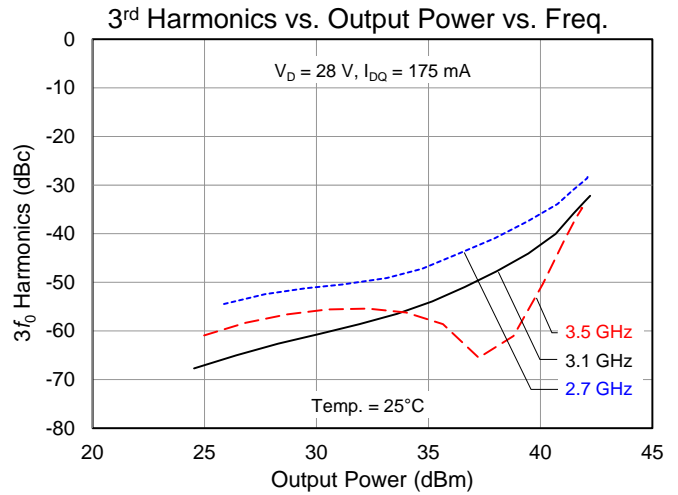
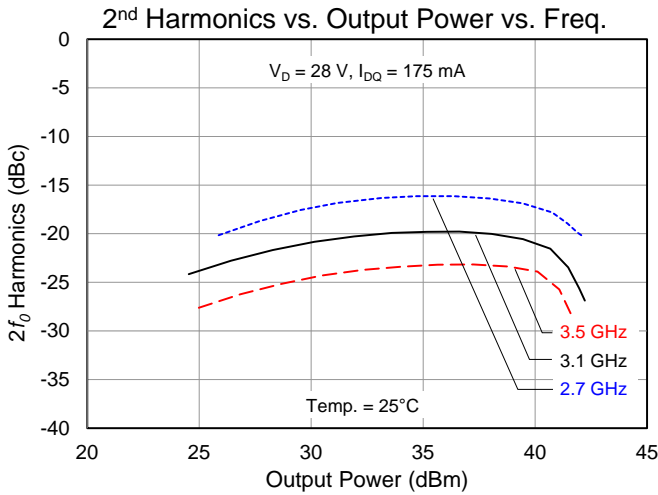
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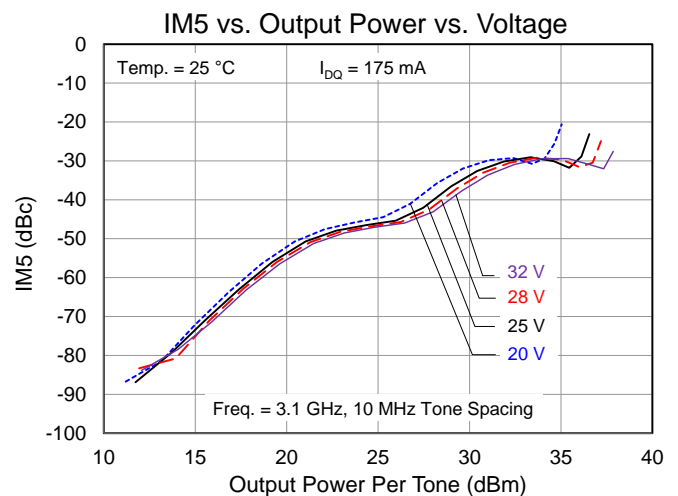
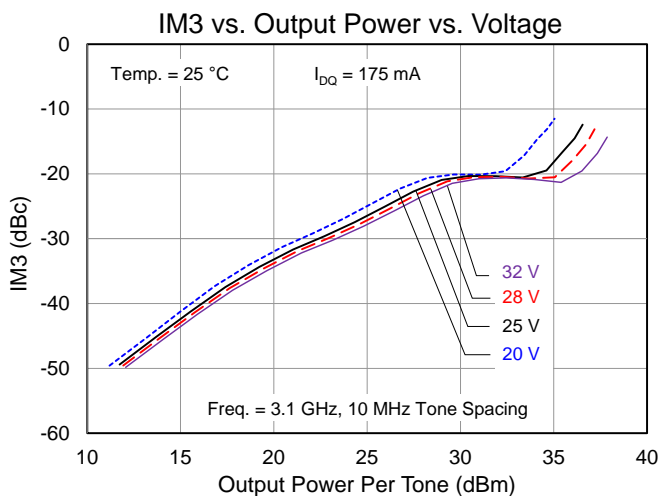
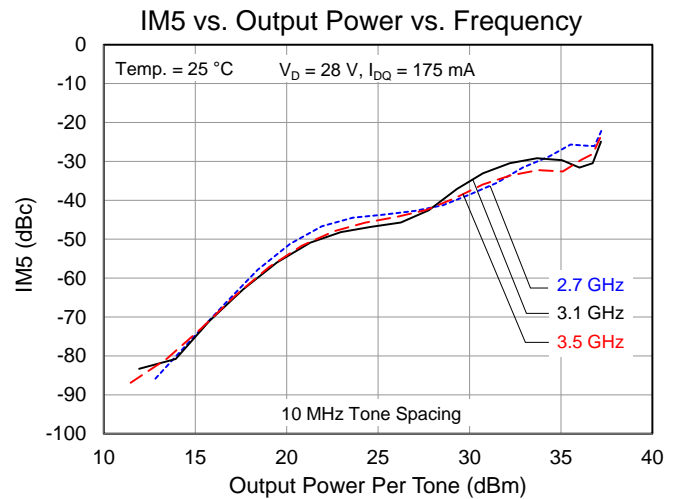
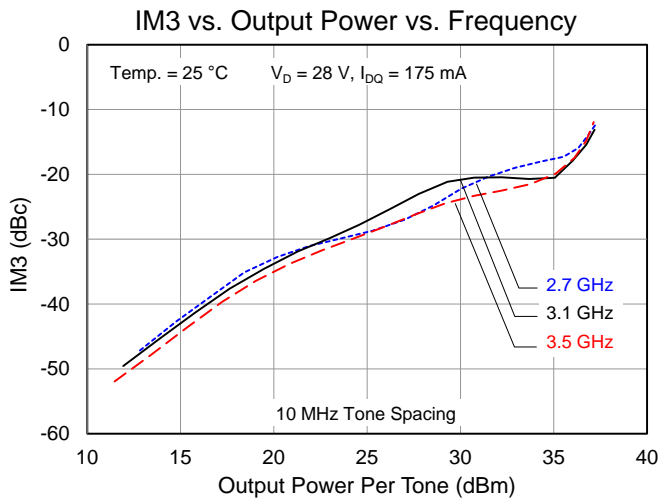
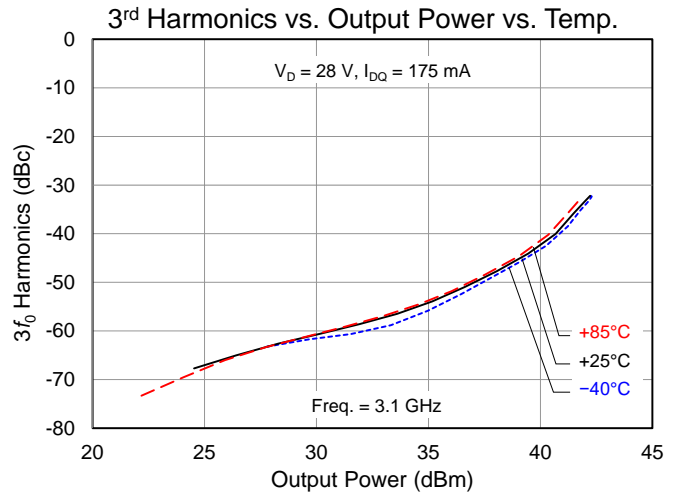
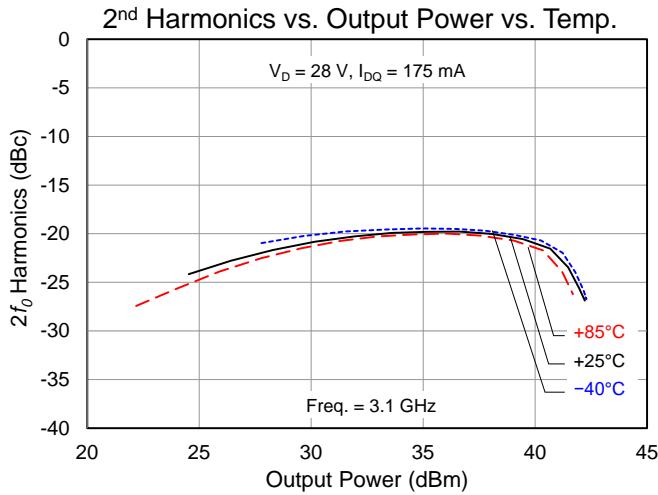
Typical Performance: Large Signal and Linearity

Condition: CW



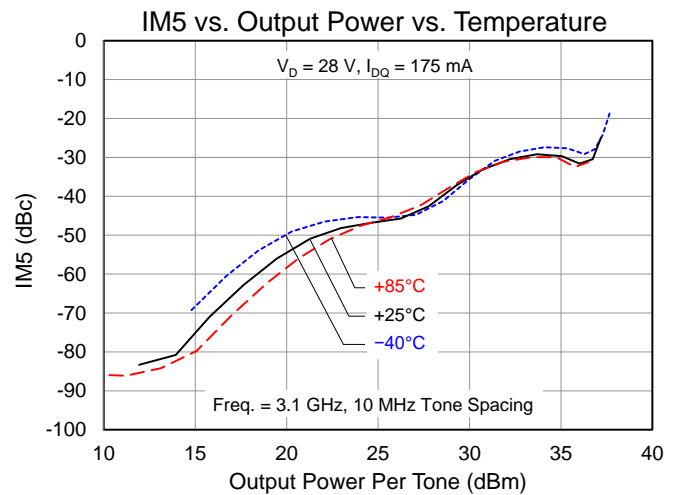
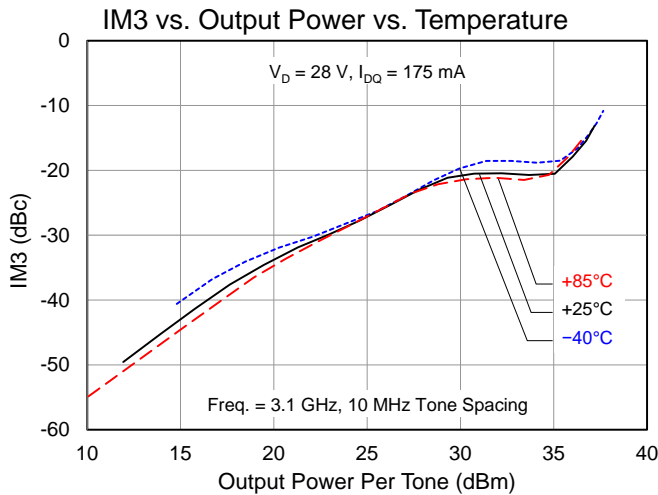
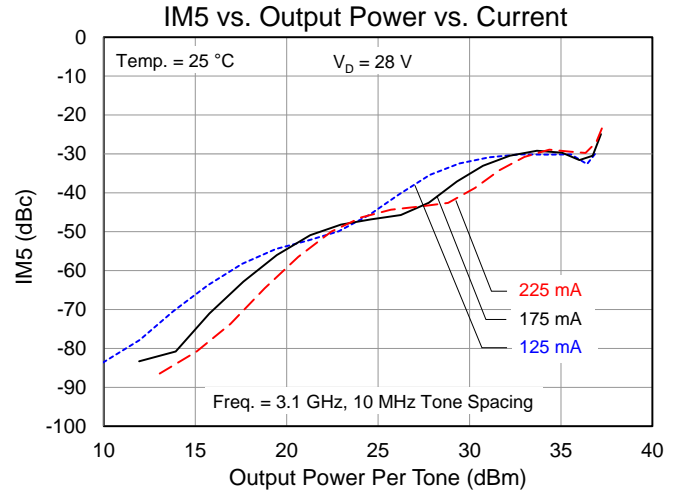
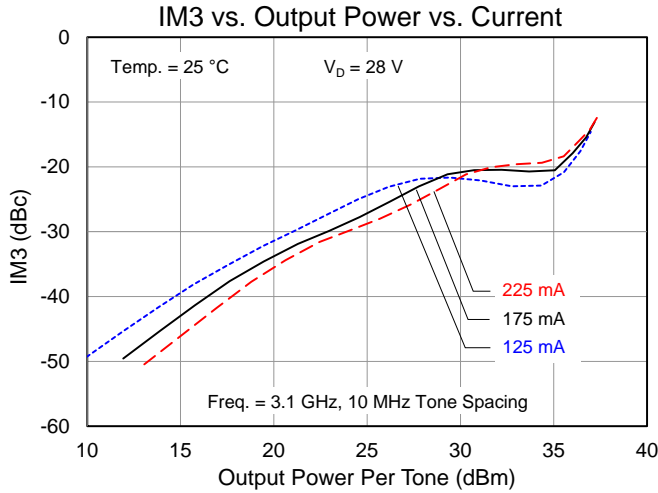
Typical Performance: Large Signal and Linearity

Condition: CW



Typical Performance: Large Signal and Linearity

Condition: CW



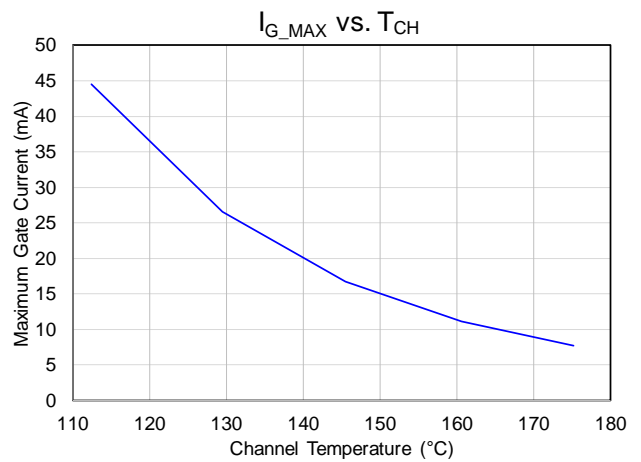
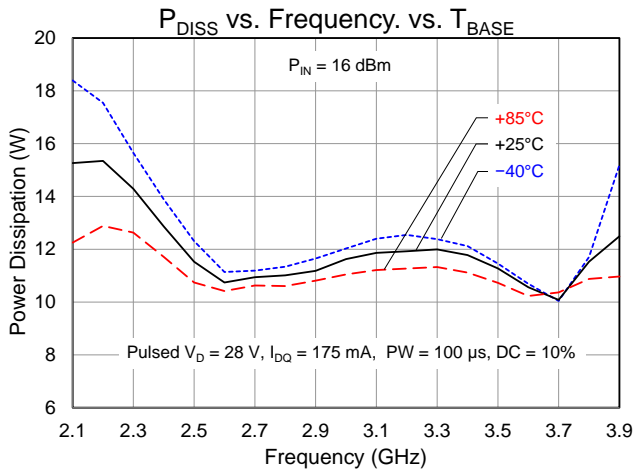
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{DQ} = 175\text{ mA}$, $P_{DISS} = 4.9\text{ W}$ (Quiescent DC, CW)	2.43	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH}) ⁽²⁾		96.9	$^{\circ}\text{C}$
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85\text{ }^{\circ}\text{C}$, $V_D = 28\text{ V}$, $I_{D_Drive} = 805\text{ mA}$, Freq. = 3.3 GHz, $P_{IN} = 16\text{ dBm}$, $P_{OUT} = 40.5\text{ dBm}$, $P_{DISS} = 11.0\text{ W}$ (PW = 100 μs , DC = 10%)	2.16	$^{\circ}\text{C/W}$
Channel Temperature (T_{CH}) ⁽²⁾ (w/RF drive)		108.8	$^{\circ}\text{C}$

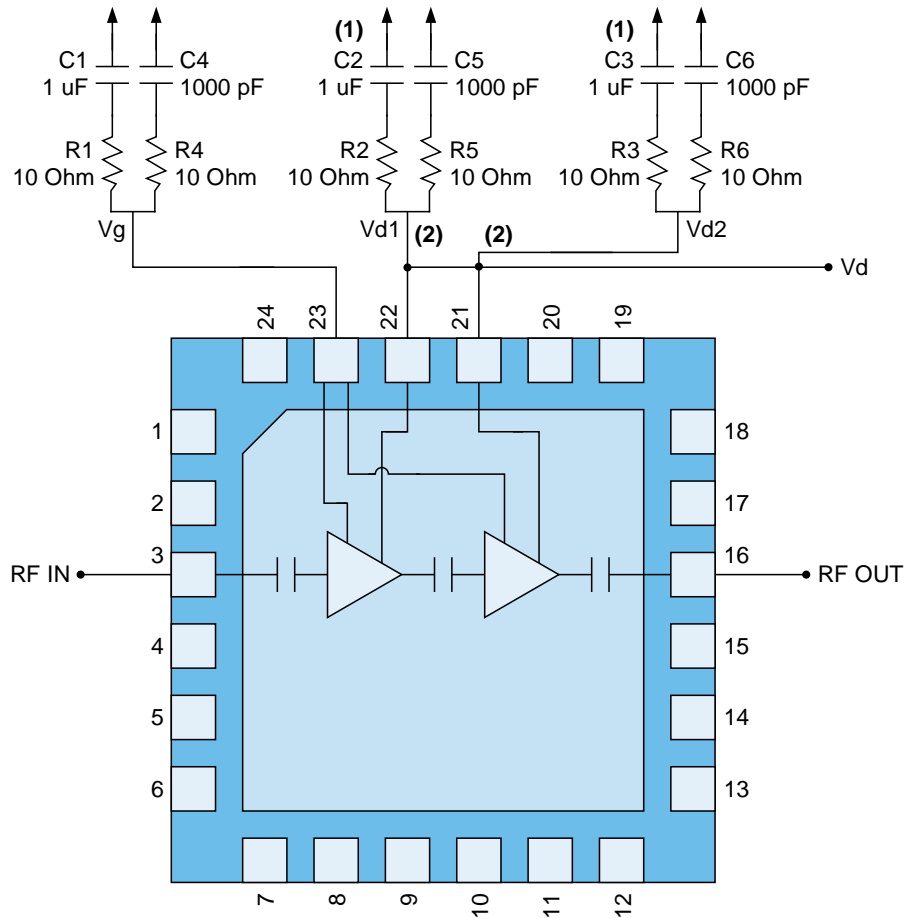
Notes:

1. Thermal resistance determined to the back of package (85 $^{\circ}\text{C}$)
2. IR scan equivalent. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Power Dissipation and Maximum Gate Current



Applications Information



Notes:

1. Remove if pulsing on drain
2. V_D: Tied V_{D1} & V_{D2} together

Bias-up Procedure

Set I_D limit to 1.3 A, I_G limit to 8 mA

Apply -5 V to V_G

Apply +28 V to V_D; ensure I_{DQ} is approx. 0 mA

Adjust V_G until I_{DQ} = 175 mA (V_G ~ -2.7 V Typ.).

Turn off RF signal

Bias-down Procedure

Turn off RF signal

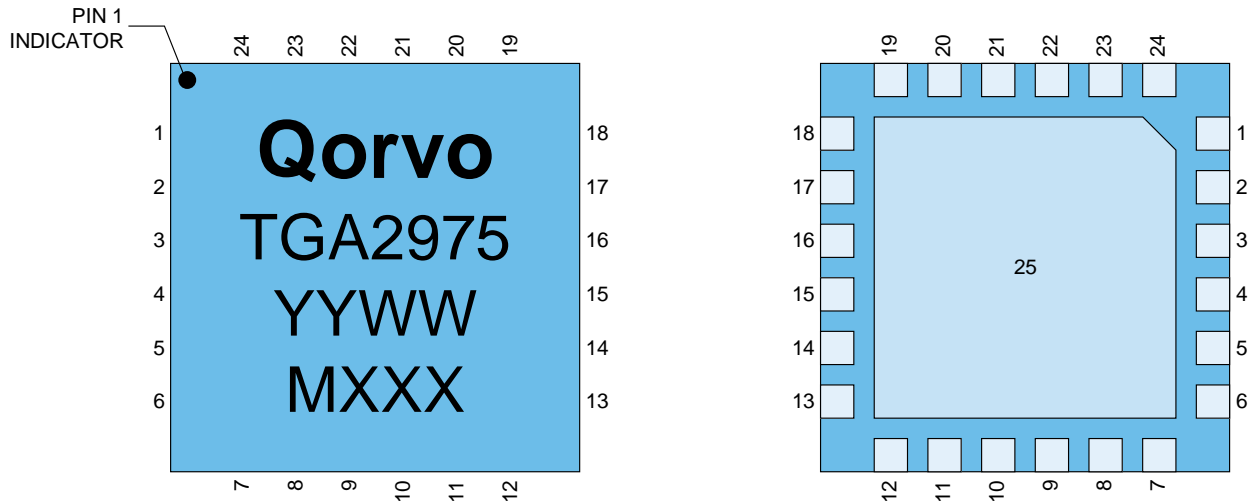
Reduce V_G to -5 V; ensure I_{DQ} is approx. 0 mA

Set V_D to 0 V

Turn off V_D supply

Turn off V_G supply

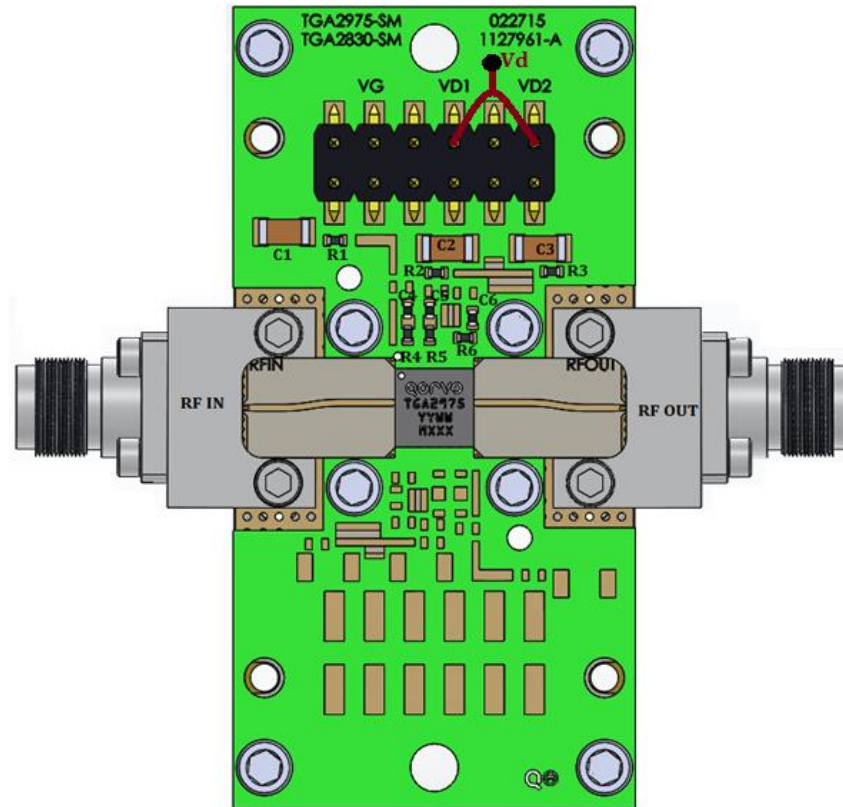
Pin Layout



Pin Description

Pin No.	Symbol	Description
1, 2, 4-15, 17-20, 24	NC	No internal connection; can be grounded on PCB or left open
3	RF _{IN}	Input; matched to 50 Ω; DC blocked
16	RF _{OUT}	Output; matched to 50 Ω; DC blocked
21	DRAIN 2	Drain voltage; bias network is required; see recommended Application Information on page 13
22	DRAIN 1	Drain voltage; bias network is required; see recommended Application Information on page 13
23	GATE	Gate voltage; bias network is required; see recommended Application Information on page 13
25	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

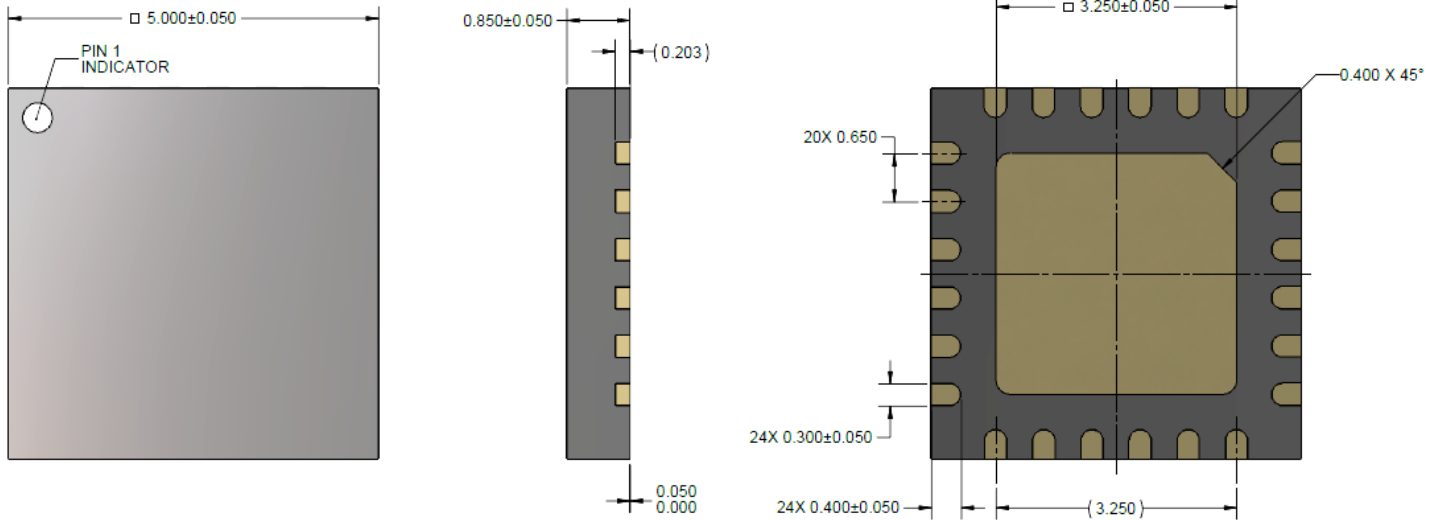
Evaluation Board



Bill of Material

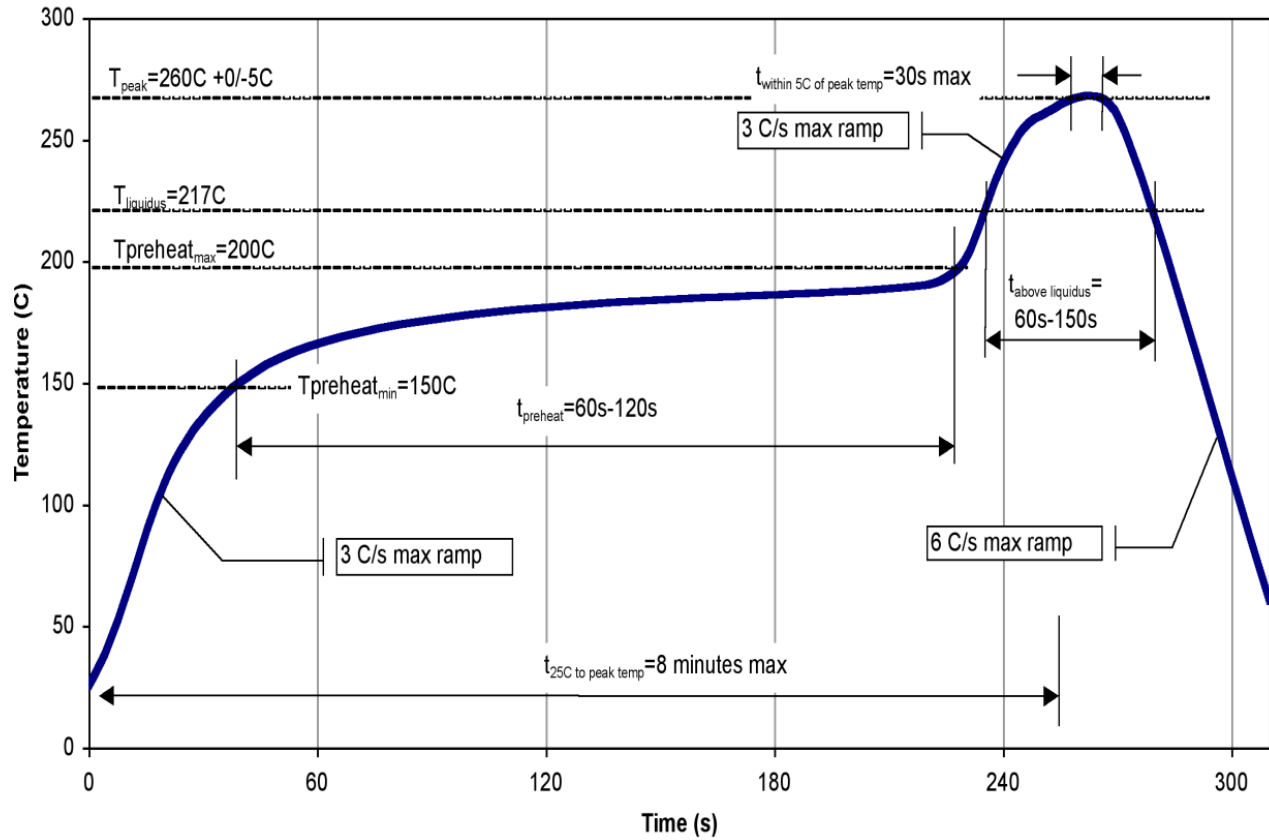
Reference Design	Value	Description	Manufacture	Part Number
C1–C3	1 μ F	Cap, 1206, 50 V, 5%, X7R	Various	
C4–C6	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
R1–R6	10 Ω	Res, 0402, 5%	Various	

Mechanical Information



Units: millimeter (mm)
 Tolerances: unless specified
 x.xx = ± 0.01
 x.xxx = ± 0.005
 Materials:
 Package Leads are Ni-Pd-Au
 Part is Mold Encapsulated.
 Marking:
 2975: Part number
 YY: Part Assembly year
 WW: Part Assembly week
 MXXX: Batch ID

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD-Human Body Model (HBM)	1B	ANSI/ESDA/JEDEC JS-001
ESD-Charge Device Model (CDM)	C3	JESD22-C101
MSL-Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020 Lead-free solder, 260 °C.

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations.

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Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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