Clock generator for digital still camera

BU2382FV

BU2382FV is a high-performance 2-channel PLL IC. PLL circuit generates necessary clocks by inputting standard clocks of crystal oscillator from outside. Changing a connection of wire can generate any clocks required for any applications of users. Jitter and S/N characteristic has achieved almost the same high-quality sound and vision as oscillating module because of optimization of PLL. Frequency can be changed by the internal dividing control.

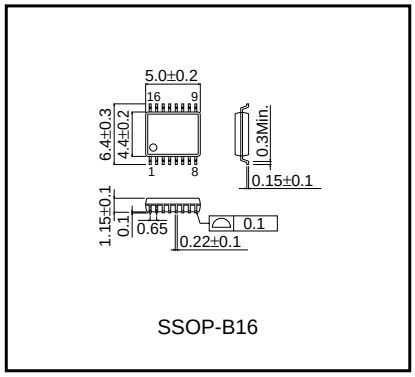
●Applications

Digital still camera

●Features

1) Generate clocks for CDS, USB with standard clock input
2) No external elements required
3) Standard clocks apply to two kinds of NTSC/PAL
4) Power down control in each 2-channel PLL
5) Single power supply of 3.3V operating
6) SSOP-B16 small package

●External dimensions (Unit : mm)



SSOP-B16

●Absolute maximum ratings (Ta=25°C)

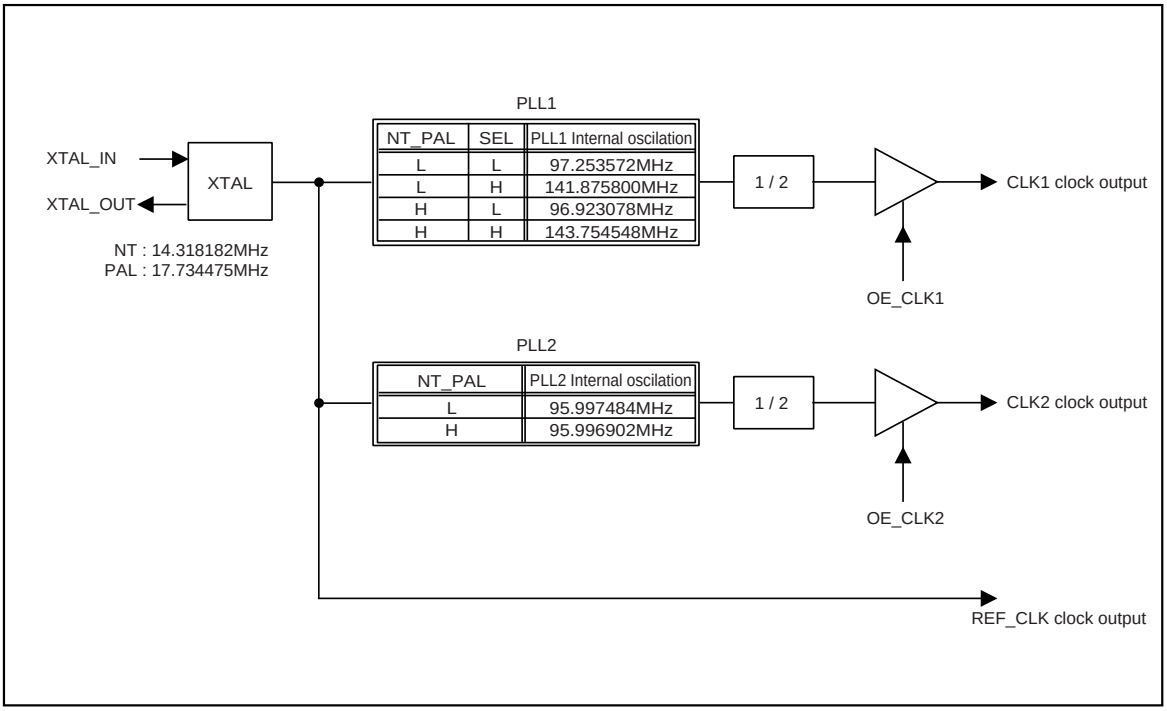
Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{DD}+0.5	V
Storage temperature range	Tstg	–30 to +125	°C
Power dissipation	Pd	450	mW

∗IC destruction is not occurred, however, operation can not be guaranteed.
∗Derating : 4.5mW/°C for operation above Ta=25°C.
∗This product is not designed for protection against radioactive rays.
∗Power dissipation is the rate when the IC is mounted on the board.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	–	3.6	V
Input "H" voltage range	VIH	0.8V_{DD}	–	V_{DD}	V
Input "L" voltage range	VIL	0	–	0.2V_{DD}	V
Operating temperature	Topr	–5	–	+70	°C
Output load	CL	–	–	15	pF

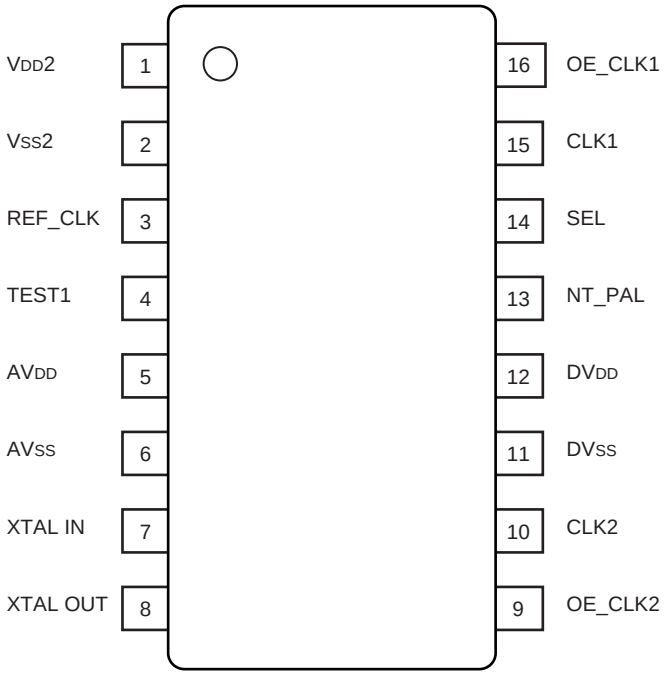
●**Block diagram**



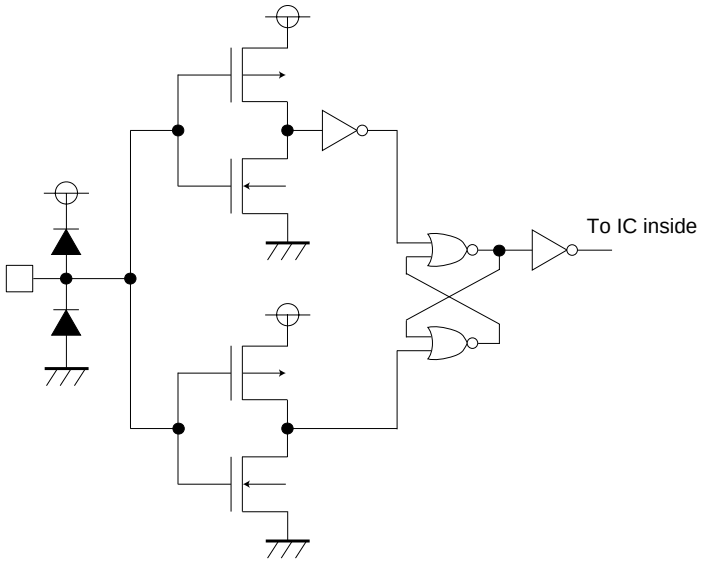
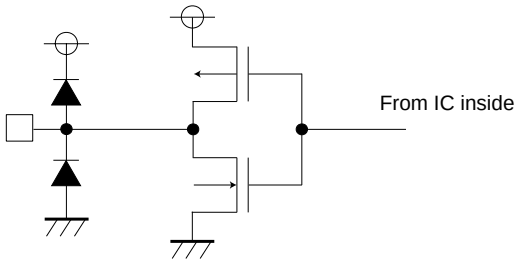
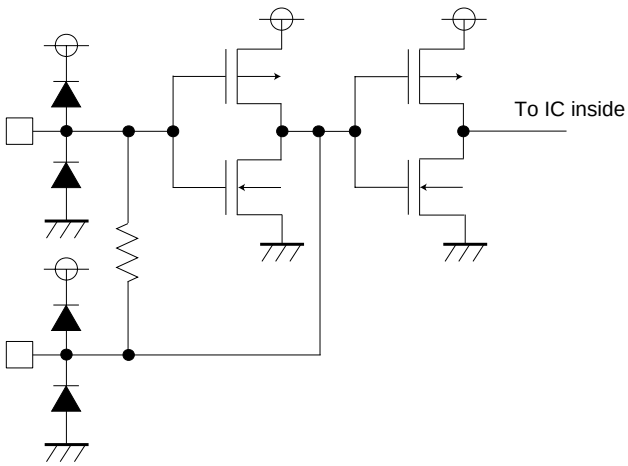
NT_PAL	SEL	REF–CLK (MHz)	CLK1 (MHz)	CLK2 (MHz)
L	L	17.734475	48.626786 XTAL ∗ (170 / 31) /2	47.998742 XTAL ∗ (249 / 46) /2
L	H	17.734475	70.937900 XTAL ∗ (360 / 45) /2	47.998742 XTAL ∗ (249 / 46) /2
H	L	14.318182	48.461539 XTAL ∗ (176 / 26) /2	47.998451 XTAL ∗ (295 / 44) /2
H	H	14.318182	71.877274 XTAL ∗ (502 / 50) /2	47.998451 XTAL ∗ (295 / 44) /2

●**Pin descriptions**

Pin No.	Pin name	Functions
1	$V_{DD}2$	V_{DD} for clock output
2	$V_{SS}2$	GND for clock output
3	REF_CLK	Crystal output
4	TEST1	Test mode control pin
5	AV_{DD}	Analog V_{DD}
6	AV_{SS}	Analog GND
7	$XTAL_{IN}$	Standard crystal input
8	$XTAL_{OUT}$	Standard crystal output
9	OE_CLK2	Output enable pin for CLK2 (H : enable, L : output L fixed)
10	CLK2	CLK2 clock output
11	DV_{SS}	Digital GND
12	DV_{DD}	Digital V_{DD}
13	NT_PAL	NT / PAL select (L : PAL, H : NTSC)
14	SEL	Output select
15	CLK1	CLK1 clock outpt
16	OE_CLK1	Output enable pin for CLK1 (H : enable, L :output Lfixed)



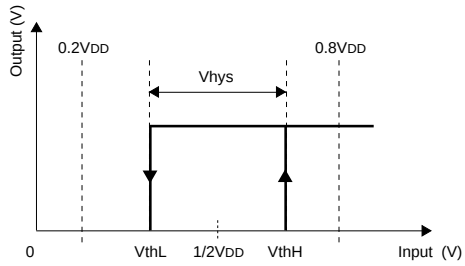
●**Input output circuits**

Pin No.	Equivalent circuit
Input PIN (Schmidt trigger) 9, 13, 14, 16 (With pull_up) 4 (With pull_down)	
Output PIN 3, 10, 15	
Crystal PIN 7, 8	

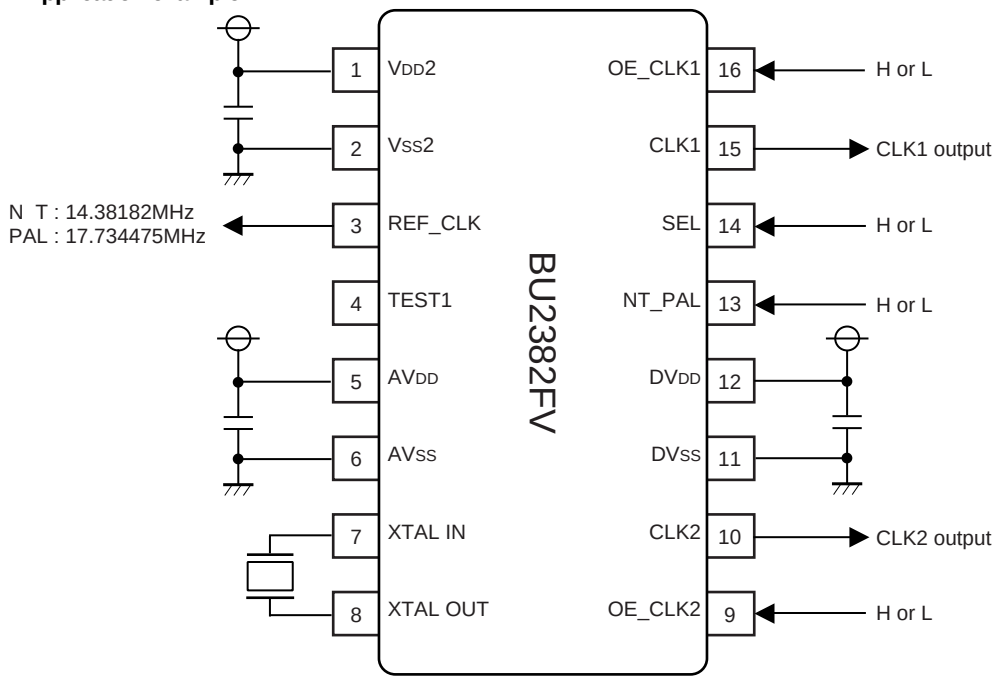
●**Electrical characteristics** (Unless specified otherwise Ta=25°C, VCC=3.3V, crystal frequency=14.318182MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output H voltage	VOH	2.4	–	–	V	IOH=4.0mA
Output L voltage	VOL	–	–	0.4	V	IOL=4.0mA
Input VthL ∗3	VthL	0.2VDD	–	–	V	∗1
Input VthH ∗3	VthH	–	–	0.8VDD	V	∗1
Hysteresis width ∗3	Vhys	–	0.4	–	V	Vhys=VthH-VthL
Operating circuit current	IDD	–	30	45	mA	No load
CLK1	CLK1_LL CLK1_LH CLK1_HL CLK1_HH	–	48.626786 70.937900 48.461539 71.877274	–	MHz	XTAL ∗170/31/2 (XTAL=17.734475MHz) XTAL ∗360/45/2 (XTAL=17.734475MHz) XTAL ∗176/26/2 (XTAL=14.318182MHz) XTAL ∗502/50/2 (XTAL=14.318182MHz)
CLK2	CLK2_L CLK2_H	–	47.998742 47.998451	–	MHz	XTAL ∗249/46/2 (XTAL=17.734475MHz) XTAL ∗295/44/2 (XTAL=14.318182MHz)
Duty	Duty	45	50	55	%	1/2 VDD test
Jitter 1σ	JsSD	–	30	–	psec	1σ short time jitter
Jitter MIN-MAX	JsABS	–	180	–	psec	MIN.-MAX.
Rise time	tr	–	2.5	–	nsec	20% to 80% time of VDD
Fall time	tf	–	2.5	–	nsec	20% to 80% time of VDD
Output Lock time	tlock	–	–	1	msec	∗2

Note) Output frequency is determined by the operation expression (Frequency divide) input to XTAL IN.
Output at 27MHz input is shown above.
Jitter is value when using Time interval analyzer with 10000 sampling.
∗1) Low and high limit voltage in the schmitt trigger input Pin having hysteresis features shown in ∗3 diagram.
∗2) Time that output takes to stabilize in the specific frequency range after the power supply reaches to 3.0V.
∗3) Make reference to the diagram.



●**Application example**



Note) The BU2382FV is basically placed on the board.
Decoupling capacitance (0.1μF) need to be placed between Pin1 ($V_{DD}2$) and Pin2 ($V_{SS}2$), Pin5 (AV_{DD}) and Pin6 (AV_{SS}), Pin11 (DV_{SS}) and Pin12 (DV_{DD}).
To obtain accurate frequency, capacitance (pF) need to be placed between Pin8 (XTAL IN) and Pin6 (AV_{SS}). Pin7 (XTAL OUT) and Pin6 (AV_{SS}).
Tantalum capacitance (10 to 100μF), ferrite beads may need to be placed to prevent power supply drop in certain board's case.
To reduce high frequency noise, selected bypass capacitors (<1Ω at problem high frequency) maybe used for power pin as close to BU2382FV as possible.

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