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TECHNICAL DATA

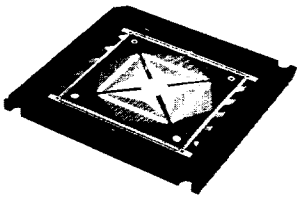
MCA10000ECL

MCA10000ECL MACROCELL ARRAY

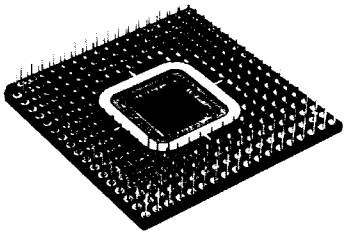
MCA3 ECL SERIES
MACROCELL ARRAY

The MCA10000ECL Array is a member of Motorola's "Third-Generation" MCA3 ECL series. Motorola's MOSAIC III process provides the MCA10000ECL with the logic power of over 10,000 equivalent 120 picosecond (typical) gates on one integrated circuit chip. This advanced process technology, combined with innovative gate array design, gives the array the performance and flexibility to meet today's high-performance system needs.

- Logic Function Fully Specified by User
- Metal Mask Programmable (Three Unique Masks)
- Over 10000 Equivalent Logic Gates
- Internal Gate Delays — 120 ps Typical
- Input Cell Delays — 120 ps Typical
- Output Cell Delays — 300 ps Typical
- Flexible I/O Structure with up to 256 Signal Lines
- Supported By Complete CAD Development System
- Interfaces with MECL 10KH or ECL 100K Logic Families
- Programmable Speed/Power Levels
- Series-Terminated ECL Outputs for Multichip Applications
- Three-Level Series Gated Macros
- MCA2 and MCA3 ECL Series Library Compatibility
- High Performance Packages including 289 TAB PGA with Optional Pin-Fin Heatsink, 235 PGA and 360 Lead TAB Tape

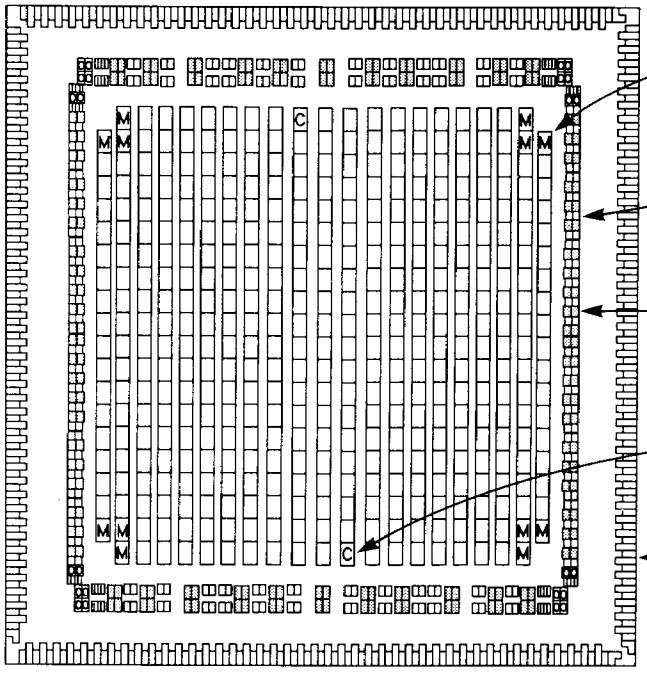


360 Lead TAB



235 PGA (Pin Grid Array) Package

FIGURE 1 — MACROCELL ARRAY LAYOUT



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Rev. 2
(Replaces ADI1390R1)

TABLE 1 — BASIC MCA10000ECL ARRAY FEATURES

1. Array contains 1656 internal quarter cells, 200 output driver (O) cells, 224 input interface (I) cells, 256 I/O ports.
2. Compatible with MECL 10KH and ECL 100K input/output logic levels.
3. Up to 12,402 equivalent gates if full adders, output latches, and input OR's are used.
4. Up to 11,160 equivalent gates if D flip-flops, output latches, and input OR's are used.
5. Die size: 385 x 385 mils.
6. Speed/power programmable from 8–15 Watts Low Power Array (LPA) and 12–30 Watts High Power Array (HPA).
7. From 0.8 to 3.0 mW/gate (using 10000 gates and 8.0–30 Watts).
8. Current source pulldowns on internal macrocell outputs to V_{EE2} (−3.4 Vdc nominal).
9. Input cell delays: 150 ps (HPA), 300 ps (LPA) worst case.
10. Internal cell delays: 175 ps (HPA), 300 ps (LPA) worst case (2-input OR, FO = 1, metal = 0).
11. Output cell delays: approx. 600 ps worst case (includes 250 ps package pin delay).
12. Standard 50 and 25 ohm ECL output drivers. Optional low-power 68 ohm drivers.
13. Series-terminated (STECL) outputs with on-chip series resistors and programmable current sinks.
14. Expandable MUX/DECODE macro functions.
15. High-performance 289 PGA package with controlled impedance.
16. Two on-chip clock pulse generators/buffers.
17. Three-level series gated macros available for increased functional density and performance.

PRODUCT DESCRIPTION

Motorola's "Third Generation" — MCA3 ECL series is a two part family which includes the MCA10000ECL and the MCA2200ECL. This data sheet features the MCA10000ECL array. The MCA10000ECL Macrocell Array contains the equivalent of over 10000 gates, each with a typical delay of 120 ps with one load and no metal. The array is fabricated using Motorola's MOSAIC III process which features poly-electrode-transistors (see Figure 2).

The array is fully compatible with the two prevailing industry ECL standards: MECL 10KH and ECL 100K. The ECL 100K compatible version features temperature compensation over a junction temperature range of 25 to 115 degrees Centigrade. Both 10KH and 100K versions of the MCA10000ECL are specified for use with a V_{EE1} of either −4.5 Vdc or −5.2 Vdc (nominal).

The array contains four types of cells in which macrocell functions can be placed: internal (M) cells, input (I) cells, output (O) cells, and clock (C) cells. The MCA3 ECL Series Design Manual includes an extensive, common Macrocell Library for the MCA10000ECL and MCA2200ECL arrays. The Macrocell Library listing illustrates all the logic functions (macros) which can be implemented in these cells and provides critical design information such as propagation delays and power requirements for each macro. The MCA3 library supports all of the macro functions from Motorola's MCA2500ECL library as well as numerous additional functions optimized around the MCA3 cell architecture. With few exceptions, all marcos in the MCA3 library can be implemented in either the MCA10000ECL or MCA2200ECL array configuration. However, the MCA2200ECL array is offered only in the high power version.

The MCA10000ECL contains 414 M-cells, 224 I-cells, 200 O-cells, and 2 C-cells as shown in Figure 1. The MCA10000ECL is available in either a high or low power version and macrocells on both versions are speed/power programmable.

The majority of the designer's circuit is implemented using the internal (M) cells. The internal cells contain a wide variety of SSI/MSI functions ranging from combinational logic to all forms of latches and flip-flops. An internal quarter cell can contain functions as large as a D flip-flop (the L892 is a dual D flip-flop in a half cell). Logic may also be implemented in the input and output cells. (See Figure 3.)

The output cells contain functions such as a 4-input OR/NOR (LX02) or a D latch (LX92). The array supports standard ECL 50 and 68 ohm outputs, 25 ohm cutoff drivers, and 50 ohm cutoff drivers. The designer, however, may use an external load of 60 ohms with a slight loss in V_{OH} noise margin. In addition, the designer may select series-terminated (STECL) outputs or inputs with current-source pulldowns for multichip applications.

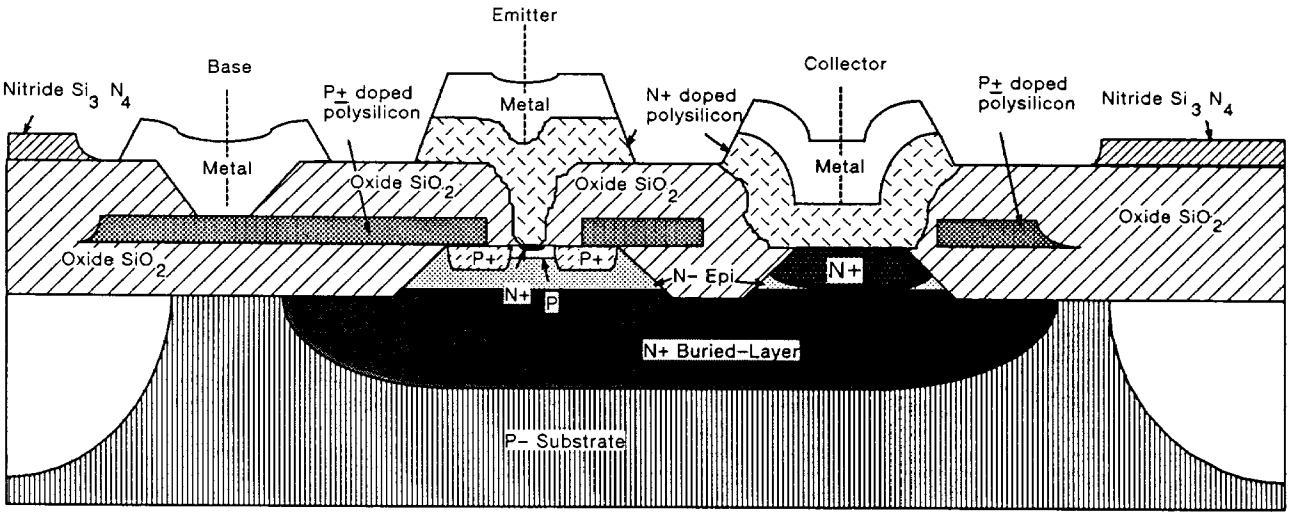
Input (I) macrocells are used for interfacing with external ECL 100K levels (optional for 10KH) or for buffering signals driving lower-level inputs on the array.

The MCA10000ECL array uses three layers of metal for routing: two layers for internal macro implementation and inter-macro routing, and a third layer for power and ground bussing. Both macro interconnection routing and power and ground distribution are invisible to the user. Vertical (metal-1) channels are located between the columns of cell sites. Horizontal (metal-2) channels may be routed over the macrocell locations. The placement of a macro will not obstruct metal-2 routing. The three metal layers are separated by a layer of dielectric isolation and are connected using "VIA's."

Macros such as adders, multiplexers, decoders, latches, flip-flops, XORs, AND-ORs, etc. are built using first layer metal within a cell. (Horizontal metal-2 routing channels are not required.) This eliminates the majority of interconnects that normally have to be made in the channels of a gate array and significantly reduces routing channel requirements. The MCA10000ECL contains a number of free routing channels which is generally sufficient to provide for auto-routability even in a fully utilized array.

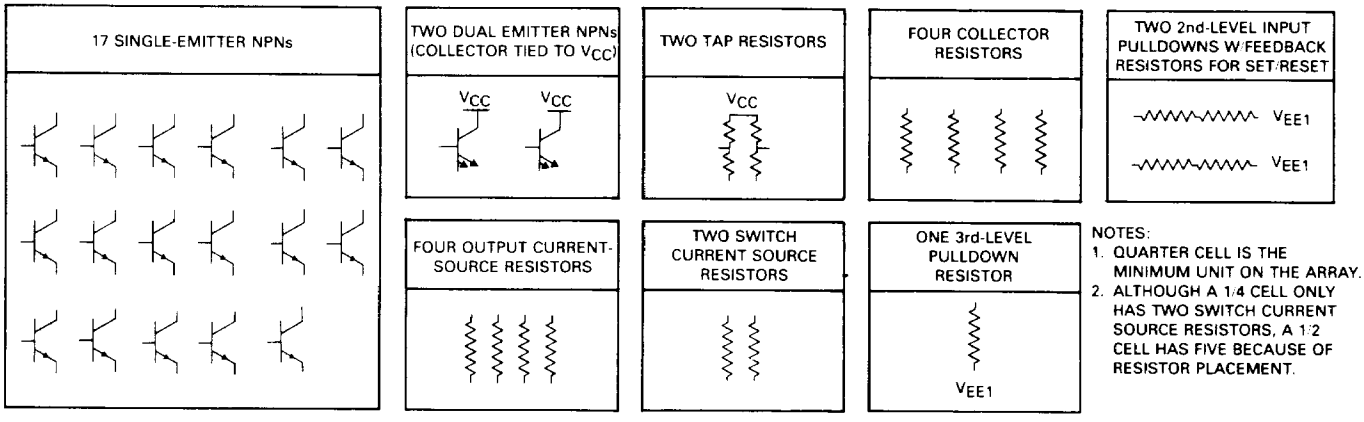
The chip uses ECL circuitry for the internal array and for the I/O. Single-level, two-level, and three-level series-gated ECL structures are used to implement logic functions. Series-gating allows complex macro functions to be implemented with fewer transistors while maintaining maximum performance.

FIGURE 2 — CROSS SECTION OF MOSAIC III PROCESS



MOSAIC III (Motorola Oxide-isolated Self Aligned Implanted Circuit) — Patents Pending

FIGURE 3 — INTERNAL CELL ARCHITECTURE (1/4 MAJOR (M) CELL)



PROCESS DESCRIPTION

The MCA10000ECL is implemented using a new process called MOSAIC III which achieves the high performance requirements of 0.12 ns (typical) for internal gate delays. This third-generation process is oxide-isolated in the same manner as was its predecessor, MOSAIC II.

The key improvement over MOSAIC II is the use of the poly electrode transistor (PET) structure which utilizes p+ polysilicon for extrinsic base doping and the base electrode and n+ polysilicon for the emitter. The polysilicon base electrode greatly enhances switching speed by reducing the series base resistance and collector-base capacitance. An "edge-defined" technique is used to achieve submicron emitter widths without the use of submicron lithography. MOSAIC III allows for polysilicon resistors in order to reduce node capacitance. The process also provides for the deposition of gold bumps as an interface for tape-automated bonding (TAB). Three levels of metallization are used, two for interconnection wiring and the third for power bus distribution.

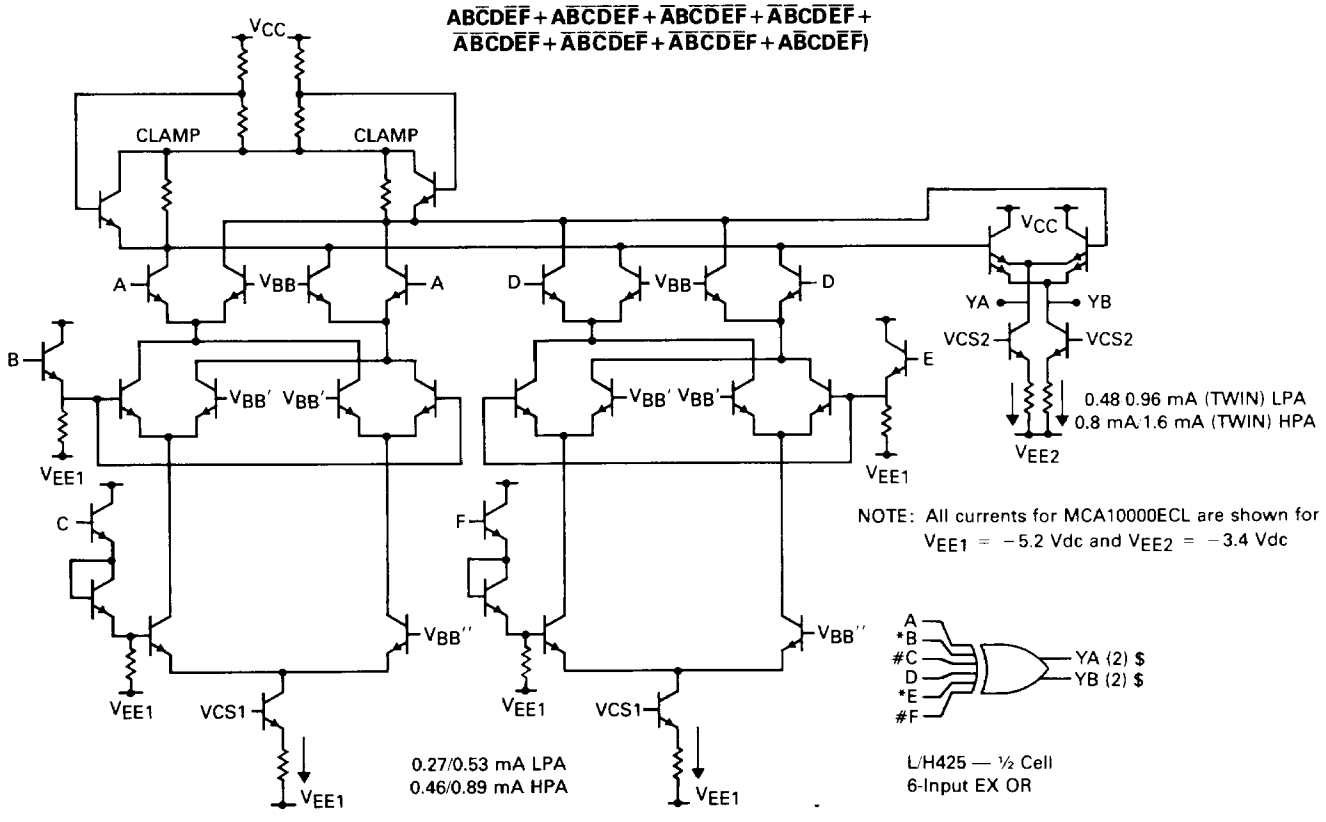
MCA3 ECL Series Performance

The MCA10000ECL array is the result of a successful match between state-of-the-art bipolar processing technology (MOSAIC III) and innovative circuit design techniques. Several key features of Motorola's MCA2 macrocell arrays as well as many new features designed to take advantage of the MOSAIC III process are implemented on the array. Speed/power programmability allows the designer to choose the exact performance level to fit his or her design needs. In the low speed/power version, the MCA10000ECL displays improved delay performance to that of the Motorola MCA2500ECL, but with four times the gate count and only slightly more power dissipation. The high-power version of the array yields performance levels which are over twice those of the MCA2500ECL.

The MCA10000ECL uses input (I) cells as input signal buffers to insure adequate voltage levels and noise margins for interfacing with external ECL 100K logic levels. I-cells are also used to buffer external signals which drive lower level macrocell inputs. I-cells are optional for 10KH interface and 100K differential inputs.

FIGURE 4 — SCHEMATIC OF 6-INPUT EXCLUSIVE OR GATE

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FEATURES

Series Gating

The value of ECL series-gating can be seen in the logic equation for the 6-input exclusive OR gate shown in Figure 4. Note that the 'L' at the beginning of the macro name implies that this is the low power version of the macro. The second-level inputs into the series-gated tree are indicated by asterisks (*) while the third-level inputs are denoted by pound signs (#).

To implement this function with gates would require thirty-two 6-input AND gates, one 32-input OR gate, and any additional gates required to form the true and complement of each input. If only 3-input gates were used, over one hundred of them would be needed to form the function.

A minimum of 224 connections would be required if gates were used, compared to seven connections for the three-level series gated macro. Each output of the cell has a two-emitter transistor that allows twice the output emitter follower current to be selected for increased drive and performance. The ability to "twin" macrocell outputs allows for output emitter currents of 0.48–0.96 mA in the low-power array or 0.8–1.6 mA in the high-power array. This also provides emitter-dotting capability while retaining the non-dotted output function through the second emitter.

Speed/Power Programmability

The speed/power programmability feature of the MCA10000ECL allows the designer to choose from a range of four performance levels. Via Motorola's CAD system, the designer can select either a high or low value resistor implant option. The output emitter-follower and switch current-source currents for each macrocell can then be individually programmed to one of two speed/power levels as shown in Figure 5. These features allow for a performance range from 0.25 ns worst case gate delays and 10 Watts (typical) power dissipation to 0.15 ns worse case gate delays and 30 Watts (typical) power dissipation for the array. The Internal Major Cell macro library contains tables which show the various delay times based on the speed/power level selected.

Series-Terminated ECL (STECL) Outputs

To facilitate multichip design, the array provides ECL outputs with programmable current-source pulldowns and selectable, on-chip series-terminating resistors. Figure 6 shows the STECL output circuit. The current source pulldown may be programmed to either 6.0 or 10 mA and a value of 0, 27, or 40 ohms may be selected for the series-termination. This feature is ideal for applications where hybrid packaging constraints may make external line terminations difficult.

FIGURE 5 — SPEED/POWER PROGRAMMABILITY

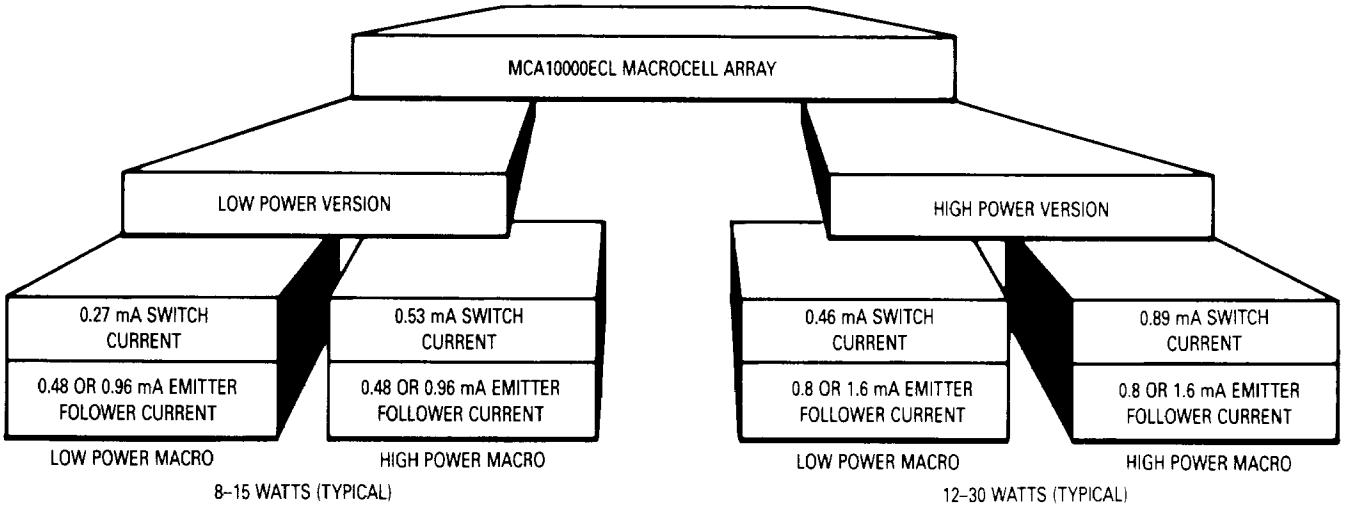
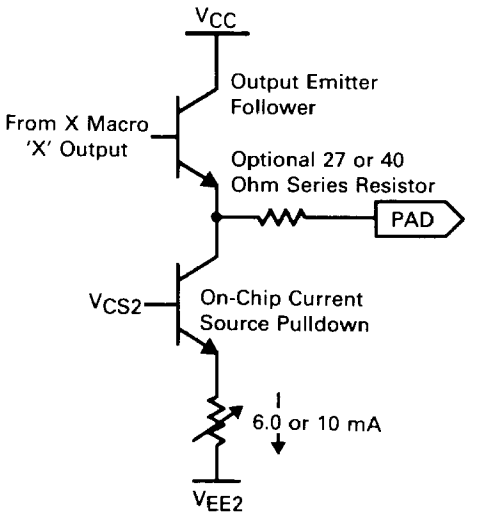


FIGURE 6 — SERIES-TERMINATED ECL (STECL) OUTPUTS



Flexible I/O Structure

There is a total of 424 output and input cells on the chip — 200 Output (O) Cells and 224 input Interface (I) Cells. The chip contains 256 I/O ports which can be used as either inputs or outputs. ECL outputs are capable of driving 50, 60, and 68 ohm loads at standard ECL levels as well as 50 and 25 ohm loads to cutoff. Input pad with active current source pulldowns of 6.0 or 10 mA can also be selected.

Clock Pulse Generators

The MCA10000ECL array contains two clock pulse generator cell sites which are capable of producing a narrow, edge-triggered pulse. The clock generator output can also be forced to either a high or low state. The output signal from the generator is produced by a 6.0 mA emitter follower and is therefore capable of driving a large fan-out on the chip with minimal speed degradation. When using the clock generators, only a single clock edge need be supplied to the chip, thus eliminating the necessity of providing narrow clock pulses which are difficult to distribute between chips due to pulse shrinkage caused by loading conditions.

PACKAGING

The MCA10000ECL macrocell array is offered in a 235 PGA, a 289 PGA (both with optional heat sinks), and in 360-lead TAB tape in a custom carrier. (See Figures 13 thru 16) The 235-pin grid array package has 180 pins available for logic signals, while the 289-pin grid array package can have up to 256 signal pins. The 289 PGA is the higher performance package in terms of number of I/O, electrical performance, and thermal performance. The reduced number of V_{CC}/V_{EE} pins needed on the 289 is due to use of power and ground planes in the package itself to reduce voltage drops and inductance on these pins. The high power array is currently available in the 289 PGA and the 360 TAB. The low power array is available in 235 PGA, 360 lead TAB tape, 289 PGA and 289 PGA with heatsink.

The following list summarizes the features of both packages and the TAB tape:

289 Pin Grid Array
- 0.100" pin spacing
- 256 I/O
- 32 power/ground (1 loc. pin)
- multi-layer epoxy-bonded fiberglass (non-hermetic)
- CuW die attach heat slug
- TAB bond interconnect
- .008" outer lead bond pitch
- .004" pad pitch
- Ag filled epoxy die attach
- optional Motorola pin-fin heat sink

235 Pin Grid Array
- 0.100" pin spacing
- 180 I/O
- 55 power/ground
- multi-layer ceramic (hermetic)
- CuW die attach heat slug
- wire-bond interconnect
- Ag/filled epoxy die attach
- optional Thermalloy pin-fin heat sink (Part No. 2329B)

TAB (Tape Automated Bond) Tape
- Tape is in S35mm format
- Die on tape is supplied in a carrier
- Tape has two metal layers (signal layer and ground plane)
- 360 leads, .004" inner lead bond pitch, .008" outer lead bond pitch
- Tape metallurgy: Sn over .001" Cu conductor

The tape-automated bonding (TAB) process used in the 289-pin grid array package involves the use of special solder bumps on the die which are mass-bonded to a flexible tape consisting of thin copper leads attached to a polyimide dielectric substrate. Customers who opt to do their own packaging may choose to receive the MCA10000ECL bonded to the TAB tape. Parts in tape are supplied in a specially designed carrier.

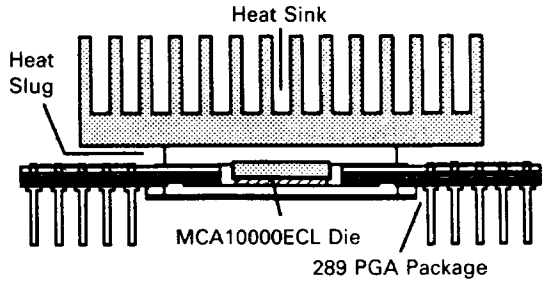
Heat Sinks and Cooling Considerations

The thermal requirements for an MCA3 design will vary according to array size, choice of power version, percent utilization of the array, desired reliability levels, and the mixture of high and low power macrocells within the array. In the low-power version of the array (8–15 Watts typical dissipation for a fully utilized array), a heat sink and air flow will be required to meet the maximum junction temperature limit of 115°C for ac specifications. The highest performance version (12–30 Watts typical dissipation for a fully utilized array) may require techniques such as impinged air with a heat sink or the use of liquid cooling in order to meet the maximum junction temperature limit.

Using the Heat Sink With the 289 PGA

The heat sink currently being offered by Motorola for the 289 PGA is a black anodized 6061 aluminum pin-fin heat sink containing 4 screw holes for direct mounting to the heat slug on the package. The chip is attached *directly* to the heat slug using a silver filled epoxy compound in order to provide a low thermal resistance (see Figure 7). A 'thermal compound' is used between the heat slug and the heat sink to provide good thermal contact. The aluminum pin-fin heat sink was chosen because of its overall thermal performance, low cost, and lower weight compared to a copper version.

FIGURE 7 — HEAT SINK MOUNTED ON THE 289 PGA



Forced Convection Impingement

Forced convection impingement involves forcing ambient air through an opening directly down on the heat sink (see Figure 8). The air flow through the pin fins is generally non-laminar. The thermal resistance from the device to the ambient air (θ_{JA}) depends heavily on the flow rate of the impinged air.

FIGURE 8 — FORCED CONVECTION IMPINGEMENT

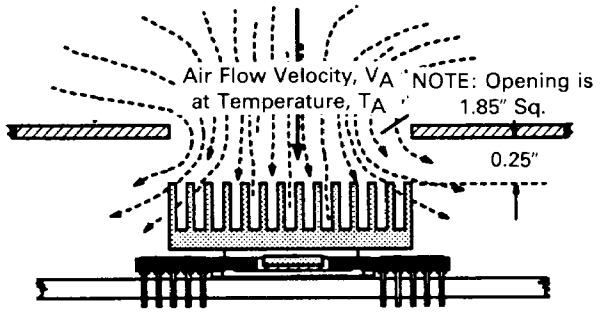
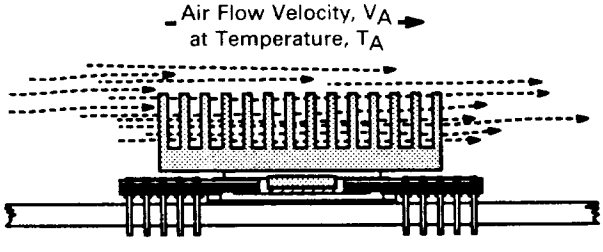


FIGURE 9 — FORCED CONVECTION HORIZONTAL



Thermal Resistance

The total thermal resistance of the package/heat sink configuration depends on many variables including parallel heat flow paths other than from the die to the heat sink (e.g. heat may flow from the board itself to the heat sink). The thermal resistance from the die to the heat

FIGURE 10 — THERMAL RESISTANCE (TYP) JUNCTION-TO-AMBIENT PGA PACKAGE WITH HEAT SINK

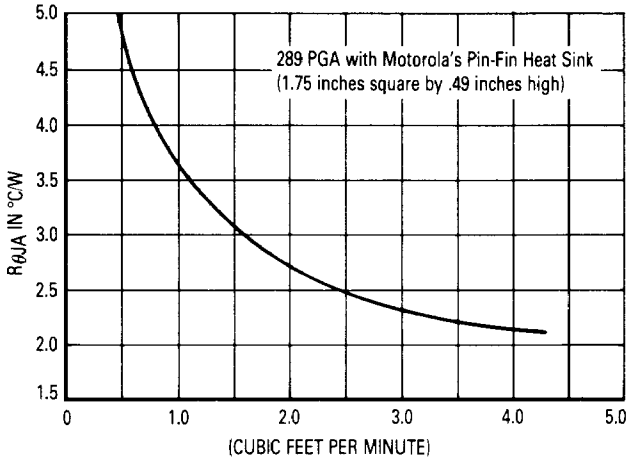


FIGURE 10a — IMPINGED AIR FLOW (289 PGA)

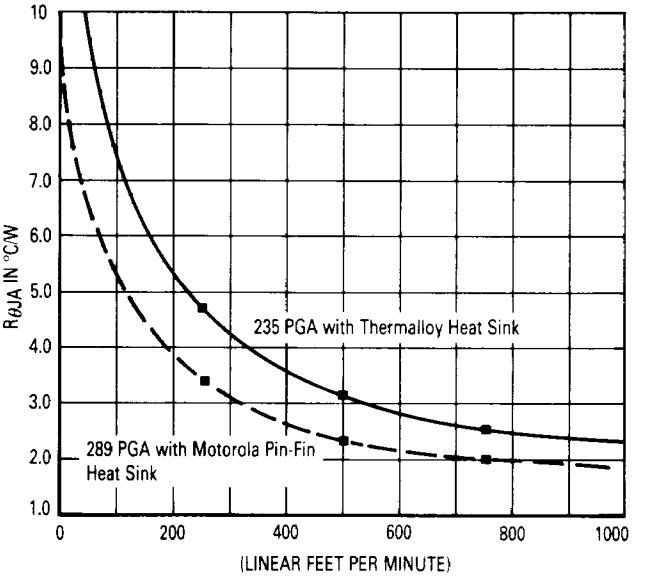


FIGURE 10b — HORIZONTAL AIR FLOW (235 & 289 PGA)

sink is composed of thermal resistances for the silicon, epoxy die attach to the heat slug, and the heat sink to ambient air.

$\theta_{JA} = \theta_{CA} + \theta_{JC}$

Example Calculation of Junction Temperature:

Assumptions:
289 PGA with heat sink
Horizontal air flow
T_A = 25°C (ambient)
P_D = 25 Watts (die power)
air flow = 600 lfpm

From Figure 10b θ_{JA} = 2.2

The junction temperature of the device is given by

$T_J = T_A + P_D\,\theta_{JA} = 25 + (25)(2.2) = 80°C$

Forced Convection Horizontal ("Conventional Flow")

Horizontal air flow, or forced convection horizontal is a conventional air flow configuration used in many TTL and lower power ECL environments (see Figure 9). Ambient air is blown horizontally (parallel to the plane of the package) over the package and heat sink.

Thermal Characteristics

θ_{JC} is typically 0.6 to 0.8°C/W for the 289 PGA package and 0.8 to 1.1°C/W for the 235 PGA package. Almost all the heat generated by the device is removed via the CuW heat slug to which the die is attached. Therefore, a heat sink or cold plate should be attached directly to the CuW heat slug in order to effectively remove heat from the package and die. Given that $\theta_{JA} = \theta_{JC} + \theta_{CA}$, the array must operate in a thermal environment such that θ_{CA} (the thermal resistance between the package case and ambient air) and T_A (the ambient temperature) are controlled in order to meet the T_J specification for AC performance of 115°C.

DESIGN DEVELOPMENT INTERFACE SYSTEM

The first step towards successful design on an MCA3 ECL Array is to contact the local Motorola sales office. The sales engineer will describe the array pricing structure and place the customer in contact with one of Motorola's Design Centers (see location listings on page 26). The application is reviewed to assure performance objectives and program schedules can be met. Design flow variables will be explained.

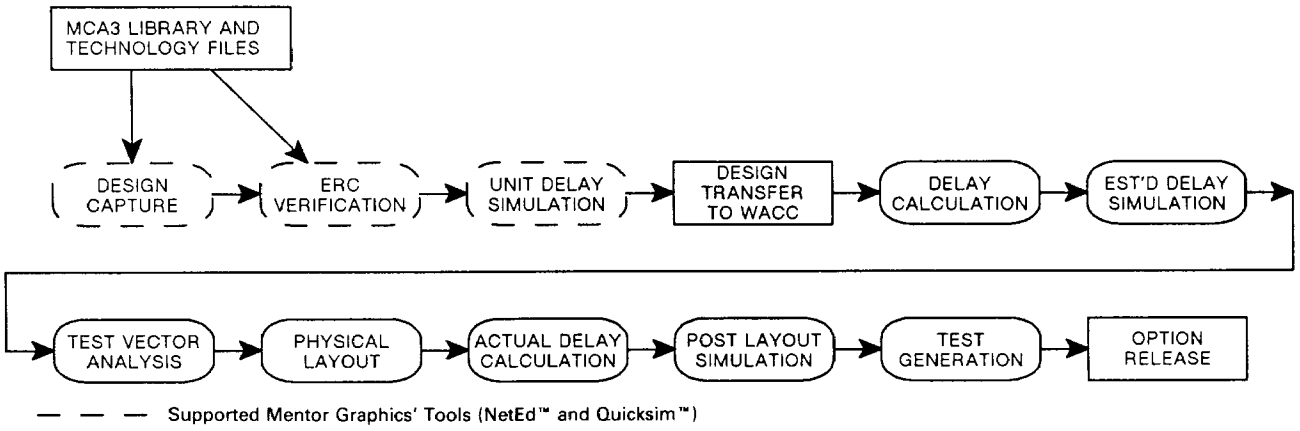
Once the optimum design flow has been determined, a Semicustom Purchase Agreement (SPA) between the customer and Motorola can be prepared. A SPA specifies the cost to the customer for services in design development and manufacture of prototype devices. The completion of this agreement is normally accomplished when the customer receives ten prototype devices.

Workstation Interface

Motorola's Open Architecture CAD System (OACS™) supports front end design on Apollo/Mentor engineering workstations. Timing and layout design tools are supported on Motorola's mainframe CAD system (WACC).

In a typical design flow using the MCA3 OACS tool set (see Figure 11), the customer executes the first design phase by developing the schematic and performing functional simulations on the workstation. Motorola then uses the resulting design files to layout the circuit and complete the design. Post layout simulations are performed and evaluated to design requirements. Design and/or layout iterations are made if necessary.

FIGURE 11 — TYPICAL MCA3ECL OACS SYSTEM DESIGN FLOW



MCA3 OACS System Features:

- Installation and Verification Utilities
- Produces Standard EDIF 2.0.0 Netlist
- Electrical Rules Checking
- Functional Simulation
- Netlist Translation to WACC

PRODUCT RELIABILITY

The highest possible level of quality in concrete, measurable terms is Motorola's goal for its products and services. Each process and product is extensively characterized and qualified. Reliability assurance engineers work closely with macrocell array designers and computer aided design software engineers to identify and eliminate problem causes. Statistical process control techniques are used in each step of manufacturing to assure first pass design success for all customers.

In addition to initial qualification the Reliability Engineering Department performs ongoing reliability testing to maintain a high level of confidence in fabrication and assembly operations. Failure rate as a function of junction temperature is plotted for the MCA10000ECL array in Figure 12. At a junction temperature of 115°C the failure rate is calculated to be 98 FIT (0.0297%/1000 hrs.) with a 90% confidence level. An activation energy of 0.70 EV was used to calculate acceleration factors for other temperatures.

1 FIT = One device failure per 10^9 device hours

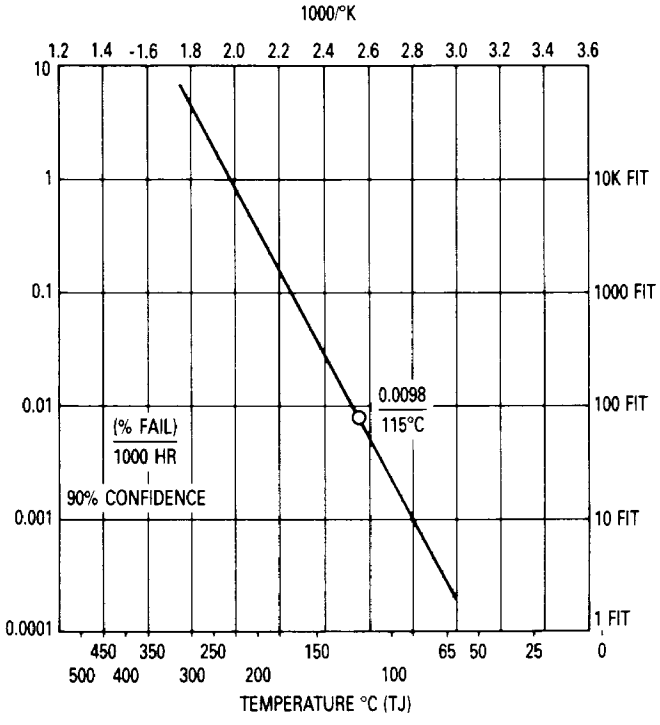
or

One part per million failure rate per 10^3 hours

This data has been derived from over 1,157,000 device hours without a single failure.

As a result of exceedingly high quality and reliability standards, Motorola has achieved one of the lowest part reject records in the industry.

FIGURE 12 — FAILURE RATE versus JUNCTION TEMPERATURE



MCA10000ECL
MOSAIC III MACROCELL ARRAY
Static operation failure-rate as a function of junction temperature
(Slope of line based on Arrhenius equation
with 0.70 EV activation energy)

MACROCELL LIBRARY

Each macrocell M, O, and I Cell location contains a number of conventional transistors and resistors that can be interconnected with CAD selected metal patterns to form logic functions. The macrocell library contains pre-defined metal patterns for more than 180 different logic functions. Designers may select any of the macrocell functions for any M, O, and I Cell location. Each macrocell, however, may only be placed in the appropriate cell location type. An M-cell, may only be placed in an M cell location, an X-cell may only be placed in an O cell location, and a I-cell may only be placed in a I-cell location.

A list of macrocells is shown in Table 2.

Internal (M) Cells

The M Cells in the array comprise the internal area on the chip and are used for the majority of logic capability. Each M Cell contains 76 resistors and 76 transistors. The macros in the M-Cell library can use 1/4, 1/2, 3/4 or 1 entire Internal cell location. Each macro specifies how much of the cell is needed to implement that particular function.

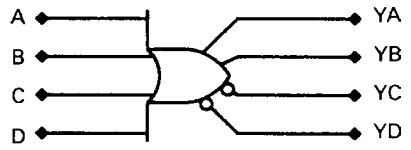
Worst-case propagation delay is specified for V_{EE1} = −4.5 V ± 0.3 V or V_{EE1} = −5.2 V ± 8%, V_{EE2} = −3.4 V ± 8%, and a maximum junction temperature of T_J max = 115°C. In general, a lower junction temperature can result in faster propagation delays. Macrocell power dissipation is specified at V_{EE1} = −5.2 V. For V_{EE1} = −4.5 V, the typical power is calculated by multiplying P_D by the factor 0.87. The specified power dissipation values do not include the output emitter follower power which is 2.72 mW/output in the high-power array or 1.63 mW/output in the low-power array (V_{EE2} = −3.4 V).

The worst-case setup times are also listed for all flip-flops and latches. Hold times are zero unless otherwise specified.

The worst-case minimum pulse width is specified for the clock inputs of flip-flops and latches to insure proper operation.

An asterisk (*) indicates an input into the 2nd level of a series-gated tree. A pound sign (#) indicates an input into the 3rd level of a series gate structure. Internal input followers are used to translate to the proper levels.

MACRO: 201 — 4-Input OR/NOR
1/4 Cell
1 Level Series Gating



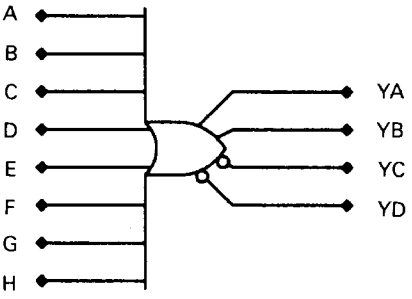
POWER: (mW)

	Low Power Array	High Power Array
L Macro	1.4	2.4
H Macro	2.8	4.7

$YA = YB = \overline{YC} = \overline{YD} = A + B + C + D$

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B,C,D	YA,YB	250	275	200	200	200	200	175	175
A,B,C,D	YC,YD	400	400	300	300	300	300	250	250

MACRO: 403 — 8-Input OR/NOR
1/4 Cell
1 Level Series Gating



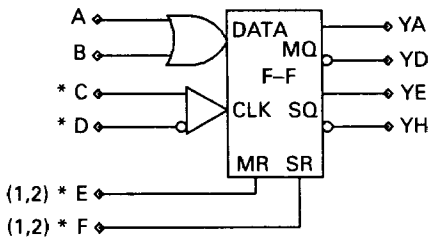
POWER: (mW)

	Low Power Array	High Power Array
L Macro	1.4	2.4
H Macro	2.8	4.7

$YA = YB = \overline{YC} = \overline{YD} = A + B + C + D + E + F + G + H$

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B,C,D,E,F,G,H	YA,YB	225	250	175	200	175	175	150	150
A,B,C,D,E,F,G,H	YC,YD	800	725	475	400	475	400	300	275

MACRO: 376 — D Flip-Flop with Differential Clock
1/2 Cell
2 Level Series Gating



POWER: (mW)

	Low Power Array	High Power Array
L Macro	9.3	17.6
H Macro	12.0	22.0

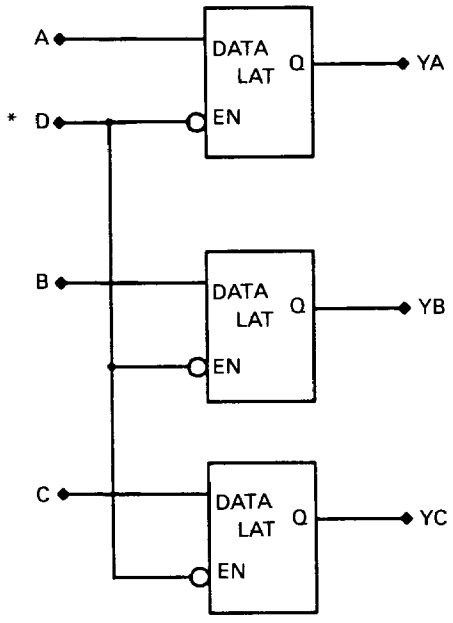
TRUTH TABLE

Master Reset	Slave Reset	Data	Clock		Master Q	Slave Q
E	F	A+B	C	D	YA	YE
L	L	X	H	L	—	—
L	L	L/H	L	H	L/H	—
L	L	L	L→H	H→L	L	L
L	L	H	L→H	H→L	H	H
H	X	X	H	L	L	L
H	L	L/H	L	H	L/H	—
X	H	L/H	L	H	L/H	L/L
L	H	X	H	L	—	—
H	H	H	L→H	H→L	⌝	⌐
X	X	L	L→H	H→L	L	L
H	L	H	L→H	H→L	⌝	⌐
L	H	H	L→H	H→L	H	⌐

NOTE: — = NO CHANGE

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A/B	YA	300	300	200	250	200	200	175	200
A,B	YD	200	250	175	200	150	175	150	175
C,D	YA	350	450	275	350	250	300	225	275
C,D	YD	275	400	250	300	250	275	200	250
C,D	YE	350	500	275	375	250	325	225	300
C,D	YH	275	400	250	300	250	275	200	250
E	YA	—	550	—	400	—	375	—	325
E	YD	450	—	350	—	325	—	300	—
E	YE	—	1050	—	750	—	700	—	600
E	YH	850	—	650	—	600	—	550	—
F	YE	—	550	—	400	—	375	—	325
F	YH	450	—	350	—	325	—	300	—
SET UP TIME		475		375		375		250	
MIN CLOCK PERIOD		1250		900		900		600	
MIN CLK PSE WIDTH		625		450		450		300	
MIN RST PSE WIDTH		975		900		900		600	
MIN REST RECRY TIME		625		450		450		300	

MACRO: 893 — 3xD Latch with Common Clock
1/2 Cell
2 Level Series Gating



POWER: (mW)

	Low Power Array	High Power Array
L Macro	12.8	21.3

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B,C	YA,YB,YC	350	400			250	250		
D	YA,YB,YC	475	525			375	475		
SET UP TIME		600				450			
MIN ENABLE PULSE WIDTH		1000				750			

TRUTH TABLE

Data	$\overline{EN}$	Q
A/B/C	D	YA/YB/YC
X	H	—
L	L	L
H	L	H

NOTE: — = NO CHANGE

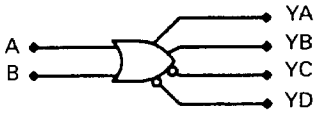
NOTE:
Latches are enabled when input D is low.

Input Macrocells

The input interface cells are interspersed among the Output cells around the periphery of the chip. All 100K inputs coming onto the chip must be connected to an Interface Cell. 10KH inputs may go directly to the upper level of an M-cell. The output of I cells is then routed to the internal portion of the macrocell array. These cells are necessary to insure full compatibility and adequate noise margins when interfacing with the various ECL logic families. Interface Cells can perform simple logic functions such as a 2-input NOR or a differential buffer.

NOTE: Power values listed are for V_{EE2} = −3.4 Vdc.

MACRO: I00 — 2 Input OR/NOR
1 I-Cell
1 Level Series Gating



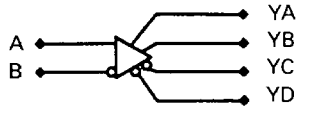
$YA = YB = \overline{YC} = \overline{YD} = A + B$

POWER: (mW)

	Low Power Array	High Power Array
L Macro	0.9	1.5
H Macro	1.8	2.9

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B	YA,YB	225	250	175	200	175	175	150	150
A,B	YC,YD	225	275	175	200	175	200	150	175

MACRO: I03 — Differential Buffer
1 I-Cell
1 Level Series Gating



$YA = YB = \overline{YC} = \overline{YD} = A = \overline{B}$

POWER: (mW)

	Low Power Array	High Power Array
L Macro	0.9	1.5
H Macro	1.8	2.9

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B	YA–YD	175	225	175	200	150	150	150	150

TRUTH TABLE

A	B	YA,YB	YC,YD
L	L	ND	ND
L	H	L	H
H	L	H	L
H	H	ND	ND

NOTE: ND = NOT DEFINED

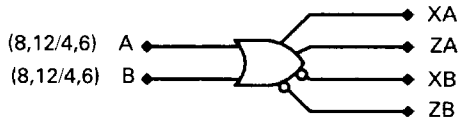
Output Driver (X) Macrocells

The Output Cells are located around the periphery of the array. Macrocells implemented using O-Cells have either an 'HX,' 'LX,' or 'ZX' (cutoff driver) prefix followed by the macro number (e.g. HX71). X macrocells can use 1 or 2 of these Output Cells as indicated in the library.

The X Cells are used primarily to provide an output interface between the internal logic in the array and the logic outside the package by supplying 25 ohm, 50 ohm, and 68 ohm drive capability. These macros also provide extra logic capability with logic functions such as OR-AND, Exclusive OR with enable, flip-flops and latches. The Output cell provides macros with a similar logic capability to 1/4 of a Major Cell.

NOTE: DC loading is shown in parentheses (). For example, if (8,12/4,6) is shown, that input represents a DC load of 8 for a low power macro in the low power array, 12 for a high power macro in the low power array, 4 for a low power macro in the high power array, and 6 for a high power macro in the high power array. The number of AC loads is shown in a separate table if it is other than one.

MACRO: X01 — 2 Input OR/NOR
1 O-Cell
1 Level Series Gating



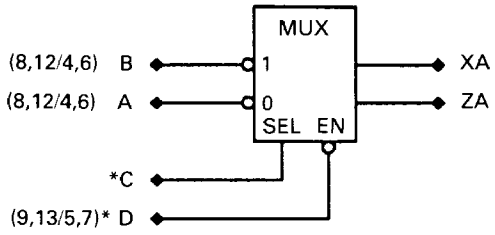
POWER: (mW)

	Low Power Array	High Power Array
L Macro	12.4	13.1
H Macro	17.9	19.1

$XA = ZA = \overline{XB} = \overline{ZB} = A + B$

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B	XA	500	300	350	275	475	300	350	200
A,B	XB	525	350	375	275	500	300	350	250
A,B	ZA	425	425	325	350	400	400	325	325
A,B	ZB	425	450	350	350	400	425	325	350

MACRO: X53 — 2-to-1 MUX with Enable (Low)
1 O-Cell
2 Level Series Gating



POWER: (mW)

	Low Power Array	High Power Array
L Macro	13.8	15.0
H Macro	19.4	21.0

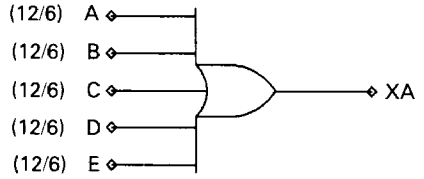
TRUTH TABLE

D	C	XA,ZA
H	X	L
L	L	$\overline{A}$
L	H	$\overline{B}$

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B	XA	550	400	400	300	550	375	400	300
A,B	ZA	500	500	400	375	475	475	375	375
C	XA	650	450	500	350	625	450	450	375
C	ZA	575	575	475	425	550	575	450	425
D	XA	675	475	500	375	650	475	475	375
D	ZA	600	600	475	450	575	600	450	450

	Number of AC Loads		
Input	1st Level	2nd Level	3rd Level
D	1	1	

MACRO: ZX05 — 5 Input OR (50 Ohm Cutoff Driver)
1 O-Cell
1 Level Series Gating



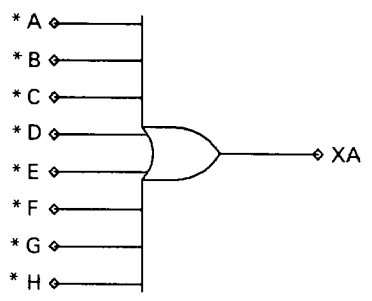
$XA = A + B + C + D + E$

POWER: (mW)

	Low Power Array	High Power Array
L Macro	17.9	19.1

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B,C,D,E	XA	550	550			550	550		

MACRO: ZX85 — 8-Input OR GATE (25 Ohm Cutoff Driver)*
2 O-Cell
2 Level Series Gating



XA = A + B + C + D + E + F + G + H

POWER: (mW)

	Low Power Array
L Macro	38.9

MACRO DELAYS (ps)		Low Power Array				High Power Array			
		L Macro		H Macro		L Macro		H Macro	
IN	OUT	(+)	(−)	(+)	(−)	(+)	(−)	(+)	(−)
A,B,C,D	XA	500	300						
E,F,G,H	XA	600	425						

NOTE: * Indicates macro is available on MCA10000ECL Low Power Array only.

TABLE 2 — MACRO LISTING

SIZE indicates the macrocell size in quarter cells for the Internal (M) macrocells and in full I or O cells for the Input Interface or Output macrocells, respectively.

SG indicates the levels of series gating used in the macrocell function. Note that a '3' in this column denotes a macro which uses three-level series gating and thus cannot be used with a supply voltage of −4.5 Vdc. **All three-level series gated functions are indicated by shading.**

INTERNAL (M) MACROCELLS

Macro	Function	Size	SG
L/H200	5-INPUT OR/NOR	1/4 CELL	1
L/H201	4-INPUT OR/NOR	1/4 CELL	1
L/H202	2-INPUT OR/NOR	1/4 CELL	1
L/H203	8-INPUT OR/NOR	1/2 CELL	2
L204	12-INPUT OR/NOR	1/2 CELL	1
L/H207	6-INPUT OR/NOR	1/4 CELL	2
L/H211	2-2 OR/AND	1/4 CELL	2
L/H212	3-2-2-2 OR/AND	1/2 CELL	2
L213	4-3-3-3 OR/AND	1/2 CELL	1
L/H214	2-2-2-2-1-1-1-1 OR/AND	FULL CELL	2
L/H215	2-2-3-3-3 OR/AND	FULL CELL	2
L/H216	4-2-3-2-3 OR/AND	FULL CELL	2
L217	5-4-3-2 OR/AND	1/2 CELL	1
L/H218	5-4-3-2-1 OR/AND	FULL CELL	2
L/H219	3-3 OR/AND	1/4 CELL	2
L/H221	2-2 OR/EXOR	1/4 CELL	2
L/H222	DUAL 2-2 OR/AND/EXNOR	FULL CELL	2
L/H223	4-INPUT EXNOR	1/2 CELL	2
L/H224	4-INPUT EXOR	1/2 CELL	2
L/H225	2-1-1-2 OR/AND/EXOR	1/2 CELL	2
L/H226	2-1-1-2 OR/AND/EXNOR	1/2 CELL	2
L/H227	2-1 EXOR/AND/NAND	1/2 CELL	2
L/H228	2-1 AND/EXOR	1/4 CELL	2
L251	4-TO-1 MUX W/ENABLE (LOW)	1/2 CELL	2
L/H252	QUAD 2-TO-1 MUX	FULL CELL	2
L/H253	2-TO-1 MUX W/ENABLE (LOW)	1/4 CELL	2
L/H254	2-TO-1 MUX W/GATED INPUTS	1/4 CELL	2
L/H255	DUAL 2-TO-1 MUX W/COM. SELECT	1/2 CELL	2
L/H256	2-TO-1 MUX	1/4 CELL	2
L258	4-TO-1 MUX W/ENABLE (HIGH)	1/2 CELL	2
L/H259	4-TO-1 MUX	1/2 CELL	2
L/H261	1-OF-4 DECODER W/ENABLE (LOW)	1/2 CELL	2
L/H262	1-OF-4 DECODER W/ENABLE (HIGH)	1/2 CELL	2
L/H263	1-OF-4 DECODER (HIGH)	FULL CELL	2
L/H277	4-2-4-2-4-2 OR/AND	3/4 CELL	2

TABLE 2 — MACRO LISTING (continued)

INTERNAL (M) MACROCELLS

Macro	Function	Size	SG
L/H278	3 DATA INPUT DATA LATCH	1/4 CELL	2
L/H279	4-2-4-2-4-2-4-2 OR/AND	FULL CELL	2
L/H280	4-2-4-2 OR/AND	1/2 CELL	2
L/H281	FULL ADDER	FULL CELL	2
L/H282	FULL ADDER W/GATED INPUTS	1/2 CELL	2
L/H283	2-BIT LOOK-AHEAD CARRY	FULL CELL	2
L/H284	HALF ADDER W/GATED INPUTS	1/4 CELL	2
L/H285	3-BIT ADDER (SUM)	1/2 CELL	2
L/H286	3-BIT ADDER (CARRY)	1/2 CELL	2
L/H290	D FLIP-FLOP WITH SET AND RESET	1/2 CELL	2
L/H291	D FLIP-FLOP WITH RESET	1/2 CELL	2
L/H292	D FLIP-FLOP WITH MUX	3/4 CELL	2
L/H293	D LATCH WITH RESET	1/4 CELL	2
L/H294	D LATCH WITH MUX	1/2 CELL	2
L/H295	GATED 2-WAY D LATCH	1/2 CELL	2
L/H296	EXNOR D LATCH	1/2 CELL	2
L/H297	GATED 4-WAY D LATCH	3/4 CELL	2
L/H298	DUAL D LATCH W/RESET	1/2 CELL	2
L302	INPUT OR/NOR	1/2 CELL	1
L/H310	4-4-4-4 OR/AND	FULL CELL	1
L/H311	3-3-3-3 AND/OR	FULL CELL	2
L/H312	3-3-3 AND/OR	1/2 CELL	2
L/H313	2-2 OR/AND	1/4 CELL	2
L/H315	2-2-1-1 OR/AND	1/2 CELL	2
L/H318	3-3 AND/OR	1/2 CELL	1
L319	3-3-2-1 AND/OR	1/2 CELL	2
L/H320	2-3-4-4 AND/OR W/ENABLE (HIGH)	FULL CELL	2
L/H321	6-6-4-4-2-2 OR/AND	FULL CELL	2
L322	3-3-3 AND/OR (LPA ONLY)	1/2 CELL	1
L/H323	3-2-2-2-2-3 AND/OR	FULL CELL	2
L/H324	5-5-5-5 AND/OR	FULL CELL	1
L328	2-1 AND/EXOR (LPA ONLY)	1/2 CELL	2
L/H331	3-2-2 AND/OR	1/2 CELL	2
L/H332	GATED OR	1/2 CELL	2
L/H333	GATED OR	1/2 CELL	2
L/H370	DIFFERENTIAL LINE RECEIVER	1/4 CELL	2
L/H371	2-1 MUX WITH DIFFERENTIAL INPUTS	1/4 CELL	2
L/H372	D FLIP-FLOP W/DIFFERENTIAL CLOCK AND DATA	1/2 CELL	2
L/H373	2-1 MUX W/DIFF INPUTS AND DIFF MUX CTL	1/4 CELL	1
L/H374	DIFFERENTIAL LINE RECEIVER	1/4 CELL	1
L/H375	D FLIP-FLOP WITH DIFFERENTIAL CLOCK	1/2 CELL	2
L/H376	D FLIP-FLOP WITH DIFFERENTIAL CLOCK	1/2 CELL	2
L380	NOR LATCH	1/4 CELL	1
L/H381	D FLIP-FLOP WITH SET	1/2 CELL	2
L/H391	D FLIP-FLOP, NEGATIVE EDGE TRIGGERED	1/2 CELL	2
L/H392	D FLIP-FLOP WITH MUX, NEGATIVE EDGE TRIGGERED	3/4 CELL	2
L/H393	D LATCH WITH CLOCK ENABLE (HIGH)	1/4 CELL	2
L/H394			
L394	D FLIP-FLOP WITH MUX, NEGATIVE EDGE TRIGGERED	FULL CELL	2
L/H395	D FLIP-FLOP WITH ASYN SET AND DATA ENABLE	FULL CELL	2
L/H396	SCAN D FLIP-FLOP	FULL CELL	2
L/H397	D LATCH WITH ASYN SET	1/4 CELL	2
L/H398	SCAN D LATCH W/ASYN SET	1/2 CELL	2
L/H400	12-INPUT OR	1/4 CELL	2
L/H401	12-INPUT NOR	1/4 CELL	2
L402	2-INPUT OR/NOR, 3-INPUT OR/NOR	1/4 CELL	1
L/H403	8-INPUT OR/NOR	1/4 CELL	1
L/H404	12-INPUT NOR	1/2 CELL	3
L/H411	2-2-2 OR/AND	1/4 CELL	3
L/H413	4-3-3-3 OR/AND	1/2 CELL	2
L414	3-3-3-3 OR/AND	1/2 CELL	2

INTERNAL (M) MACROCELLS

Macro	Function	Size	SG
L/H416	4-2-3-2-3 OR/AND	FULL CELL	3
L/H417	5-4-3-2 OR/AND	1/2 CELL	2
L/H418	5-4-3-2-1 OR/AND	3/4 CELL	2
L/H419	4-4 OR/AND	1/4 CELL	2
L421	DUAL EXOR	1/4 CELL	2
L/H422	DUAL 2-2 OR/AND/EXOR	1/2 CELL	3
L/H424	6-INPUT EXNOR	1/2 CELL	3
L/H425	6-INPUT EXOR	1/2 CELL	3
L/H427	2-1 EXOR/AND/NAND	1/4 CELL	3
L/H438	6-5-4-3-2-1 OR/AND	1/2 CELL	3
L/H451	4-1 MUX W/ENABLE (LOW)	1/2 CELL	3
L452	QUAD 2-TO-1 MUX	1/2 CELL	2
L/H453	2-TO-1 MUX W/ENABLE (LOW)	1/4 CELL	3
L/H454	2-TO-1 MUX W/ENABLE (HIGH)	1/4 CELL	3
L/H455	DUAL 2-TO-1 MUX W/ENABLE (HIGH)	1/2 CELL	3
L456	TRIPLE 2-TO-1 MUX (COMMON SELECT)	1/2 CELL	2
L457	TRIPLE 2-TO-1 MUX	1/2 CELL	2
L/H458	4-1 MUX W/ENABLE (HIGH)	1/2 CELL	3
L/H459	DUAL 4-1 MUX	1/2 CELL	3
L/H461	1-OF-4 DECODER WITH ENABLE (LOW)	1/2 CELL	3
L/H462	1-OF-4 DECODER WITH ENABLE (HIGH)	1/2 CELL	3
L464	8-3 ENCODER	FULL CELL	3
L/H465	1-OF-4 DECODER WITH ENABLE (LOW)	1/2 CELL	3
L/H466	1-OF-4 DECODER WITH ENABLE (HIGH)	1/2 CELL	3
L470	DUAL 2-TO-1 MUX (COMMON SELECT)	1/4 CELL	2
L474	DIFFERENTIAL LINE RECEIVER (LPA ONLY)	1/2 CELL	2
L482	TRIPLE FULL ADDER	FULL CELL	2
L/H485	3-BIT ADDER	1/2 CELL	3
L/H501	2 INPUT OR (L MACRO, LPA ONLY)	1/4 CELL	1
L/H502	2 INPUT NOR (L MACRO, LPA ONLY)	1/4 CELL	1
L503	5x2 INPUT OR	1/2 CELL	1
L/H510	4-4-4-4 OR/AND	1/2 CELL	2
L/H511	3-3-3-3 AND/OR	1/2 CELL	3
L/H512	3-3-3 AND/OR	1/2 CELL	3
L/H513	3-1-1-1 OR/AND	1/4 CELL	2
L/H518	3-3 AND/OR	1/4 CELL	2
L/H519	3-3-2-1 AND/OR	1/2 CELL	2
L/H520	2-3-4-4 AND/OR W/ENABLE (HIGH)	1/2 CELL	3
L/H523	3-2-2-2-2-3 AND/OR	FULL CELL	3
H553	2-TO-1 MUX W/ENABLE (LOW)	1/4 CELL	2
L/H571	8 OUTPUT BUFFER W/DIF INPUT AND ENABLE (L MACRO, LPA ONLY)	1/2 CELL	3
L585	SCAN D FLIP-FLOP W/2-TO-1 MUX DATA INPUT	1/2 CELL	2
L593	W BUFFER	1/4 CELL	1
L/H611	3-3-3 OR/AND	1/4 CELL	3
L/H616	4-2-3-3-2 OR/AND	1/2 CELL	3
L/H618	5-4-3-2-1 OR/AND	1/2 CELL	3
L/H658	4-1 MUX	1/2 CELL	3
L/H685	FULL ADDER W/GATED INPUTS	1/2 CELL	3
L/H691	D FLIP-FLOP W/RESET	1/2 CELL	2
L/H692	D FLIP-FLOP WITH MUX	3/4 CELL	2
L/H694	D FLIP-FLOP W/RESET (NEGATIVE HOLD TIME)	1/2 CELL	2
L/H802	3-INPUT EXOR/EXNOR	1/4 CELL	3
L/H803	3-INPUT EXOR/EXNOR	1/4 CELL	3
L804	DUAL 2 INPUT AND	1/4 CELL	2
L805	DUAL 2 INPUT NAND	1/4 CELL	2
L806	DUAL 2 INPUT AND/NAND	1/4 CELL	2
L807	DUAL 2 INPUT AND/NAND	1/4 CELL	2
L/H809	8-1 MUX WITH ENABLE (HIGH)	FULL CELL	3
L/H810	8-1 MUX WITH ENABLE (HIGH)	FULL CELL	3
L811	DUAL 4 INPUT OR	1/4 CELL	1

TABLE 2 — MACRO LISTING (continued)

INTERNAL (M) MACROCELLS

Macro	Function	Size	SG
L812	DUAL 4 INPUT OR/NOR	1/4 CELL	1
L813	DUAL 4 INPUT OR/NOR	1/4 CELL	1
L814	DUAL 4 INPUT NOR	1/4 CELL	1
L815	DUAL 2 INPUT OR	1/4 CELL	1
L816	DUAL 2 INPUT OR/NOR	1/4 CELL	1
L817	DUAL 2 INPUT OR/NOR	1/4 CELL	1
L818	DUAL 2 INPUT NOR	1/4 CELL	1
L/H819	3-2-1 OR/AND	1/4 CELL	3
L820	2-INPUT OR, 2-INPUT AND	1/4 CELL	2
L850	EXPANDABLE 2-1 MUX (CODER) AND 2x2-1 MUX	1/2 CELL	2
L851	EXPANDABLE 2-1 MUX	1/2 CELL	2
L852	EXPANDABLE 2-1 MUX	1/2 CELL	2
L853	EXPANDABLE 2-1 MUX	1/2 CELL	2
L860	EXPANDABLE 4-1 MUX (CODER) WITH ENABLE	1/2 CELL	3
L/H861	EXPANDABLE 4-1 MUX	1/2 CELL	3
L/H862	EXPANDABLE 4-1 MUX	1/2 CELL	3
L/H863	EXPANDABLE 4-1 MUX	1/2 CELL	3
L870	EXPANDABLE 8-1 MUX (CODER)	1/2 CELL	3
L/H871	EXPANDABLE 8-1 MUX	1/2 CELL	3
L/H872	EXPANDABLE 8-1 MUX	1/2 CELL	3
L/H873	EXPANDABLE 8-1 MUX	1/2 CELL	3
L891	D FLIP-FLOP	1/2 CELL	2
L892	D FLIP-FLOP	1/2 CELL	2
L893	3xD LATCH WITH COMMON CLOCK	1/2 CELL	2
L/H894	D LATCH WITH MUX	1/4 CELL	3
L895	D FLIP-FLOP	1/4 CELL	2
L896	3xD LATCH WITH COMMON CLOCK AND RESET	1/2 CELL	2
L897	DUAL LATCH WITH COMMON ENABLE (LPA ONLY)	1/4 CELL	2

INPUT INTERFACE (I) MACROCELLS

L/HI00	2 INPUT OR/NOR	1 I-CELL	1
L/HI01	2 INPUT OR (H MACRO, HPA ONLY)	1 I-CELL	1
L/HI02	2 INPUT NOR (H MACRO, HPA ONLY)	1 I-CELL	1
L/HI03	DIFFERENTIAL BUFFER	1 I-CELL	1
L/HI04	DIFFERENTIAL BUFFER (H MACRO, HPA ONLY)	1 I-CELL	2
L/HI05	DIFFERENTIAL BUFFER (H MACRO, HPA ONLY)	1 I-CELL	1
L/HI06	INPUT BUFFER	1 I-CELL	1
L/HI07	INPUT BUFFER (H MACRO, HPA ONLY)	1 I-CELL	1
L/HI08	INPUT BUFFER (H MACRO, HPA ONLY)	1 I-CELL	1

X MACROCELLS (50 AND 68 OHM OUTPUT DRIVERS)

L/HX01	2 INPUT OR/NOR	1 O-CELL	1
L/HX02	4 INPUT OR/NOR	1 O-CELL	1
L/HX03	2-2 OR GATES	1 O-CELL	2
L/HX04	2-2 OR GATES	1 O-CELL	2
L/HX05	5 INPUT OR/NOR	1 O-CELL	1
L/HX06	8 INPUT OR/NOR	2 O-CELLS	2
L/HX07	DUAL AND/OR	2 O-CELLS	2
L/HX08	DUAL AND/OR	2 O-CELLS	2
L/HX11	2-2 OR/AND	1 O-CELL	2
L/HX21	2-2 OR/EXOR	1 O-CELL	2
L/HX51	2-TO-1 MUX	1 O-CELL	2
L/HX52	DUAL 2-TO-1 MUX	2 O-CELLS	2
L/HX53	2-TO-1 MUX WITH ENABLE (LOW)	1 O-CELL	2
L/HX58	4-TO-1 MUX	2 O-CELLS	3
LX59	4-TO-1 MUX (Y OUTPUTS)	2 O-CELLS	3
L/HX71	DIFFERENTIAL BUFFER	1 O-CELL	2
L/HX91	D FLIP-FLOP W/RESET	2 O-CELLS	2
L/HX92	D LATCH WITH RESET	1 O-CELL	2
L/HX93	DUAL D LATCH WITH RESET	2 O-CELLS	2
L/HX94	D FLIP-FLOP W/RESET	2 O-CELLS	2

TABLE 2 — MACRO LISTING (continued)

ZX MACROCELLS (25 AND 50 OHM CUTOFF DRIVERS)

Macro	Function	Size	SG
ZX01	2 INPUT OR (50 OHM CUTOFF DRIVER)	1 O-CELL	1
ZX02	4 INPUT OR (50 OHM CUTOFF DRIVER)	1 O-CELL	1
ZX03	2-2 OR (50 OHM CUTOFF DRIVER)	1 O-CELL	2
ZX04	2-2 OR (50 OHM CUTOFF DRIVER)	1 O-CELL	2
ZX05	5-INPUT OR (50 OHM CUTOFF DRIVER)	1 O-CELL	1
ZX06	8-INPUT OR (50 OHM CUTOFF DRIVER)	2 O-CELLS	2
ZX07	DUAL AND/OR (50 OHM CUTOFF DRIVER)	2 O-CELLS	2
ZX11	2-2 OR/AND (50 Ω CUTOFF)	1 O-CELL	2
ZX51	2-TO-1 MUX (50 Ω CUTOFF)	1 O-CELL	2
ZX52	DUAL 2-TO-1 MUX (50 Ω CUTOFF)	2 O-CELLS	2
ZX58	4-TO-1 MUX (50 Ω CUTOFF)	2 O-CELLS	3
ZX71	DIFFERENTIAL BUFFER (50 OHM CUTOFF DRIVER)	1 O-CELL	2
ZX81	25 OHM OR/NOR DRIVER (CUTOFF)*	1 O-CELL	2
ZX82	4 INPUT OR GATE (25 OHM CUTOFF DRIVER)*	1 O-CELL	2
ZX83	2-2 OR GATES (25 OHM CUTOFF DRIVER)*	2 O-CELLS	3
ZX84	2-2 OR GATES (25 OHM CUTOFF DRIVER)*	2 O-CELLS	3
ZX85	8 INPUT OR GATE (25 OHM CUTOFF DRIVER)*	2 O-CELLS	2
ZX86	2-2 OR/AND (25 OHM CUTOFF DRIVER)*	1 O-CELL	3
ZX87	2-TO-1 MUX (25 OHM CUTOFF DRIVER)*	2 O-CELLS	3

CLOCK BUFFER MACROCELLS

CLK5	DIFFERENTIAL CLOCK GENERATOR (5 GATES)	CLK CELL	2
CLK6	DIFFERENTIAL CLOCK GENERATOR (6 GATES)	CLK CELL	2
CLK7	DIFFERENTIAL CLOCK GENERATOR (6 GATES + EXT. GATES)	CLK CELL	2

STANDARD ECL OUTPUTS

VO25	25 OHM PAD CELL	PAD CELL	
VO50	50/68 OHM PAD CELL	PAD CELL	

BIDIRECTIONAL I/O CELLS

VB25	25 OHM BIDIRECTIONAL PAD CELL	PAD CELL	
VB50	50 OHM BIDIRECTIONAL PAD CELL	PAD CELL	
VBS0	BIDIRECTIONAL STECL BUFFER	PAD CELL	

SERIES-TERMINATED (STECL) OUTPUTS

VS00	STECL PAD CELL — 0 OHMS SERIES	PAD CELL	
VS27	STECL PAD CELL — 27 OHMS SERIES	PAD CELL	
VS40	STECL PAD CELL — 40 OHMS SERIES	PAD CELL	

TABLE 3 — DC ELECTRICAL CHARACTERISTICS

MCA3 arrays are available in the following four compatibility options:

10KH operating at −4.5 Vdc	10KH operating at −5.2 Vdc
100K operating at −4.5 Vdc	100K operating at −5.2 Vdc

The power supply voltage limits for the following tables are:

V_{EE1} = −4.2 to −4.8 volts or	V_{CC} = V_{CCO} = 0 volts
V_{EE1} = −4.784 to −5.616 volts	V_{EE2} = −3.128 to −3.672 volts

10KH COMPATIBLE OPTIONS — ECL OUTPUTS/INPUTS

		Specification Limits						
		T_J = 25°C		T_J = 65°C		T_J = 115°C		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
V_{OH}[1]	Output HIGH Voltage	−1020	−840	−980	−810	−920	−735	mV
V_{OH}[2]	Output HIGH Voltage (low power)	−1045	−840	−1000	−810	−940	−735	mV
V_{OH}[3]	Output HIGH Voltage (cutoff)	−1050	−840	−1010	−810	−950	−735	mV
V_{OL}	Output LOW Voltage	−1950	−1630	−1950	−1630	−1950	−1600	mV
V_{OL}[3]	Output LOW Voltage (cutoff)	−2020	−1950	−2020	−1950	−2020	−1950	mV
V_{IH}	Input HIGH Voltage	−1170	−810	−1130	−780	−1070	−700	mV
V_{IL}	Input LOW Voltage	−2020	−1480	−2020	−1480	−2020	−1450	mV

1. Standard (HX macro) 50 ohm outputs terminated with a 50 ohm resistor to −2.0 volts or low power (LX macro) outputs terminated with a 68 ohm resistor to −2.0 volts.
2. Low power outputs are VO50 or VB50 outputs which are driven by an LX macrocell. This spec shows levels for low power outputs with a 60 ohm external load to −2.0 volts.
3. Cutoff outputs include both 50 ohm and 25 ohm cutoff outputs.

100K COMPATIBLE OPTIONS — ECL OUTPUTS/INPUTS

		Specification Limits			
		T_J = 25°C to 115°C			
Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}[1]	Output HIGH Voltage	−1025	−955	−880	mV
V_{OH}[2]	Output HIGH Voltage (low power)	−1045	−975	−880	mV
V_{OH}[3]	Output HIGH Voltage (cutoff)	−1050	−910	−735	mV
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV
V_{OL}[3]	Output LOW Voltage (cutoff)	−2020	−1985	−1950	mV
V_{IH}	Input HIGH Voltage	−1165		−850	mV
V_{IL}	Input LOW Voltage	−2020		−1475	mV

1. Standard (HX macro) 50 ohm outputs terminated with a 50 ohm resistor to −2.0 volts or low power (LX macro) outputs terminated with a 68 ohm resistor to −2.0 volts.
2. Low power outputs are VO50 or VB50 outputs which are driven by an LX macrocell. This spec shows levels for low power outputs with a 60 ohm external load to −2.0 volts.
3. Cutoff outputs include 50 and 25 ohm cutoff outputs. Cutoff outputs are terminated with 25/50 ohm resistors to −2.0 volts. Cutoff outputs are not compensated for temperature and, therefore exhibit the same temperature tracking as the 10KH specification above.

TABLE 3 — DC ELECTRICAL CHARACTERISTICS (continued)

10KH COMPATIBLE OPTIONS — STECL OUTPUTS/INPUTS (6.0 mA and 10 mA Current Source)

Symbol	Characteristic	Specification Limits						Unit
		T_J = 25°C		T_J = 65°C		T_J = 115°C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	−1020	−810	−980	−780	−920	−700	mV
V_{OL}	Output LOW Voltage	−1950	−1630	−1950	−1630	−1950	−1600	mV
V_{IH}	Input HIGH Voltage	−1170	−810	−1130	−780	−1070	−700	mV
V_{IL}	Input LOW Voltage	−2020	−1480	−2020	−1480	−2020	−1450	mV

1. STECL output levels are specified with no external load.
2. This table specifies levels for all STECL outputs driven by HX or LX output macrocells.

100K COMPATIBLE OPTIONS — STECL OUTPUTS/INPUTS (6.0 mA and 10 mA Current Source)

Symbol	Characteristic	Specification Limits			Unit
		T_J = 25°C to 115°C			
		Min	Typ	Max	
V_{OH}	Output HIGH Voltage	−1025	−945	−850	mV
V_{OL}	Output LOW Voltage	−1900	−1785	−1620	mV
V_{IH}	Input HIGH Voltage	−1165		−850	mV
V_{IL}	Input LOW Voltage	−2020		−1475	mV

1. STECL output levels are specified with no external load.
2. This table secifies levels for all STECL outputs driven by HX or LX output macrocells.

DC CURRENT LIMITS — 10KH AND 100K COMPATIBLE OPTIONS

Symbol	Input Forcing Voltages	Specification Limits	Unit
		T_J = 25°C to 115°C	
I_{INH} Max	V_{IH} Max	$I_{pulldown} + (N_L)(I_{input})$	mA
$I_{pulldown}$	where:	0.067 for standard input (75K pulldown)	mA
$I_{pulldown}$		12.5 for 10 mA current source input	mA
$I_{pulldown}$		7.5 for 6.0 mA current source input	mA
N_L		no. of DC unit loads connected to input	UL's
I_{input}		0.5 in the low power array	mA
I_{input}		1.0 in the high power array	mA
I_{INL} Min	V_{IL} Min	0.5	μA
I_{EE1}, I_{EE2}	—	CAD LIMIT	—

DC CURRENT AND RESISTOR LIMITS — STECL OUTPUTS AND INPUT CS

Symbol	Characteristic	Specification Limits			Unit
		T_J = 25°C to 115°C			
		Min	Typ	Max	
I_{out} 10	STECL and Input CS	8.0	10	12.5	mA
I_{out} 6.0	STECL and Input CS	4.5	6.0	7.5	mA
R_{out} 27	STECL Series Resistor	20	27	42	ohms
R_{out} 40	STECL Series Resistor	30	40	56	ohms

1. I_{out} 10 and I_{out} 6.0 refer to a 10 mA or 6.0 mA, respectively, internal current source for a STECL output or an input current source.
2. R_{out} 27 and R_{out} 40 refer to a 27 ohm or 40 ohm, respectively, internal series resistor at the output of a STECL driver.

TABLE 3 — DC ELECTRICAL CHARACTERISTICS (continued)

RECOMMENDED OPERATING CONDITIONS

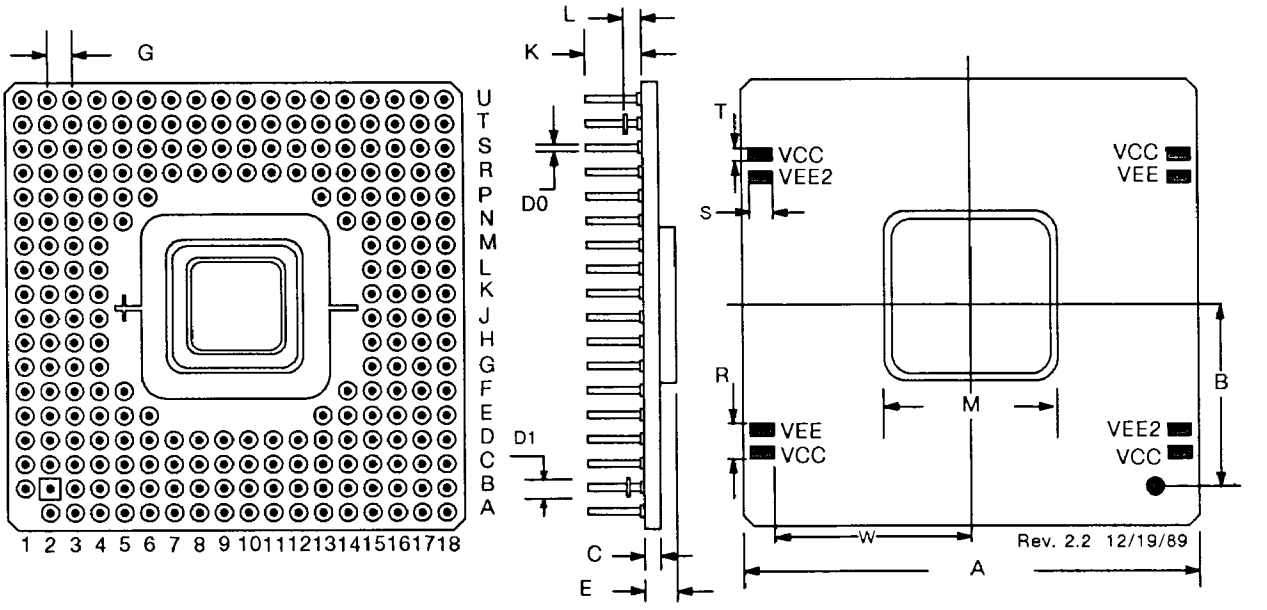
Symbol	Characteristic	Value	Unit
V_{EE1}	Supply Voltages ($V_{CC}=V_{CCO}$ = 0) for −4.5 V Options	−4.5 ± 0.3	Vdc
V_{EE2}		−3.4 ± 8%	Vdc
V_{EE1}	Supply Voltages ($V_{CC}=V_{CCO}$ = 0) for −5.2 V Options	−5.2 ± 8%	Vdc
V_{EE2}		−3.4 ± 8%	Vdc
T_J	Operating Temperature (Functional)	10 to 130	°C
T_J	Junction Temperature (AC and DC Specs)	25 to 115	°C
t_r, t_f	Max Clock Input Rise/Fall Times (20 to 80%)	5.0	ns

LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

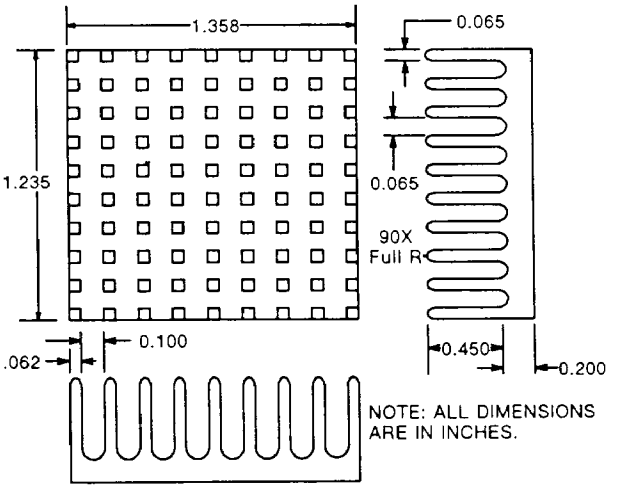
Symbol	Characteristic	Value	Unit
V_{EE1}	Supply Voltage ($V_{CC}=V_{CCO}=0$)	−7.0 to + 0.5	Vdc
V_{in}	Input Voltage ($V_{CC}=V_{CCO}=0$)	+0.5 to V_{EE2}	Vdc
V_{in}	Input Voltage on Bidirectional (Cutoff) ($V_{CC}=V_{CCO}=0$)[1]	+0.5 to −2.0	Vdc
I_{out}	Output Source Current Continuous (50/68 ohm)	30	mA
I_{out}	Output Source Current Surge (50/68 ohm)[2]	100	mA
I_{out}	Output Source Current Continuous (25 ohm)	60	mA
I_{out}	Output Source Current Surge (25 ohm)[2]	200	mA
I_{out}	Output Source Current Continuous (STECL, 10 mA)	5.0	mA
I_{out}	Output Source Current Surge (STECL, 10 mA)	40	mA
I_{out}	Output Source Current Continuous (STECL, 6.0 mA)	9.0	mA
I_{out}	Output Source Current Surge (STECL, 6.0 mA)	44	mA
T_{stg}	Storage Temperature	−55 to +150	°C
T_J	Junction Temperature (no time limit)	165	°C
T_J	Junction Temperature (<240 hours)	250	°C

1. If a cutoff output is in the low (disabled) state and is being forced by an external driver, the forcing voltage must fall between V_{CC} and −2.0 volts.
2. Surge current is defined as an output current between 30 mA and 100 mA for a 50/68 ohm output, 60 mA and 200 mA for a 25 ohm output, 5.0 mA and 40 mA for a STECL (10 mA), and 9.0 mA and 44 mA for a STECL (6.0 mA). The surge current must last for less than 10 μs and must have a duty cycle equal to or less than 1%.

FIGURE 13 — 235 PIN GRID ARRAY PACKAGE WITH OPTIONAL HEAT SINK

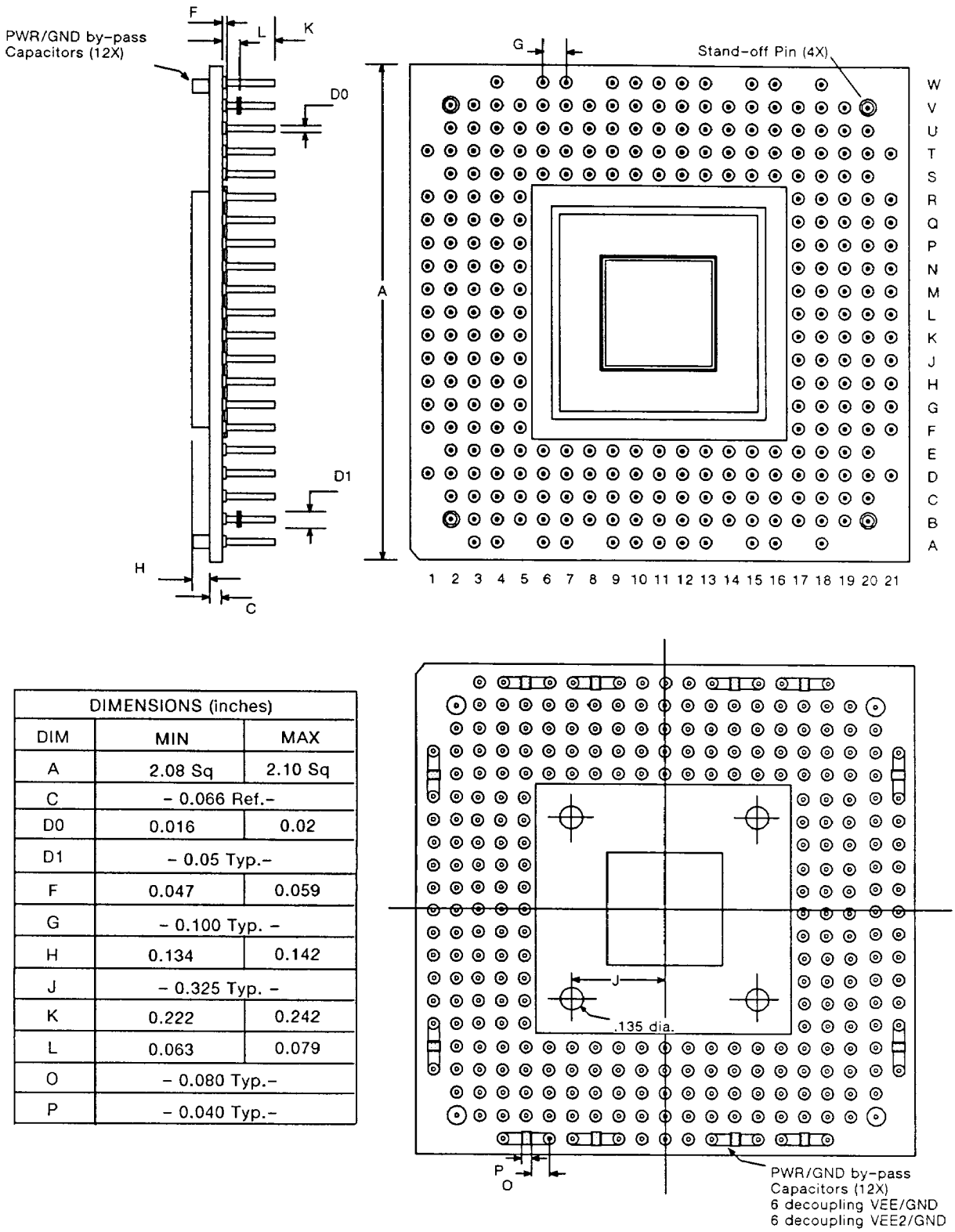


DIMENSIONS (INCHES)		
DIM	MIN	MAX
A	1.815 Sq.	1.845 Sq.
B	0.73	0.77
C	0.074	0.09
D0	0.015	0.018
D1	– 0.050 Typ.–	
E	0.139	0.147
G	– 0.100 Typ. –	
K	0.194	0.208
L	0.035	0.045
M	0.85 Sq.	0.91 Sq.
R	– 0.180 Typ. –	
S	– 0.120 Typ. –	
T	– 0.060 Typ. –	
W	0.75	0.79



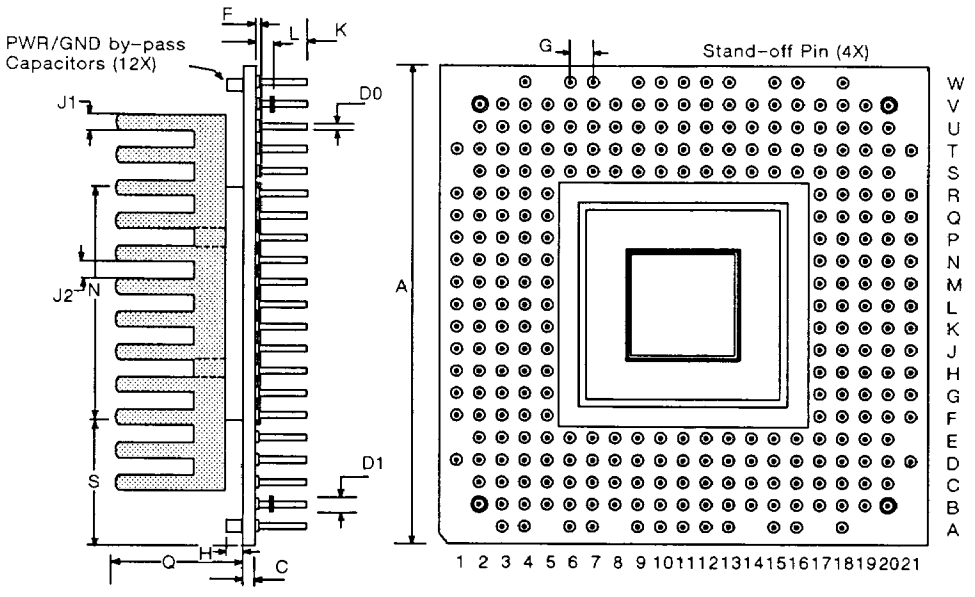
Thermalloy Heat Sink #2329B for 235 PGA

FIGURE 14 — 289 PIN GRID ARRAY PACKAGE WITH NO HEAT SINK



DIMENSIONS (inches)		
DIM	MIN	MAX
A	2.08 Sq	2.10 Sq
C	– 0.066 Ref.–	
D0	0.016	0.02
D1	– 0.05 Typ.–	
F	0.047	0.059
G	– 0.100 Typ. –	
H	0.134	0.142
J	– 0.325 Typ. –	
K	0.222	0.242
L	0.063	0.079
O	– 0.080 Typ.–	
P	– 0.040 Typ.–	

FIGURE 15 — 289 PIN GRID ARRAY PACKAGE WITH OPTIONAL HEAT SINK



DIMENSIONS (inches)		
DIM	MIN	MAX
A	2.08 Sq	2.10 Sq
C	0.066 Ref.	
D0	0.016	0.02
D1	– 0.05 Typ.–	
F	0.047	0.059
G	– 0.100 Typ. –	
H	0.134	0.142
J1	– 0.061 X 0.065 Typ. –	
K	0.222	0.242
L	0.063	0.079
J2	– 0.065 X 0.093 Typ. –	
N	– 1.000 Typ. –	
O	– 0.080 Typ. –	
P	– 0.040 Typ. –	
Q	0.614	0.642
R	– 1.755 +.015 –	
S	– 0.490 Typ. –	
T	0.645	0.655

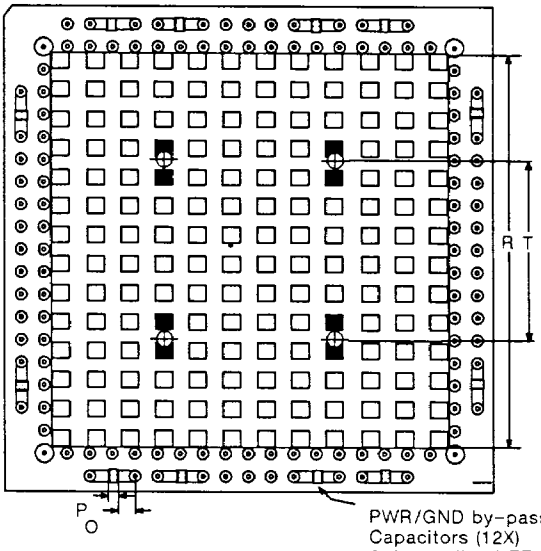
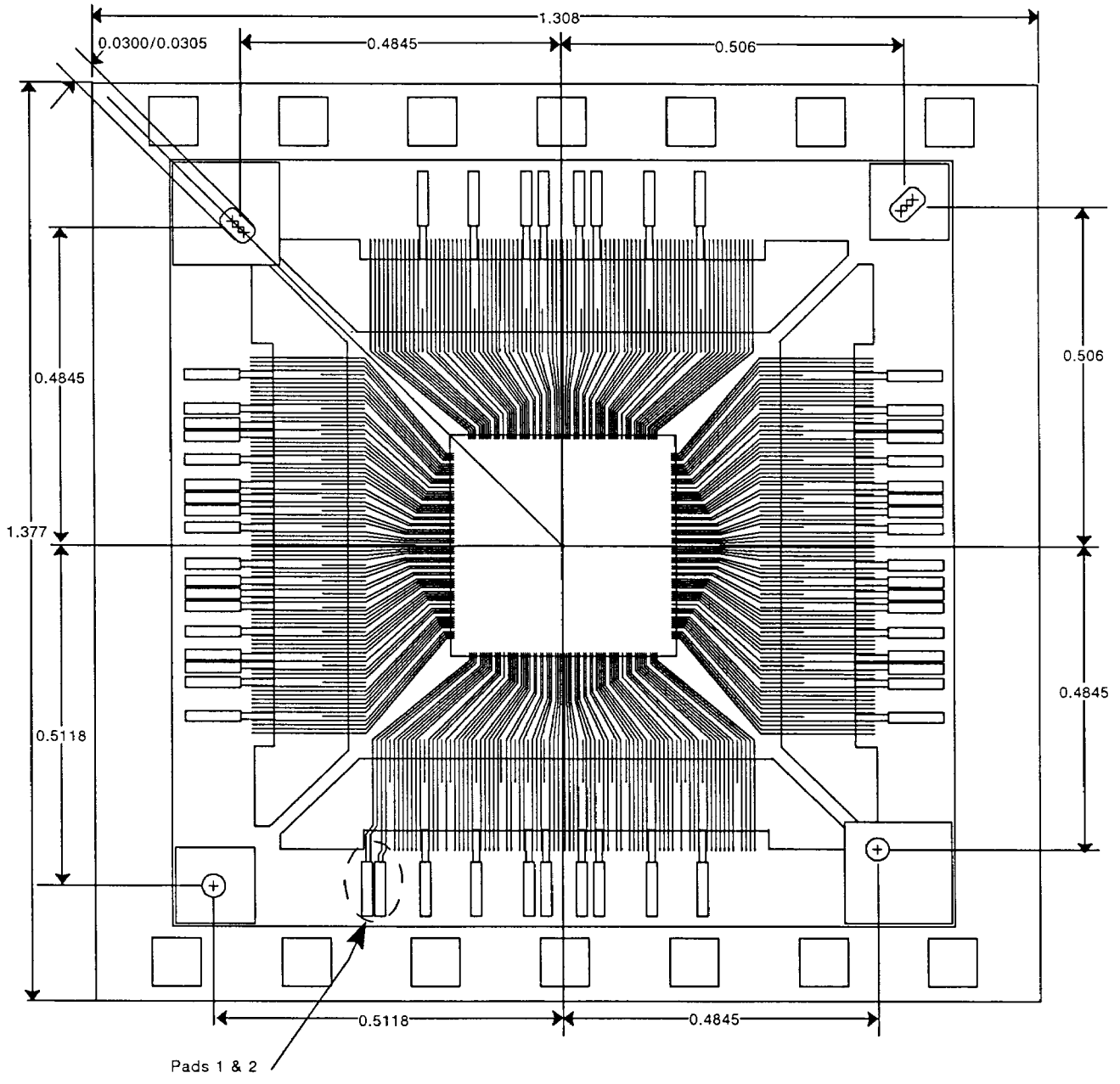


FIGURE 16 — MCA3 360 LEAD TAB TAPE
[Dimensions-Inches (not to scale)]



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