PACE1750A
SINGLE CHIP, 15MHz to 40MHz, CMOS 16-BIT PROCESSOR

FEATURES

- **Implements the MIL-STD-1750A Instruction Set Architecture**
- **Single Chip PACE Technology™ CMOS 16-Bit Processor with 32 and 48-Bit Floating Point Arithmetic**
- **DAIS Instruction Mix Execution Performance Including Floating Point Arithmetic**
  - **1.3 MIPS at 20 MHz**
  - **1.9 MIPS at 30 MHz**
  - **2.6 MIPS at 40 MHz**
- **Integer DAIS Mix Performance**
  - **3.9 MIPS at 40 MHz**
- **Conventional Integer Processing Mix Performance**
  - **5.0 MIPS at 40 MHz**
- **Instruction Execution at 40 MHz over the Military Temperature Range**
  - **0.10 µsec Integer Add/Sub**
  - **0.57 µsec Integer Multiply**
  - **0.70 µsec Floating Point Add/Sub**
  - **1.07 µsec Floating Point Multiply**
- **15, 20, 30, and 40 MHz Operation over the Military Temperature Range**
- **Extensive Error and Fault Management and Interrupt Capability**
- **24 User Accessible Registers**
- **Single 5V ± 10% Power Supply**
- **Power Dissipation over Military Temperature Range**
  - **< 0.30 watts at 20 MHz**
  - **< 0.35 watts at 30 MHz**
  - **< 0.40 watts at 40 MHz**
- **TTL Signal Level Compatible Inputs and Outputs**
- **Multiprocessor and Co-processor Capability**
- **Built-In Function (BIF) for User Defined Instructions**
- **Two programmable Timers**
- **Available in:**
  - **– 64-Pin DIP or Gull Wing (50 Mil Pin Centers)**
  - **– 68-Pin Pin Grid Array (PGA)**
  - **– 68-Lead Quad Pack (Leaded Chip Carrier)**

GENERAL DESCRIPTION

The PACE1750A is a general purpose, single chip, 16-bit CMOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support. It offers a variety of data types, including bits, bytes, 16-bit and 32-bit integers, and 32-bit and 48-bit floating point numbers. It provides 13 addressing modes, including direct, indirect, indexed, based, based indexed and immediate long and short, and it can access 2 MWords of segmented memory space (64 KWords segments).

The PACE1750A offers a well-rounded instruction set with 130 instruction types, including a comprehensive integer, floating point, integer-to-floating point and floating point-to-integer set, a variety of stack manipulation instructions, high level language support instructions such as Compare Between Bounds and Loop Control Instructions. It also offers some unique instructions such as vectored I/O, supports executive and user modes, and provides an escape mechanism which allows user-defined instructions using a coprocessor.

The chip includes 16 general purpose registers, 8 other user-accessible registers, and an array of real time application support resources, such as 2 programmable timers, a complete interrupt controller supporting 16 levels of prioritized internal and external interrupts, and a faults and exceptions handler controlling internally and externally generated faults.

The microprocessor achieves very high throughput of 2.6 MIPS for a standard real time integer/floating point instruction mix at a 40 MHz clock. It executes integer Add in 0.1 µs, integer Multiply in 0.575 µs, Floating Point Add in 0.7 µs, and Floating Point Multiply in 1.075 µs, for register operands at a 40 MHz clock speed.

The PACE1750A uses a single multiplexed 16-bit parallel bus. Status signals are provided to determine whether the processor is in the memory or I/O bus cycle, reading and writing, and whether the bus cycle is for data or instructions.

The basic bus cycle is 4 clocks long. The PACE1750A will extend the cycle by insertion of wait states in the address and data phases (in response to RDYA and RDYD signals, repectively) and will hold the machine in HI-Z if this CPU has not acquired the bus. A typical non-bus cycle is three clocks long. However, variable length cycles are used for such repetitive operations as multiply, divide, scale and normalize, reducing significantly the number of CPU CLOCKS per operation step and resulting in very fast integer and floating point execution times.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage Range	-0.5V to 7.0V
Input Voltage Range	-0.5V to V_{CC} + 0.5V
Storage Temperature Range	-65°C to + 150°C
Input Current Range	-30mA to +5mA
Voltage Applied to Inputs	-0.5V to VCC + 0.5V
Current Applied to Outputs[3]	150 mA
Maximum Power Dissipation[2]	1.5W

Operating worst case power dissipation (outputs open):	
Device type 01	0.25W at 15 MHz
Device type 02	0.30W at 20 MHz
Device type 03	0.35W at 30 MHz
Device type 04	0.40W at 40 MHz

Lead Temperature Range (soldering 10 seconds)	300°C

Thermal resistance, junction-to-case (Θ_{JC}), Note 5:	
Cases X and T	8°C/W
Cases Y and U	5°C/W
Case Z	6°C/W

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	4.5V to 5.5V
Case Operating Temperature Range	-55°C to +125°C

NOTE 1:
Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

NOTE 2:
Must withstand the added power dissipation due to short circuit test e.g., I_{OS}

NOTE 3:
Duration one second or less.

NOTE 4: Device Type Definitions from 5962-87665 SMD:
Device Type 01: 15 MHz
Device Type 02: 20 MHz
Device Type 03: 30 MHz
Device Type 04: 40 MHz

NOTE 5: Case Definitions from 5962-87665 SMD:
Case X: Dual In-Line
Case T: Dual In-Line with Gull-Wing Leads
Case Y: Leaded Chip Carrier with Gull-Wing Leads
Case U: Leaded Chip Carrier with Unformed Leads
Case Z: Pin Grid Array

DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter		Min	Max	Unit	Conditions[1]	
V_{IH}	Input HIGH Level Voltage		2.0	V_{CC} + 0.5	V		
V_{IL}	Input LOW Level Voltage[2]		–0.5	0.8	V		
V_{CD}	Input Clamp Diode Voltage			–1.2	V	V_{CC} = 4.5V, I_{IN} = –18mA	
V_{OH}	Output HIGH Level Voltage		2.4		V	V_{CC} = 4.5V	I_{OH} = –8.0mA
			V_{CC} – 0.2		V	V_{CC} = 4.5V	I_{OH} = –300µA
V_{OL}	Output LOW Level Voltage			0.5	V	V_{CC} = 4.5V	I_{OL} = 8.0mA
				0.2	V	V_{CC} = 4.5V	I_{OL} = 300µA
I_{IH1}	Input HIGH Level Current, except $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			10	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IH2}	Input HIGH Level Current, $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			50	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IL1}	Input LOW Level Current, except $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			–10	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{IL2}	Input LOW Level Current, $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			–50	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{OZH}	Output Three-State Current			50	µA	V_{OUT} = 2.4V, V_{CC} = 5.5V	
I_{OZL}	Output Three-State Current			–50	µA	V_{OUT} = 0.5V, V_{CC} = 5.5V	
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels)			10	mA	V_{IN} < 0.2V or < V_{CC} – 0.2V, f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCQT}	Quiescent Power Supply Current (TTL Input Levels)			50	mA	V_{IN} < 3.4V, f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCD}	Dynamic Power Supply Current	15 MHz		40	mA	V_{IN} = 0V to V_{CC}, tr = tf = 2.5 ns, Outputs Open, V_{CC} = 5.5V	
		20 MHz		50	mA		
		30 MHz		60	mA		
		40 MHz		70	mA		
I_{OS}	Output Short Circuit Current[3]		–25		mA	V_{OUT} = GND, V_{CC} = 5.5V	
C_{IN}	Input Capacitance			10	pF		
C_{OUT}	Output Capacitance			15	pF		
$C_{I/O}$	Bi-directional Capacitance			15	pF		

Notes

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. V_{IL} = –3.0V for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.

SIGNAL PROPAGATION DELAYS[1,2]

Symbol	Parameter	15 MHz		20 MHz		30 MHz		40 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{C(BR)L}$	$\overline{BUS\ REQ}$		45		33		25		22	ns
$t_{C(BR)H}$	$\overline{BUS\ REQ}$		45		33		25		22	ns
$t_{BGV(C)}$	$\overline{BUS\ GNT}$ setup	5		5		5		5		ns
$t_{C(BG)X}$	$\overline{BUS\ GNT}$ hold	5		5		5		5		ns
$t_{C(BB)L}$	$\overline{BUS\ BUSY}$ LOW		35		25		24		20	ns
$t_{C(BB)H}$	$\overline{BUS\ BUSY}$ HIGH		35		25		20		15	ns
$t_{BBV(C)}$	$\overline{BUS\ BUSY}$ setup	5		5		5		5		ns
$t_{C(BB)X}$	$\overline{BUS\ BUSY}$ hold	5		5		5		5		ns
$t_{C(BL)L}$	$\overline{BUS\ LOCK}$ LOW		50		30		25		21	ns
$t_{C(BL)H}$	$\overline{BUS\ LOCK}$ HIGH		50		30		25		17	ns
$t_{BLV(C)}$	$\overline{BUS\ LOCK}$ setup	5		5		5		5		ns
$t_{C(BL)X\ (IN)}$	$\overline{BUS\ LOCK}$ hold	5		5		5		5		ns
$t_{C(ST)V}$	M/$\overline{IO}$, R/$\overline{W}$ Status		45		30		25		20	ns
$t_{C(ST)V}$	AS_0-AS_3, AK_0-AK_3, D/I Status		40		25		20		20	ns
$t_{C(ST)X}$	AS_0-AS_3, AK_0-AK_3, D/I Status, M/$\overline{IO}$, R/$\overline{W}$		0		0		0		0	ns
$t_{C(SA)H}$	STRBA HIGH		25		22		17		16	ns
$t_{C(SA)L}$	STRBA LOW		25		22		17		16	ns
$t_{SAL(IBA)X}$	Address hold from STRBA LOW	5		5		5		5		ns
$t_{RAV(C)}$	RDYA setup	5		5		5		5		ns
$t_{C(RA)X}$	RDYA hold	5		5		5		5		ns
$t_{C(SDW)L}$	$\overline{STRBD}$ LOW write		25		22		17		14	ns
$t_{C(SD)H}$	$\overline{STRBD}$ HIGH		25		22		17		14	ns
$t_{FC(SDR)L}$	$\overline{STRBD}$ LOW read		25		22		17		14	ns
$t_{SDRH(IBD)X}$	$\overline{STRBD}$ HIGH	0		0		0		0		ns
$t_{SDWH(IBD)X}$	$\overline{STRBD}$ HIGH	45		30		25		17		ns
$t_{SDL(SD)H}$	$\overline{STRBD}$ write	50		40		35		20		ns
$t_{RDV(C)}$	RDYD setup	5		5		5		5		ns
$t_{C(RD)X}$	RDYD hold	5		5		5		5		ns
$t_{C(IBA)V}$	IB_0-IB_{15}		45		30		25		20	ns
$t_{FC(IBA)X}$	IB_0-IB_{15}	0		0		0		0		ns
$t_{IBDRV(C)}$	IB_0-IB_{15} setup	5		5		5		5		ns
$t_{C(IBD)X}$	IB_0-IB_{15} hold (read)	8		7		6		5		ns
$t_{C(IBD)X}$	Data valid out (write)	0		0		0		0		ns

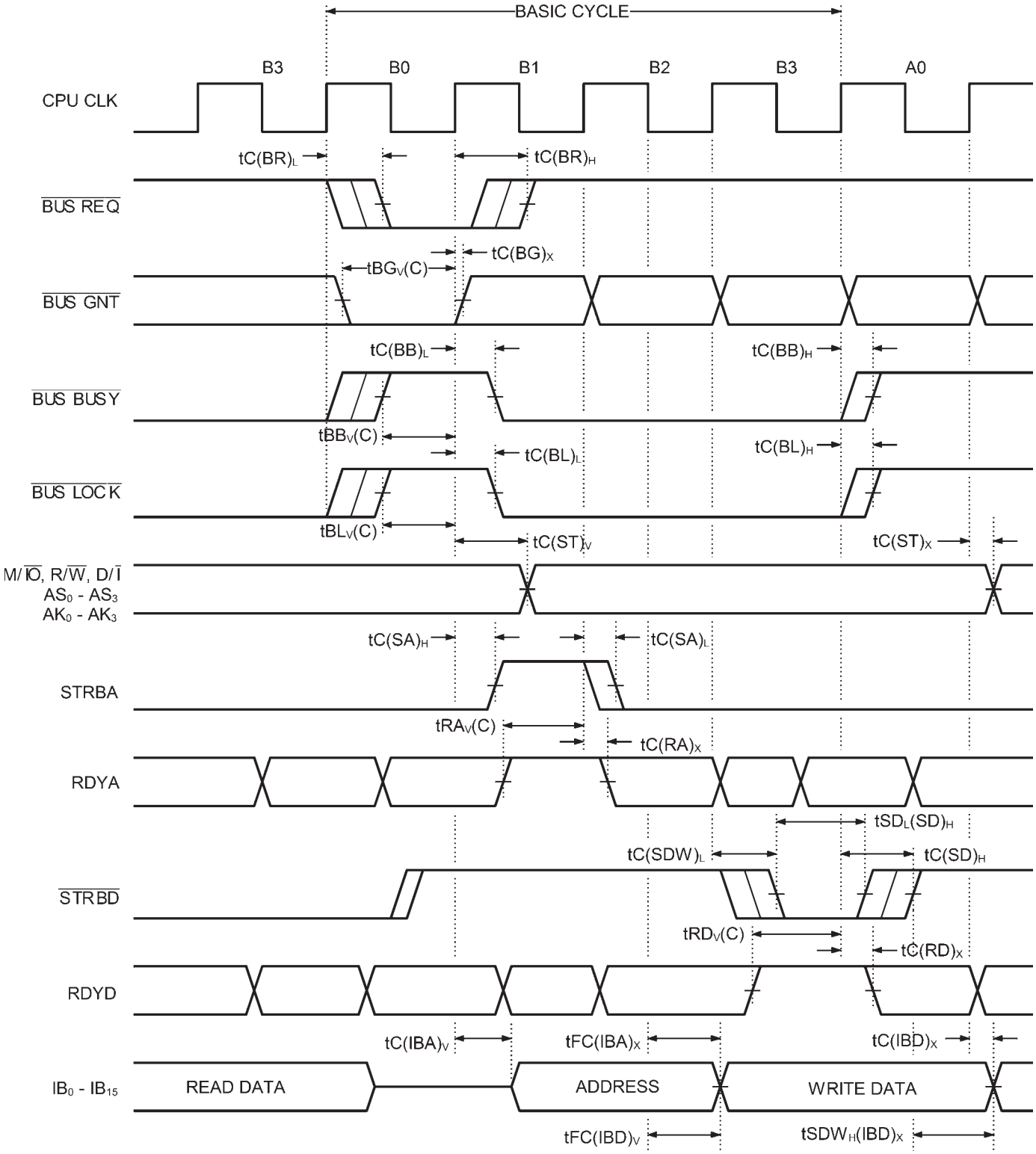
SIGNAL PROPAGATION DELAYS[1,2] (continued)

Symbol	Parameter	15 Mhz		20 MHz		30 MHz		40 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{FC(IBD)V}$	IB_0-IB_{15}		45		30		25		20	ns
$t_{C(SNW)}$	SNEW		45		30		26		22	ns
$t_{FC(TGO)}$	$\overline{\text{TRIGO RST}}$		45		30		26		22	ns
$t_{RSTL(DMA\ ENL)}$	DMA enable		45		40		35		30	ns
$t_{C(DME)}$	DMA enable		45		40		35		30	ns
$t_{FC(NPU)}$	Normal power up		45		40		35		30	ns
$t_{C(ER)}$	Clock to major error unrecoverable		75		60		50		45	ns
$t_{RSTL(NPU)}$	$\overline{\text{RESET}}$		65		50		40		30	ns
$t_{REQV(C)}$	Console request	0		0		0		0		ns
$t_{C(REQ)X}$	Console request	10		10		10		10		ns
$t_{FV(BB)H}$	Level sensitive faults	5		5		5		5		ns
$t_{BBH(F)X}$	Level sensitive faults	5		5		5		5		ns
$t_{IRV(C)}$	IOL_{1-2}INT user interrupt (0-5)	0		0		0		0		ns
$t_{C(IR)X}$	Power down interrupt level sensitive hold	10		10		10		10		ns
t_{RSTL} (t_{RSTH})	Reset pulse width	30		25		20		15		ns
$t_{C(XX)Z}$	Clock to three-state		30		22		17		13	ns
$t_{f(F)}$, $t_{1(1)}$	Edge sensitiive pulse width	5		5		5		5		ns
t_r, t_f	Clock rise and fall		5		5		5		5	ns

Notes

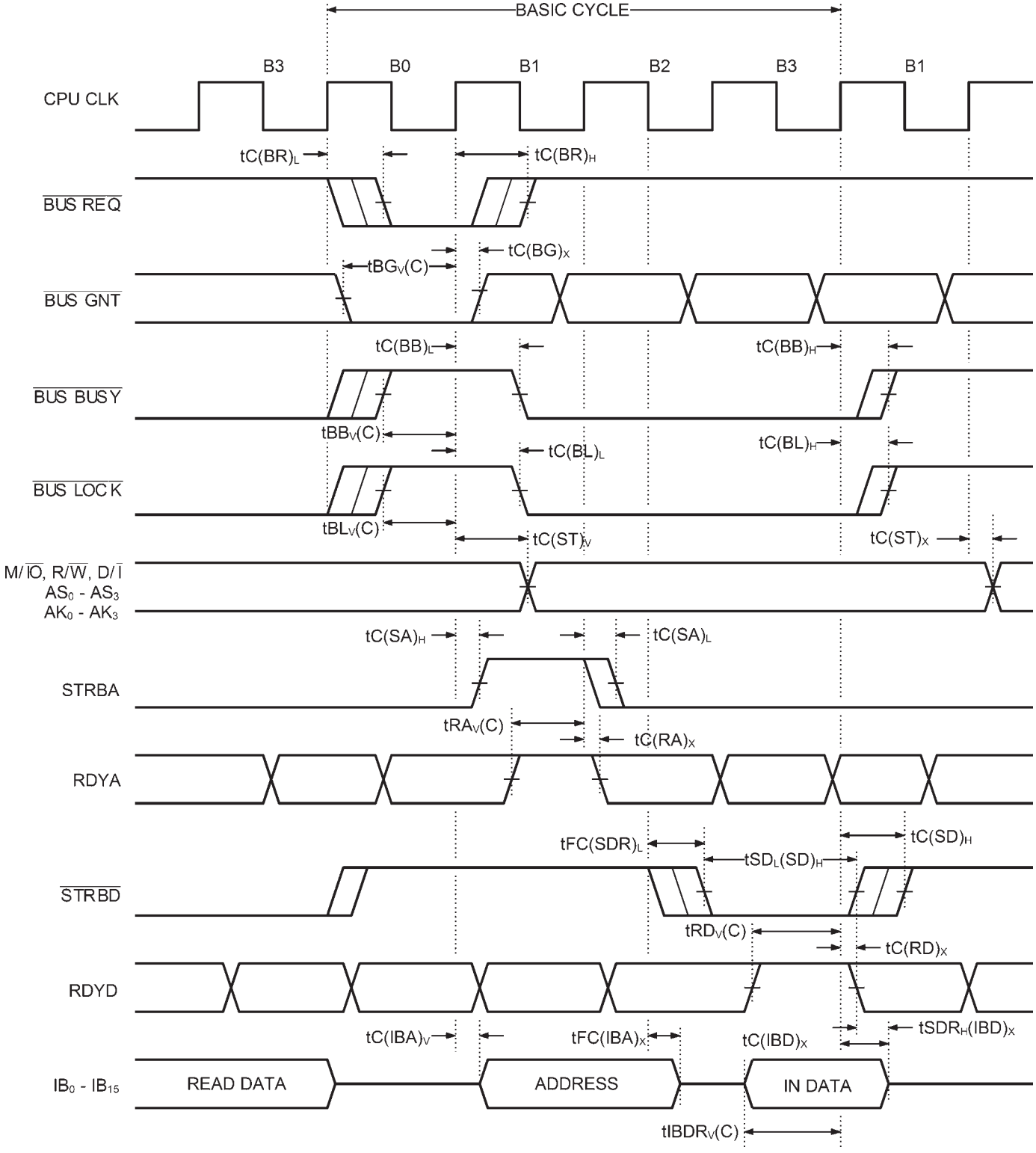
1. $4.5V \le V_{CC} \le 5.5V$, $–55°C \le T_C \le +125°C$. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. All timing parameters are composed of Three elements. The first "t" stands for timing. The second represents the "from" signal. The third in parentheses indicates "to" signal. When the CPU clock is one of the signal elements, either the rising edge "C" or the falling edge "FC" is referenced. When other elements are used, an additional suffix indicates the final logic level of the signal. "L" - low level, "H" - high level, "V" - valid, "Z" - high impedance, "X" - don't care, "LH" - low to high, "ZH" - high impedance to high, "R" - read cycle, and "W" - write cycle.

MINIMUM WRITE BUS CYCLE TIMING DIAGRAM



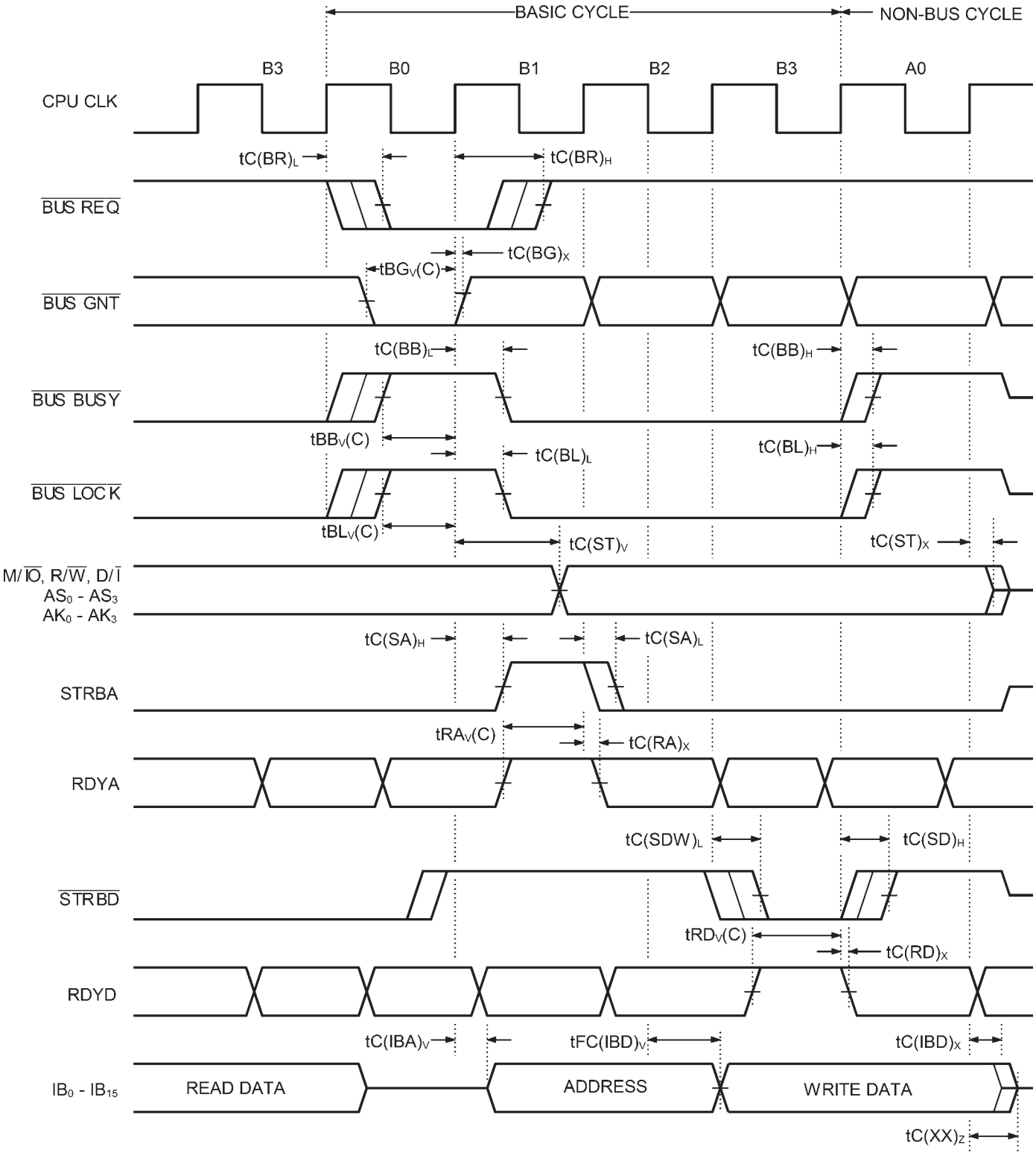
Note:
All time measurements on active signals relate to the 1.5 volt level.

MINIMUM READ BUS CYCLE TIMING DIAGRAM



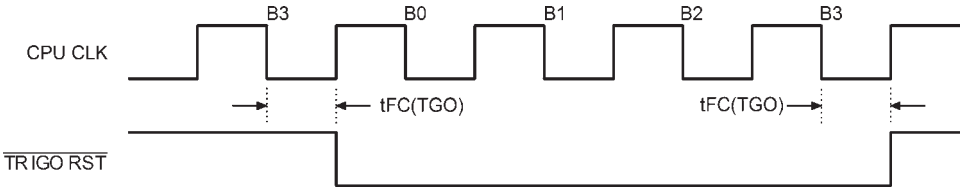
Note:
All time measurements on active signals relate to the 1.5 volt level.

MINIMUM WRITE BUS CYCLE, FOLLOWED BY A NON-BUS CYCLE, TIMING DIAGRAM

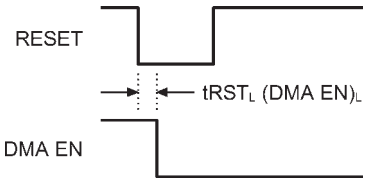


Note:
All time measurements on active signals relate to the 1.5 volt level.

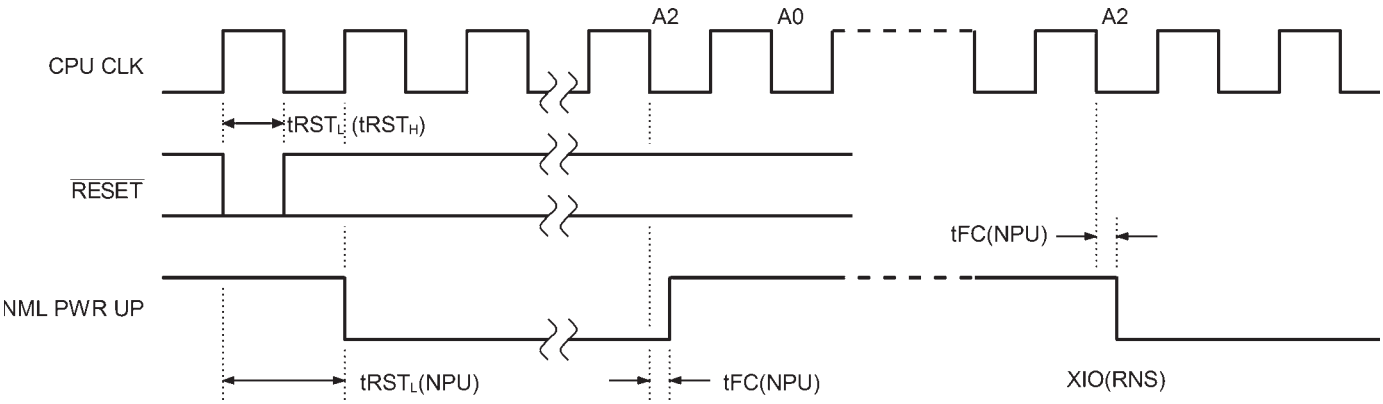
$\overline{\text{TRIGO RST}}$ DISCRETE TIMING DIAGRAM



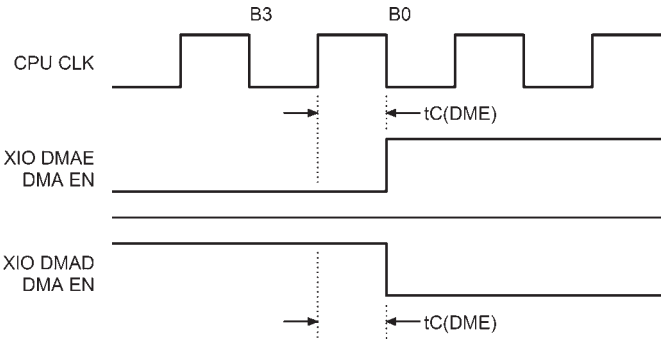
DMA EN DISCRETE TIMING DIAGRAM



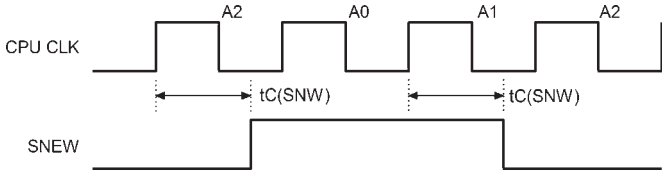
NORMAL POWER UP DISCRETE TIMING DIAGRAM



XIO OPERATIONS



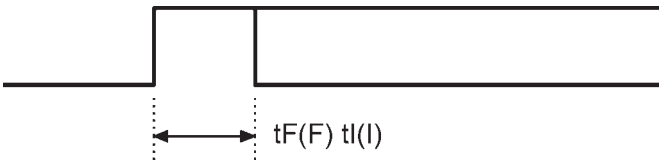
SNEW DISCRETE TIMING DIAGRAM



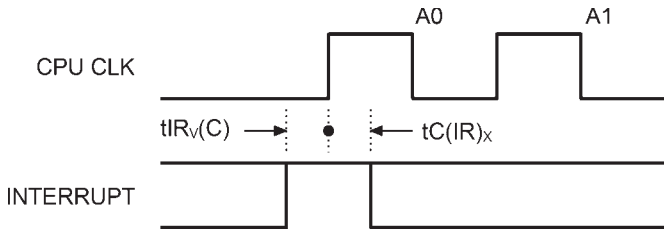
Note:
All time measurements on active signals relate to the 1.5 volt level.

EXTERNAL FAULTS AND INTERRUPTS TIMING DIAGRAM

Edge-sensitive interrupts and faults ($SYSFLT_0$, $SYSFLT_1$) min. pulse width

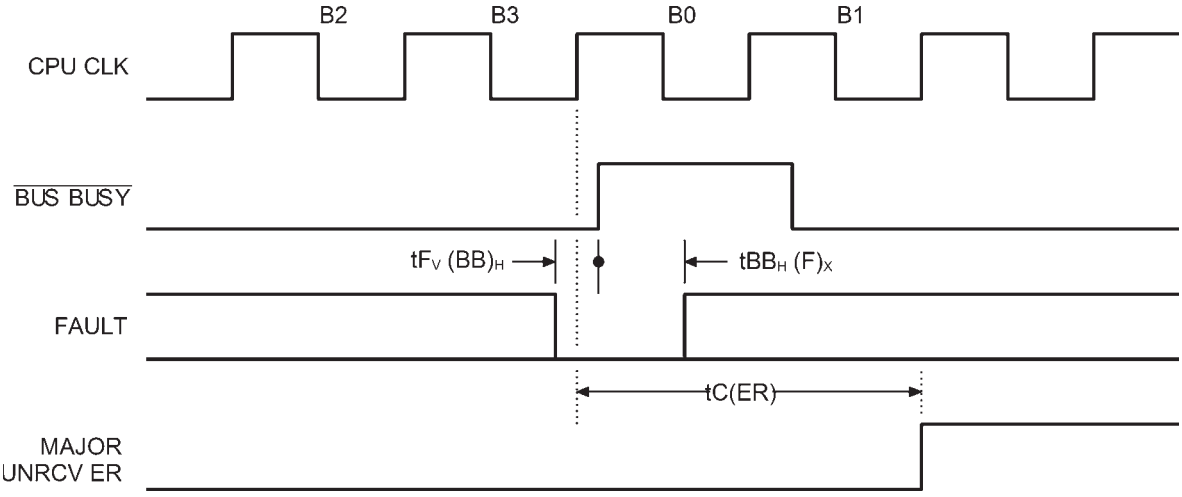


Level-sensitive interrupts

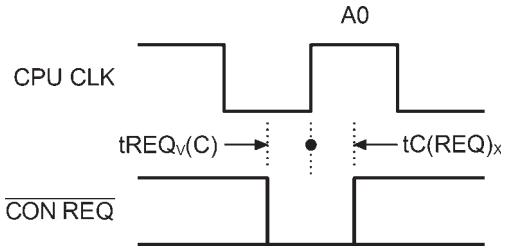


Note:
$tC(IR)_X$ max = 35 clocks

Level-sensitive faults

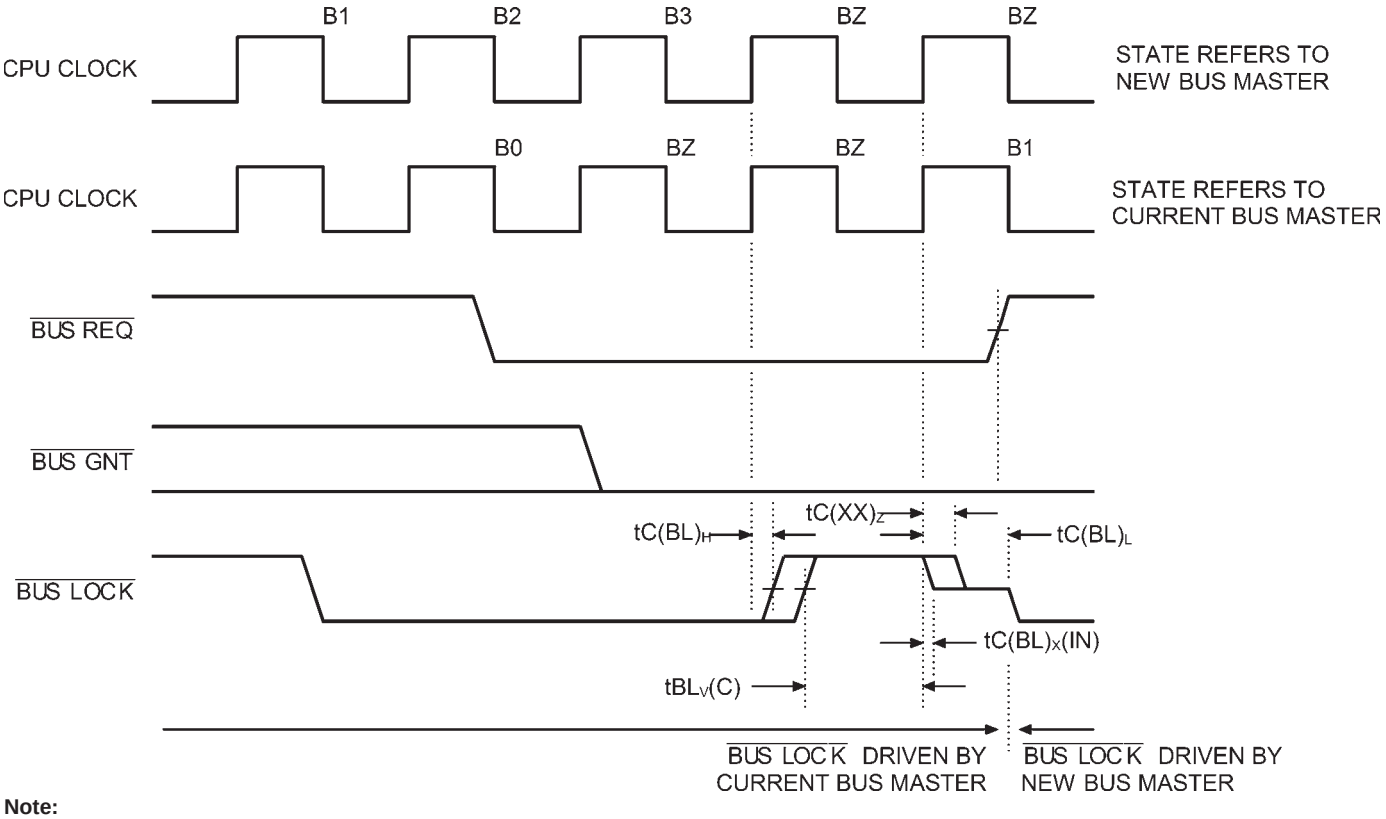


$\overline{\text{CON REQ}}$



Note:
All time measurements on active signals relate to the 1.5 volt level.

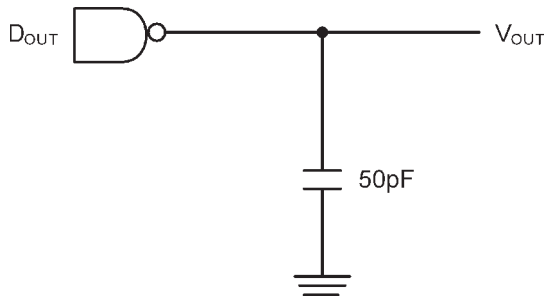
BUS ACQUISITION



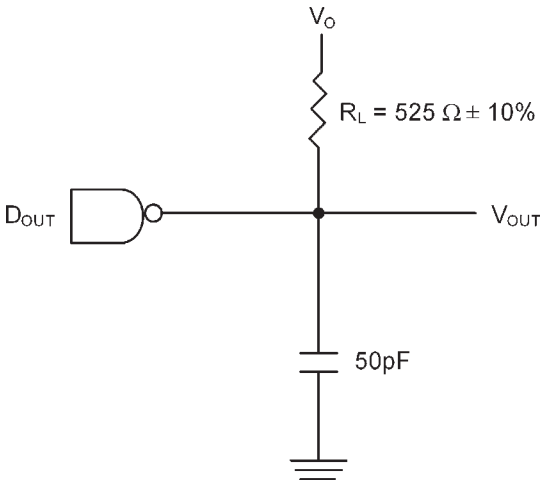
Note:
A CPU contending for the BUS will assert the $\overline{\text{BUS REQ}}$ line, and will acquire it when $\overline{\text{BUS GNT}}$ is assserted and the BUS is not locked ($\overline{\text{BUS LOCK}}$ is high).

SWITCHING TIME TEST CIRCUITS

Standard Output (Non-Three-State)



Three-State



Note:
All time measurements on active signals relate to the 1.5 volt level.

Parameter	V0	VMEA
t_{PLZ}	≥ 3V	0.5V
t_{PHZ}	0V	V_{CC} – 0.5V
t_{PXL}	$V_{CC}/2$	1.5V
t_{PXH}	$V_{CC}/2$	1.5V

SIGNAL DESCRIPTIONS

CLOCKS AND EXTERNAL REQUESTS

Mnemonic	Name	Description
CPU CLK	CPU clock	A single phase input clock signal (0-40 MHz, 40 percent to 60 percent duty cycle.
TIMER CLK	Timer clock	A 100 KHz input that, after synchronization with CPU CLK, provides the clock for timer A and timer B. If timers are used, the CPU CLK signal frequency must be > 300 KHz.
$\overline{\text{RESET}}$	Reset	An active LOW input that initializes the device.
$\overline{\text{CON REQ}}$	Console request	An active LOW input that initiates console operations after completion of the current instruction.

INTERRUPT INPUTS

Mnemonic	Name	Description
PWRDN INT	Power down interrupt	An interrupt request input that cannot be masked or disabled. This signal is active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register.
USR_0INT - USR_5INT	User interrupt	Interrupt request input signals that are active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register.
IOL_1INT - IOL_2INT	I/O level interrupts	Active HIGH interrupt request inputs that can be used to expand the number of user interrupts.

FAULTS

Mnemonic	Name	Description
$\overline{\text{MEM PRT ER}}$	Memory protect error	An active LOW input generated by the MMU or BPU, or both and sampled by the $\overline{\text{BUS BUSY}}$ signal into the Fault Register (bit 0 CPU bus cycle, bit 1 if non-CPU bus cycle).
$\overline{\text{MEM PAR ER}}$	Memory parity error	An active LOW input sampled by the $\overline{\text{BUS BUSY}}$ signal into bit 2 of the fault register.
$\overline{\text{EXT ADR ER}}$	External address error	An active LOW input sampled by the $\overline{\text{BUS BUSY}}$ signal into the Fault register (bit 5 or 8), depending on the cycle (memory or I/O).
$SYSFLT_0$ $SYSFLT_1$	System fault $_0$, System fault $_1$,	Asynchronous, positive edge-sensitive inputs that set bit 7 ($SYSFLT_0$) or bits 13 and 15 ($SYSFLT_1$) in the Fault register.

ERROR CONTROL

Mnemonic	Name	Description
UNRCV ER	Unrecoverable error	An active HIGH output that indicates the occurrence of an error classified as unrecoverable.
MAJ ER	Major error	An active HIGH output that indicates the occurrence of an error classified as major.

SIGNAL DESCRIPTIONS (Continued)

BUS CONTROL

Mnemonic	Name	Description
D/$\overline{I}$	Data or instruction	An output signal that indicates whether the current bus cycle access is for Data (HIGH) or Instruction (LOW). It is three-state during bus cycles not assigned to the CPU. This line can be used as an additional memory address bit for systems that require separate data and program memory.
R/$\overline{W}$	Read or write	An output signal that indicates direction of data flow with respect to the current bus master. A HIGH indicates a read or input operation and a LOW indicates a write or output operation. The signal is three-state during bus cycles not assigned to the CPU.
M/$\overline{IO}$	Memory or I/O	An output signal that indicates whether the current bus cycle is memory (HIGH) or I/O (LOW). This signal is three-state during bus cycles not assigned to the CPU.
STRBA	Address strobe	An active HIGH output that can be used to externally latch the memory or I/O address at the HIGH-to-LOW transition of the strobe. The signal is three-state during bus cycles not assigned to the CPU.
RDYA	Address ready	An active HIGH input that can be used to extend the address phase of a bus cycle. When RDYA is not active, wait states are inserted by the device to accommodate slower memory or I/O devices.
$\overline{STRBD}$	Data strobe	An active LOW output that can be used to strobe data in memory and XIO cycles. This signal is three-state during bus cycles not assigned to the CPU.
RDYD	Data ready	An active HIGH input that extends the data phase of a bus cycle. When RDYD is not active, wait states are inserted by the device to accommodate slower memory or I/O devlces.

INFORMATION BUS

Mnemonic	Name	Description
IB_0 - IB_{15}	Information bus	A bidirectional time-multiplexed address/data bus that is three-state during bus cycles not assigned to the CPU. IB_0 is the most significant bit.

STATUS BUS

Mnemonic	Name	Description
AK_0 - AK_3	Access key	Outputs used to match the access lock in the MMU for memory accesses (a mismatch will cause the MMU to pull the $\overline{MEM\ PRT\ ER}$ signal LOW), and also indicates processor state (PS). Privileged instructions can be executed with PS = 0 only. These signals are three-state during bus cycles not assigned to the CPU.
AS_0 - AS_3	Address state	Outputs that select the page register group in the MMU. It is three-state during bus cycles not assigned to the CPU. [These outputs together with D/$\overline{I}$ can be used to expand the device direct addressing space to 4 MBytes, in a nonprotected mode (no MMU)]. However, using this addressing mode may produce situations not specified in MIL-STD-1750.

SIGNAL DESCRIPTIONS (Continued)

BUS ARBITRATION

Mnemonic	Name	Description
$\overline{\text{BUS REQ}}$	Bus request	An active LOW output that indicates the CPU requires the bus. It becomes inactive when the CPU has acquired the bus and started the bus cycle.
$\overline{\text{BUS GNT}}$	Bus grant	An active LOW input from an external arbiter that indicates the CPU currently has the highest priority bus request. If the bus is not used and not locked, the CPU may begin a bus cycle, commencing with the next CPU clock. A HIGH level will hold the CPU in Hi-Z state (Bz), three-stating the IB bus status lines (D/$\overline{\text{I}}$, R/$\overline{\text{W}}$, M/$\overline{\text{IO}}$), strobes (STRBA, $\overline{\text{STRBD}}$), and all the other lines that go three-state when this CPU does not have the bus.
$\overline{\text{BUS BUSY}}$	Bus busy	An active LOW, bidirectional signal used to establish the beginning and end of a bus cycle. The trailing edge (LOW-to-HIGH transition) is used for sampling bits into the fault register. It is three-state in bus cycles not assigned to this CPU. However, the CPU monitors the $\overline{\text{BUS BUSY}}$ line for latching non-CPU bus cycle faults into the fault register.
$\overline{\text{BUS LOCK}}$	Bus lock	An active low, bi-directional signal used to lock the bus for successive bus cycles. During non-locked bus cycles, the $\overline{\text{BUS LOCK}}$ signal mimics the $\overline{\text{BUS BUSY}}$ signal. It is three-state during bus cycles not assigned to the CPU. The following instructions will lock the bus: INCM, DECM, SB, RB, TSB, SRM, STUB and STLB.

DISCRETE CONTROL

Mnemonic	Name	Description
DMA EN	Direct memory Access enable	An active HIGH output that indicates the DMA is enabled. It is disabled when the CPU is initialized (reset) and can be enabled or disabled under program control (I/O commands DMAE, DMAD).
NML PWRUP	Normal power up	An active HIGH output that is set when the CPU has successfully completed the built-in self test in the initialization sequence. It can be reset by the I/O command RNS.
SNEW	Start new	An active HIGH output that indicates a new instruction is about to start executing in the next cycle.
$\overline{\text{TRIGO RST}}$	Trigger-go reset	An active LOW discrete output. This signal can be pulsed low under program control I/O address 400B (Hex) and is automatically pulsed during processor initialization.

TERMINAL CONNECTIONS

Case Outline: Pin Grid Array (Case Z)

Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
B1	V_{CC}	L5	DMA EN	D11	AS_1
B2	IB_{14}	K5	$\overline{\text{CON REQ}}$	D10	AS_2
C1	IB_{13}	L6	V_{CC}	C11	AS_3
C2	IB_{12}	K6	SNEW	C10	IOL_2INT
D1	IB_{11}	L7	$\overline{\text{BUS LOCK}}$	B11	V_{CC}
D2	IB_{10}	K7	$\overline{\text{BUS GNT}}$	A10	GND
E1	IB_9	L8	$\overline{\text{BUS BUSY}}$	B10	IOL_1INT
E2	IB_8	K8	M/$\overline{\text{IO}}$	A9	USR_5INT
F1	GND	L9	D/$\overline{\text{I}}$	B9	USR_4INT
F2	IB_7	K9	R/$\overline{\text{W}}$	A8	USR_3INT
G1	IB_6	L10	GND	B8	USR_2INT
G2	IB_5	K11	RDYD	A7	USR_1INT
H1	IB_4	K10	RDYA	B7	USR_0INT
H2	IB_3	J11	$\overline{\text{BUS REQ}}$	A6	PWRDN INT
J1	IB_2	J10	$\overline{\text{STRBD}}$	B6	GND
J2	IB_1	H11	STRBA	A5	MAJ ER
K1	IB_0	H10	CPU CLK	B5	$SYSFLT_1$
L2	GND	G11	AK_0	A4	$SYSFLT_0$
K2	UNRCV ER	G10	AK_1	B4	$\overline{\text{EXT ADR ER}}$
L3	TIMER CLK	F11	AK_2	A3	$\overline{\text{MEM PAR ER}}$
K3	NML PWRUP	F10	AK_3	B3	$\overline{\text{MEM PRT ER}}$
L4	$\overline{\text{RESET}}$	E11	GND	A2	IB_{15}
K4	$\overline{\text{TRIGO RST}}$	E10	AS_0		

TERMINAL CONNECTIONS

Case Outlines: Leaded Chip Carrier with unformed leads (Case U) and Leaded Chip Carrier with Gull-Wing Leads (Case Y)

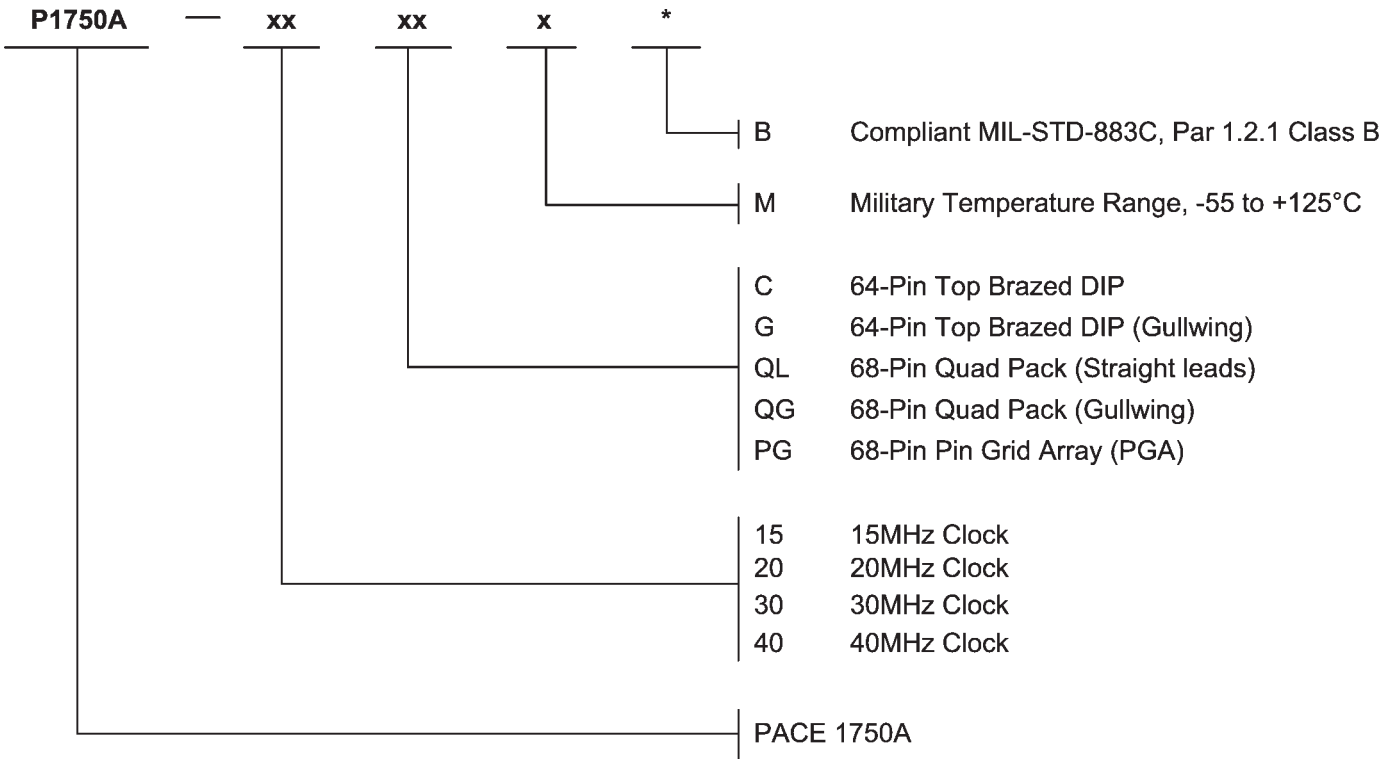
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	23	IB_{11}	46	AS_2
2	$\overline{\text{CON REQ}}$	24	IB_{12}	47	AS_1
3	DMA EN	25	IB_{13}	48	AS_0
4	$\overline{\text{TRIGO RST}}$	26	IB_{14}	49	GND
5	$\overline{\text{RESET}}$	27	IB_{15}	50	AK_3
6	NML PWRUP	28	$\overline{\text{MEM PRT ER}}$	51	AK_2
7	TIMER CLK	29	$\overline{\text{MEM PAR ER}}$	52	VCC
8	UNRCV ER	30	$\overline{\text{EXT ADR ER}}$	53	AK_1
9	GND	31	$SYSFLT_0$	54	AK_0
10	IB_0	32	$SYSFLT_1$	55	CPU CLK
11	IB_1	33	MAJ ER	56	STRBA
12	IB_2	34	GND	57	$\overline{\text{STRBD}}$
13	IB_3	35	VCC	58	$\overline{\text{BUS REQ}}$
14	IB_4	36	PWRDN INT	59	RDYA
15	IB_5	37	USR_0INT	60	RDYD
16	IB_6	38	USR_1INT	61	R/$\overline{W}$
17	IB_7	39	USR_2INT	62	D/$\overline{I}$
18	GND	40	USR_3INT	63	M/$\overline{IO}$
19	IB_8	41	USR_4INT	64	$\overline{\text{BUS BUSY}}$
20	IB_9	42	USR_5INT	65	$\overline{\text{BUS GNT}}$
21	VCC	43	IOL_1INT	66	$\overline{\text{BUS LOCK}}$
22	IB_{10}	44	IOL_2INT	67	SNEW
		45	AS_3	68	VCC

TERMINAL CONNECTIONS

Case Outlines: Dual-In-Line (Case X) and Dual-In-Line with Gull-Wing Leads (Case T)					
Terminal Number	**Terminal Symbol**	**Terminal Number**	**Terminal Symbol**	**Terminal Number**	**Terminal Symbol**
1	GND	23	IB_{13}	44	AS_1
2	$\overline{\text{CON REQ}}$	24	IB_{14}	45	AS_0
3	DMA EN	25	IB_{15}	46	GND
4	$\overline{\text{TRIGO RST}}$	26	$\overline{\text{MEM PRT ER}}$	47	AK_3
5	$\overline{\text{RESET}}$	27	$\overline{\text{MEM PAR ER}}$	48	AK_2
6	NML PWRUP	28	$\overline{\text{EXT ADR ER}}$	49	AK_1
7	TIMER CLK	29	$SYSFLT_0$	50	AK_0
8	UNRCV ER	30	$SYSFLT_1$	51	CPU CLK
9	IB_0	31	MAJ ER	52	STRBA
10	IB_1	32	GND	53	$\overline{\text{STRBD}}$
11	IB_2	33	PWRDN INT	54	$\overline{\text{BUS REQ}}$
12	IB_3	34	USR_0INT	55	RDYA
13	IB_4	35	USR_1INT	56	RDYD
14	IB_5	36	USR_2INT	57	R/$\overline{W}$
15	IB_6	37	USR_3INT	58	D/$\overline{I}$
16	IB_7	38	USR_4INT	59	M/$\overline{IO}$
17	IB_8	39	USR_5INT	60	$\overline{\text{BUS BUSY}}$
18	IB_9	40	IOL_1INT	61	$\overline{\text{BUS GNT}}$
19	VCC	41	IOL_2INT	62	$\overline{\text{BUS LOCK}}$
20	IB_{10}	42	AS_3	63	SNEW
21	IB_{11}	43	AS_2	64	VCC
22	IB_{12}				

Note: For the 30 MHz and 40 MHz devices, Pins 19 and 46 are connected as shown. For the 15 MHz and 20 MHz devices, these pins are not internally connected to the die.

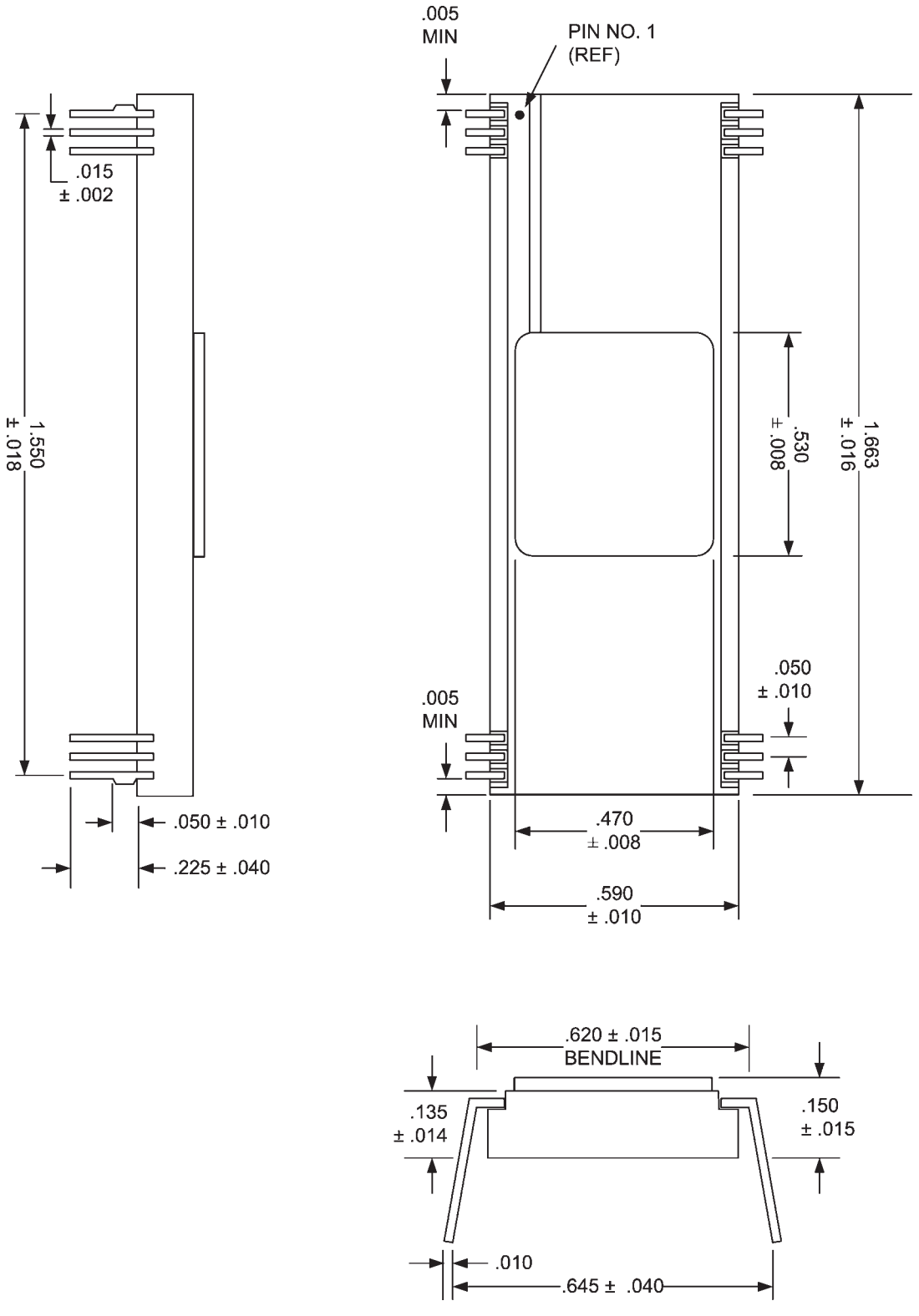
ORDERING INFORMATION



Standardized Military Drawing Part Number	Pyramid Semiconductor CAGE Number	Pyramid Semiconductor Part Number
5962-8766501TX	3DTT2	P1750A-15GMB
5962-8766501UX	3DTT2	P1750A-15QLMB
5962-8766501XX	3DTT2	P1750A-15CMB
5962-8766501YX	3DTT2	P1750A-15QGMB
5962-8766501ZX	3DTT2	P1750A-15PGMB
5962-8766502TX	3DTT2	P1750A-20GMB
5962-8766502UX	3DTT2	P1750A-20QLMB
5962-8766502XX	3DTT2	P1750A-20CMB
5962-8766502YX	3DTT2	P1750A-20QGMB
5962-8766502ZX	3DTT2	P1750A-20PGMB
5962-8766503TX	3DTT2	P1750A-30GMB
5962-8766503UX	3DTT2	P1750A-30QLMB
5962-8766503XX	3DTT2	P1750A-30CMB
5962-8766503YX	3DTT2	P1750A-30QGMB
5962-8766503ZX	3DTT2	P1750A-30PGMB
5962-8766504TX	3DTT2	P1750A-40GMB
5962-8766504UX	3DTT2	P1750A-40QLMB
5962-8766504XX	3DTT2	P1750A-40CMB
5962-8766504YX	3DTT2	P1750A-40QGMB
5962-8766504ZX	3DTT2	P1750A-40PGMB

CASE OUTLINE X:

64 Lead Top Brazed DIP Package, Straight Lead Version (Ordering Code C)



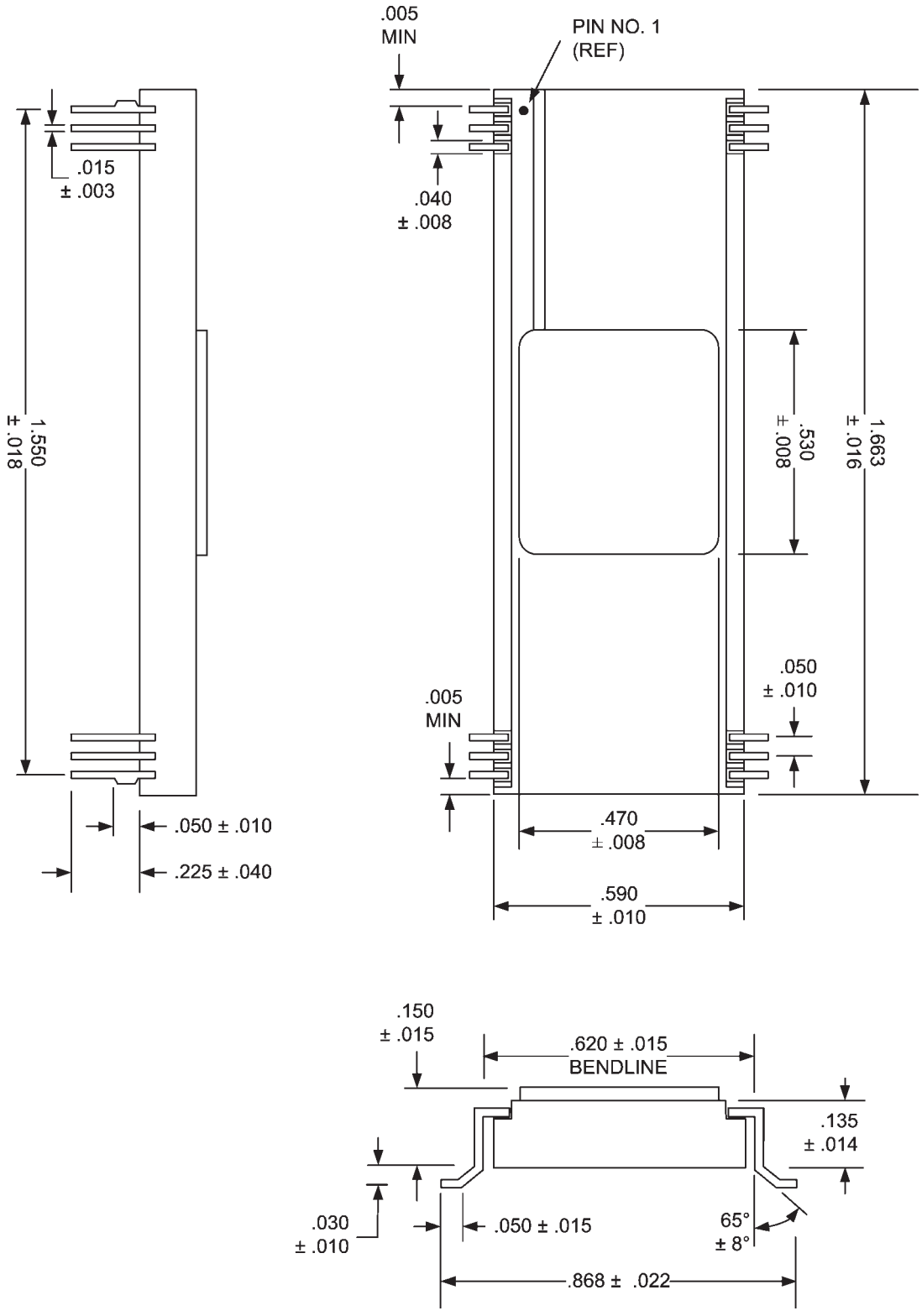
Inches	mm
.002	0.05
.005	0.12
.008	0.20
.010	0.25
.015	0.38
.016	0.40
.018	0.45
.025	0.63
.040	1.01
.050	1.27
.185	4.70
.265	6.73
.470	11.93
.530	13.46
.590	14.98
.620	15.74
.645	16.38
1.550	39.37
1.563	39.70

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.

CASE OUTLINE T:

64 Lead Top Brazed DIP Package, Gullwing Lead Version (Ordering Code G)



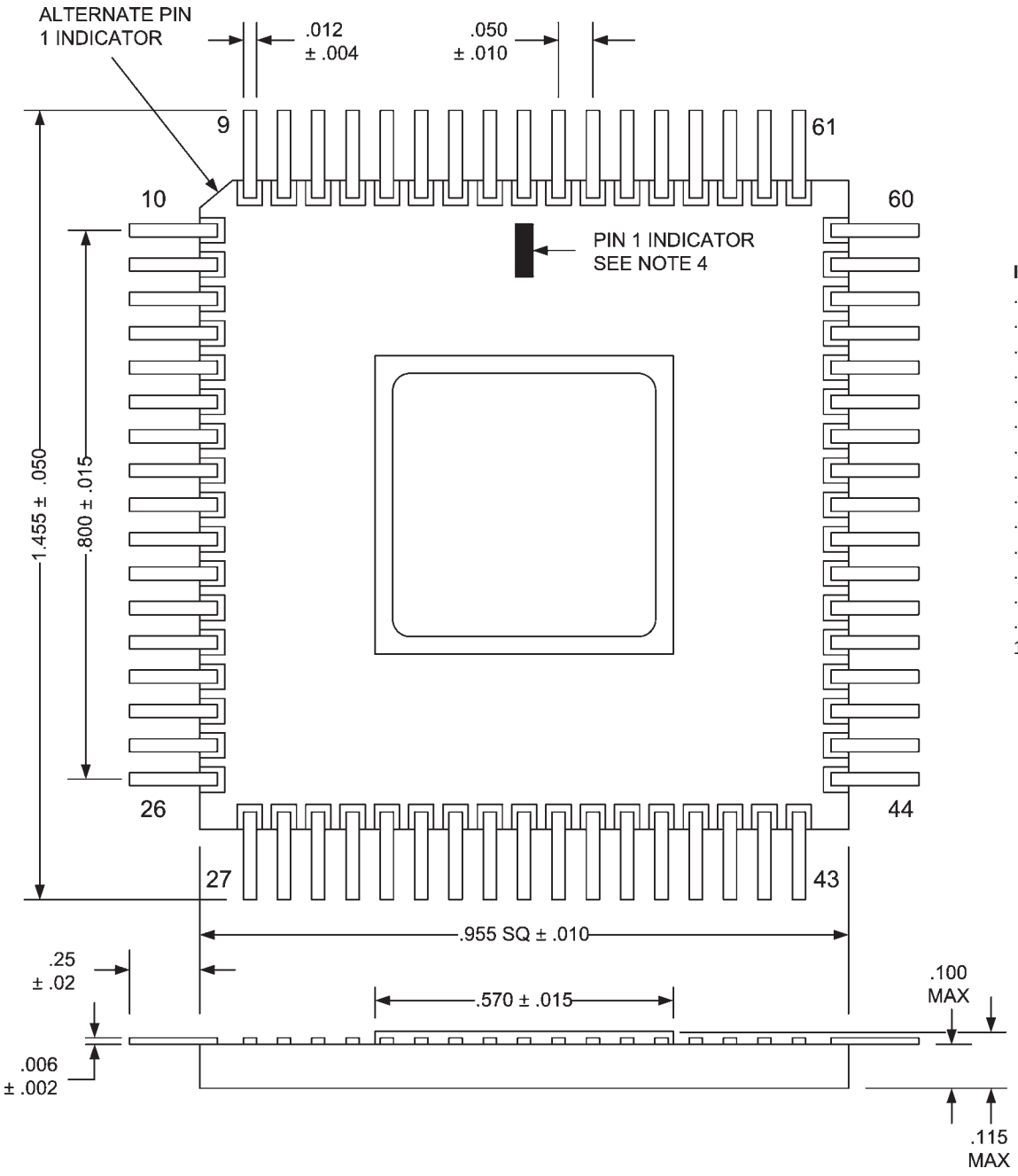
Inches	mm
.001	0.03
.003	0.08
.005	0.12
.008	0.20
.010	0.25
.015	0.38
.016	0.41
.022	0.55
.030	0.76
.040	1.01
.050	1.27
.150	3.81
.470	11.93
.530	13.46
.590	14.98
.620	15.74
.868	22.04
1.663	42.24

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Case T is derived from Case X by forming the leads to the shown gullwing configuration.

CASE OUTLINE U:

68 Lead Quad Pack with Straight Leads (Ordering Code QL)



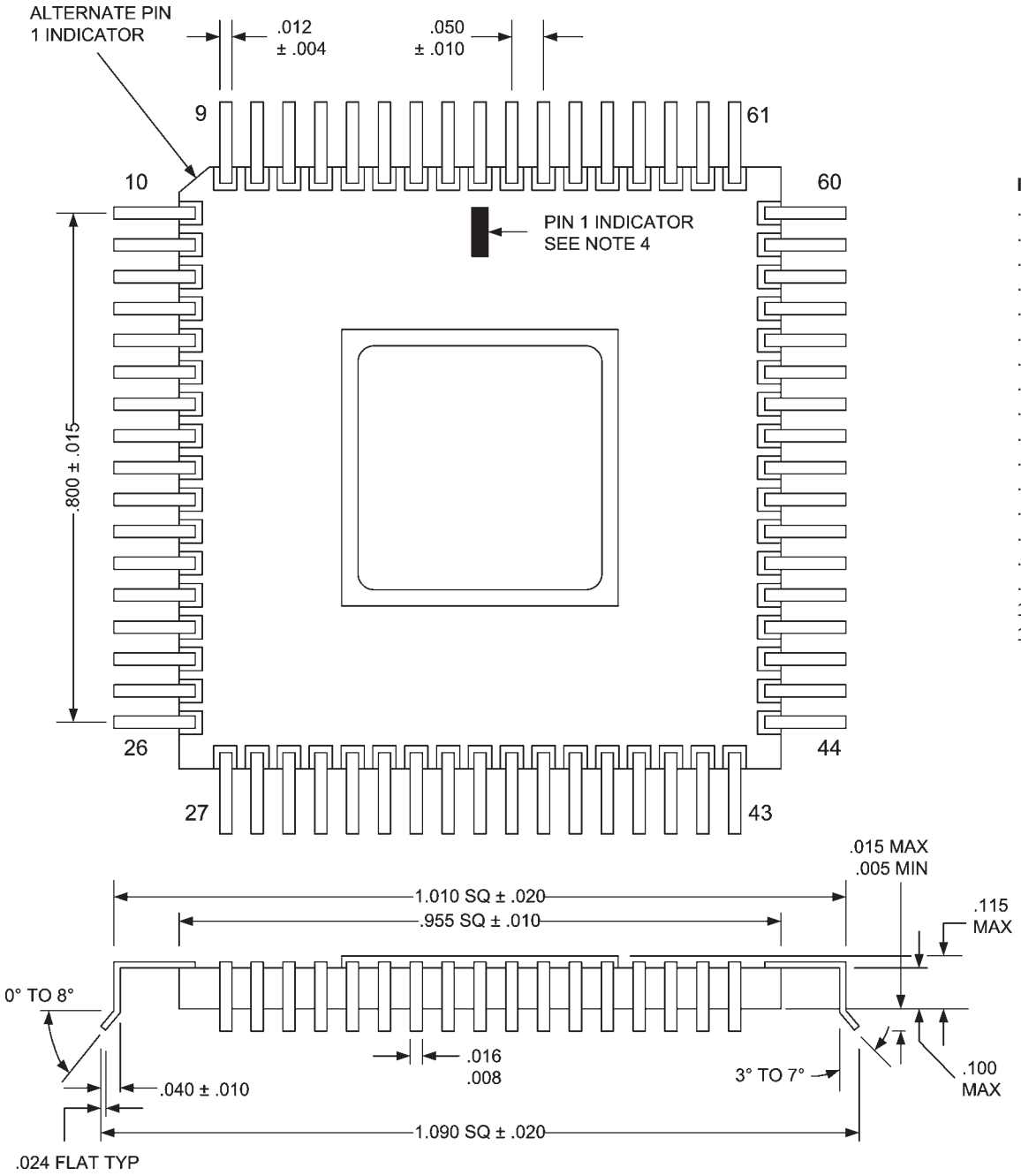
Inches	mm
.002	0.05
.004	0.10
.006	0.15
.010	0.25
.012	0.30
.020	0.51
.050	1.27
.100	2.54
.116	2.95
.250	6.40
.560	14.22
.570	14.48
.800	20.32
.955	24.25
1.090	27.69

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Pin 1 indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5) Corners indicated as notched may be either notched or square.

CASE OUTLINE Y:

68 Lead Quad Pack with Gullwing Leads (Ordering Code QG)



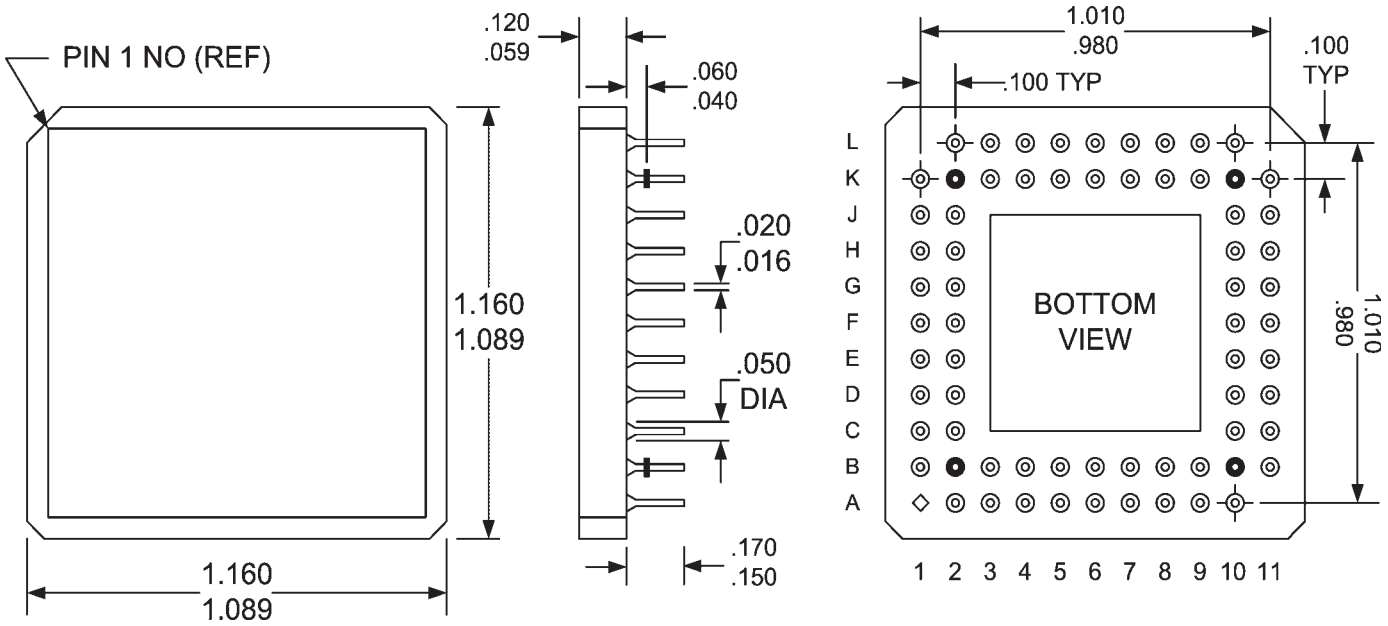
Inches	mm
.004	0.10
.005	0.12
.008	0.20
.010	0.25
.012	0.30
.015	0.38
.016	0.41
.020	0.50
.024	0.60
.040	1.02
.050	1.27
.100	2.54
.115	2.92
.570	14.48
.800	20.32
.955	24.25
1.010	25.65
1.090	27.68

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Pin 1 indicator can either be rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.
5) Corners indicated as notched my be either notched or square (with radius).
6) Case Y is derived from Case U by forming the leads to the shown gullwing configuration.

CASE OUTLINE Z:

68-Pin Pin Grid Array (PGA) (Ordering Code PG)



Inches	mm
.016	0.41
.020	0.50
.040	1.01
.050	1.27
.059	1.49
.060	1.52
.098	2.49
.100	2.54
.120	3.04
.150	3.81
.170	4.32
1.010	25.65
1.089	27.66
1.160	29.46

NOTES:

1) Dimensions are in inches.
2) Metric equivalents are given for general information only.
3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.
4) Corners except pin number 1 (ref.) can be either rounded or square.
5) All pins must be on the .100" grid.

REVISIONS

DOCUMENT NUMBER: MICRO-3 **DOCUMENT TITLE**: PACE1750A CMOS 16-BIT PROCESSOR			
REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
ORIG	May-89	RKK	New Data Sheet
A	Jul-04	JDB	Added Pyramid logo
B	Aug-05	JDB	Re-created electronic version
C	Oct-05	JDB	Altered case outline drawing for case X and case T