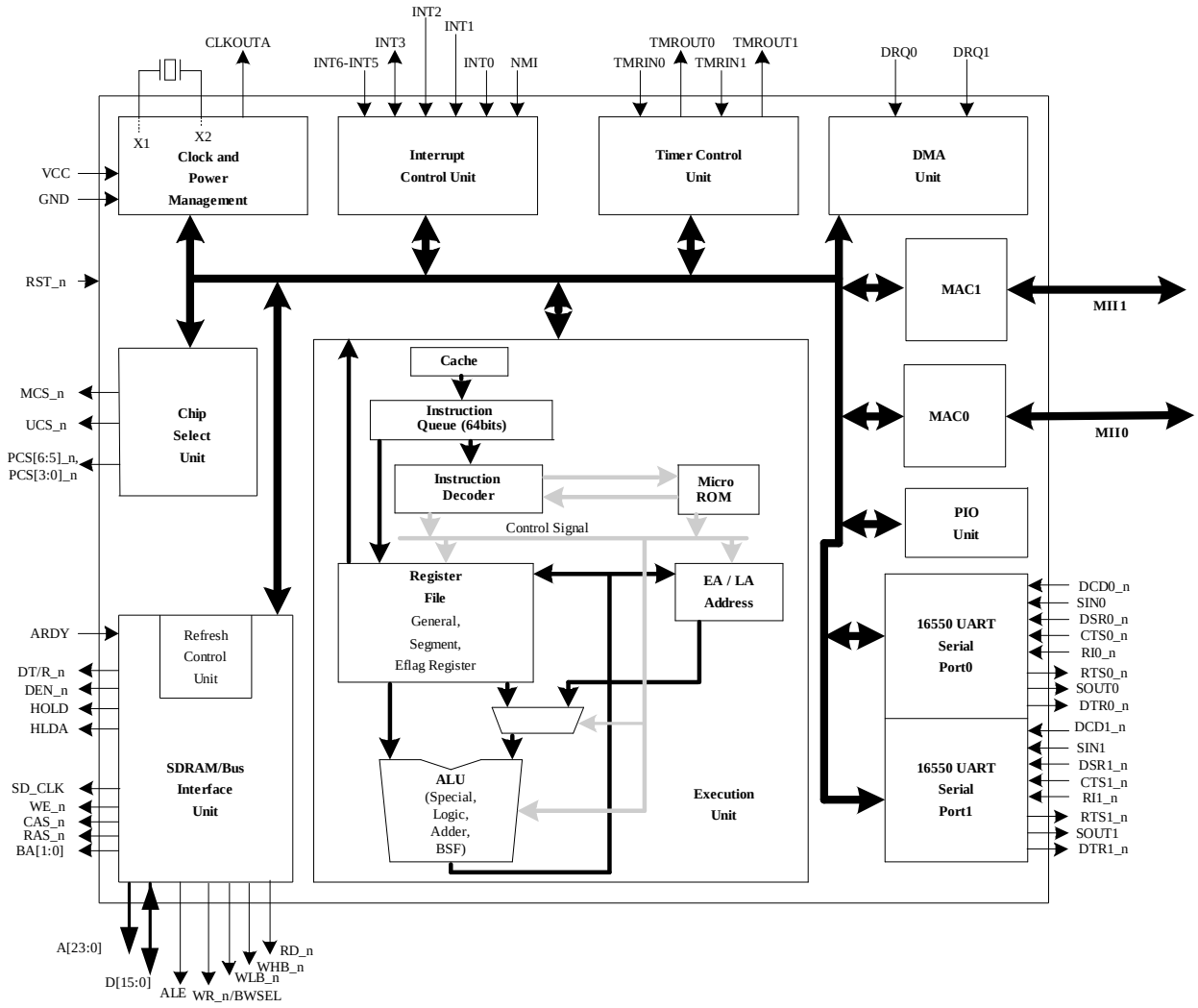
R2020
Brief Sheet
FAST ETHERNET RISC PROCESSOR

1. Features

- Five-stage pipeline
- RISC architecture
- Bus interface
  - Multiplexed address and Data bus
  - Supports non-multiplexed address bus A[23:0]
  - 8-bit or 16-bit external bus dynamic access
  - 16M-byte memory address space
  - 64K-byte I/O space
  - Supports an independent data/address bus for external I/O device
- Supports two compatible UART serial channels with 16-byte FIFO and hardware flow-control.
- Supports CPU ID
- Supports a glueless and simplified 16-bit PCMCIA bus interface
- Supports 32 PIO pins
- SDRAM control Interface
- Three independent 16-bit timers and one independent programmable watchdog timer
- The Interrupt controller with six maskable external interrupts and two non-maskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable wait-state generator
- With 8-bit or 16-bit Boot ROM bus size
- 2-Port Fast Ethernet MAC with MII interface
- Supports an 8K-byte Uniform cache
- With 25MHz input frequency and up to 100MHz maximum internal frequency.
- Compatible with 3.3V I/O and 2.5V core voltage.
- Package Type includes 160-pin PQFP.

2. Block Diagram



3. Package Information

PQFP 160 pins