

SNx5ALS180 Differential Driver and Receiver Pairs

1 Features

- Meet or exceed the requirements of TIA/EIA-422-B, TIA/EIA-485-A¹ and ITU recommendation V.11
- High-speed advanced low-power Schottky circuitry
- Designed for 25-Mbaud operation in both serial and parallel applications
- Low skew between devices: 6 ns max
- Low supply-current requirements: 30 mA max
- Individual driver and receiver I/O pins with dual V_{CC} and dual GND
- Wide positive and negative input/output bus voltage ranges
- Driver output capacity: ±60 mA
- Thermal shutdown protection
- Driver positive- and negative-current limiting
- Receiver input impedance: 12 kΩ min
- Receiver input sensitivity: ±200 mV max
- Receiver input hysteresis: 60 mV typ
- Operate from a single 5-V supply
- Glitch-free power-up and power-down protection

2 Description

The SN65ALS180 and SN75ALS180 differential driver and receiver pairs are integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. The devices are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

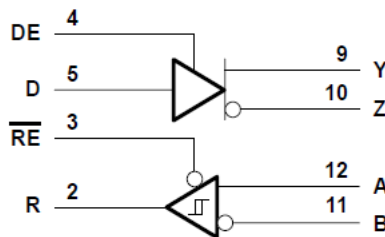
The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

These ports feature wide positive and negative common-mode voltage ranges, making the device an excellent choice for party-line applications.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SNx5ALS176	D (SOIC)	8.65 mm x 3.91 mm
	N (PDIP)	19.3 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

¹ These devices meet or exceed the requirements of TIA/EIA-485-A, except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are –6 V to 8 V for the SN75ALS180 and –4 V to 8 V for the SN65ALS180.



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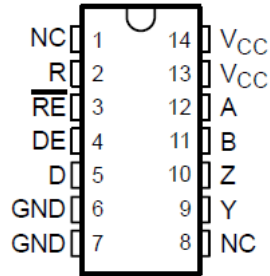
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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2003) to Revision H (January 2023)	Page
• Changed the document to the latest TI format.....	1
• Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i>	4
• Added the <i>Thermal Information</i> table.....	4
• Changed the <i>Typical Characteristics</i> graphs.....	8

4 Pin Configuration and Functions



NC – No internal connection

**Figure 4-1. SN65ALS180 D Package
SN75ALS180 D or N Package
(Top View)**

Table 4-1. Pin Functions

NO	Name	Type	Description
1	NC	-	No Internal connection
2	R	O	Receive data output
3	\overline{RE}	I	Receiver enable, active low
4	DE	I	Driver enable, active high
5	D	I	Driver data input
6, 7	GND	GND	Device ground
8	NC	-	No Internal connection
9	Y	O	Digital bus output, Y (Complementary to Z)
10	Z	O	Digital bus output, Z (Complementary to Y)
11	A	I	Bus input, A (complementary to B)
12	B	I	Bus input, B (complementary to A)
13, 14	V _{CC}	SUPPLY	4.75V to 5.25V supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		7	V
	Voltage range at any bus terminal	-10	15	V
V _I	Enable input voltage		5.5	V
T _J	Operating virtual junction temperature		150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _I or V _{IC}	Voltage at any bus terminal (separately or common mode)			12 -7	V
V _{IH}	High-level input voltage	D, DE, and RE		2	V
V _{IL}	Low-level input voltage	D, DE, and RE		0.8	V
V _{ID}	Differential input voltage ⁽¹⁾			±12	V
I _{OH}	High-level output current	Driver		-60	mA
		Receiver		-400	µA
I _{OL}	Low-level output current	Driver		60	mA
		Receiver		8	
T _A	Operating free-air temperature	SN65ALS180		-40	°C
		SN75ALS180		0	

- (1) Differential-input/output bus voltage is measured at the noninverting terminal, A/Y, with respect to the inverting terminal, B/Z.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		N (PDIP)	D (SOIC) (SN65 Devices)	D (SOIC) (SN75 Devices)	UNIT
		14-Pins	14-Pins	14-Pins	
R _{θJA}	Junction-to-ambient thermal resistance	53.4	93.2	83.7	°C/W
R _{θJC(top)}	Junction-to-case thermal resistance	40	47.5	39.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	33.3	49.4	39.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1	11.2	7.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	33	48.9	39.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT	
V _{IK}	Input clamp voltage	I _I = -18 mA				-1.5	V	
V _O	Output voltage	I _O = 0		0		6	V	
V _{OD1}	Differential output voltage	I _O = 0		1.5		6	V	
V _{OD2}	Differential output voltage	R _L = 100 Ω	See Figure 6-1	1/2V _{OD1} or 2 ⁽³⁾			V	
		R _L = 54 Ω	See Figure 6-1	1.5	2.5	5		
V _{OD3}	Differential output voltage	V _{test} = -7 V to 12 V,	See Figure 6-2	1.5		5	V	
Δ V _{OD}	Change in magnitude of differential output voltage ⁽⁴⁾	R _L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V	
V _{OCC}	Common-mode output voltage	R _L = 54 Ω or 100 Ω	See Figure 6-1			3 -1	V	
Δ V _{OCC}	Change in magnitude of common-mode output voltage ⁽⁴⁾	R _L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V	
I _O	Output current	Output disabled ⁽⁶⁾		V _O = 12 V		1	mA	
				V _O = -7 V		-0.8		
I _{IH}	High-level input current	V _I = 2.4 V				20	μA	
I _{IL}	Low-level input current	V _I = 0.4 V				-400	μA	
I _{OS}	Short-circuit output current ⁽⁵⁾	V _O = -6 V	SN75ALS180			-250	mA	
		V _O = -4 V	SN65ALS180			-250		
		V _O = 0	All			-150		
		V _O = V _{CC}	All			250		
		V _O = 8 V	All			250		
I _{CC}	Supply current	No load		Driver outputs enabled, Receiver disabled		25	30	mA
				Outputs disabled		19	26	

- (1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
- (2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
- (3) The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
- (4) Δ|V_{OD}| and Δ|V_{OCC}| are the changes in magnitude of V_{OD} and V_{OCC}, respectively, that occur when the input is changed from a high level to a low level.
- (5) Duration of the short circuit should not exceed one second for this test.
- (6) This applies for both power on and off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
t _{d(OD)}	Differential output delay time	R _L = 54 Ω	C _L = 50 pF,	See Figure 6-3	3	8	13	ns
	Pulse skew (t _{d(ODH)} - t _{d(ODL)})	R _L = 54 Ω	C _L = 50 pF,	See Figure 6-3		1	6	ns
t _{t(OD)}	Differential output transition time	R _L = 54 Ω	C _L = 50 pF,	See Figure 6-3	3	8	13	ns
t _{PZH}	Output enable time to high level	R _L = 110 Ω	See Figure 6-4			23	50	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω	See Figure 6-5			19	24	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω	See Figure 6-4			8	13	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω	See Figure 6-5			8	13	ns

- (1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.6 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$ V_{OD1} $	V_o	V_o
$ V_{OD2} $	$V_t(R_L = 100 \Omega)$	$V_t(R_L = 54 \Omega)$
$ V_{OD3} $		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta V_{OD} $	$ V_t - V_t $	$ V_t - V_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os-} - V_{os} $	$ V_{os-} - V_{os} $
I_{os}	$ I_{sa} , I_{sb} $	
I_o	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

5.7 Electrical Characteristics - Receivers

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$V_O = 2.7\text{ V}$,	$I_O = -0.4\text{ mA}$				0.2	V
V_{IT-}	Negative-going input threshold voltage	$V_O = 0.5\text{ V}$,	$I_O = 8\text{ mA}$		-0.2 ⁽²⁾			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					60		mV
V_{IK}	Enable-input clamp voltage	$I_I = -18\text{ mA}$					-1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200\text{ mV}$,	$I_{OH} = -400\text{ }\mu\text{A}$,	See Figure 6-6	2.7			V
V_{OL}	Low-level output voltage	$V_{ID} = -200\text{ mV}$,	$I_{OL} = 8\text{ mA}$,	See Figure 6-6			0.45	V
I_{OZ}	High-impedance-state output current	$V_O = 0.4\text{ V to } 2.4\text{ V}$					± 20	μA
I_I	Line input current	Other input = 0 V ⁽³⁾	$V_I = 12\text{ V}$				1	mA
			$V_I = -7\text{ V}$				-0.8	
I_{IH}	High-level enable-input current	$V_{IH} = 2.7\text{ V}$					20	mA
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4\text{ V}$					-100	mA
r_i	Input resistance				12			k Ω
I_{OS}	Short-circuit output current	$V_{ID} = 200\text{ mV}$,	$V_O = 0$		-15		-85	mA
I_{CC}	Supply current	No load	Receiver outputs enabled, Driver inputs disabled			19	30	mA
			Outputs disabled			19	26	

(1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

5.8 Switching Characteristics - Receivers

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$, See Figure 6-7	$C_L = 15\text{ pF}$,		9	14	19	ns
t_{PHL}	Propagation delay time, high- to low-level output	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$, See Figure 6-7	$C_L = 15\text{ pF}$,		9	14	19	ns
	Skew ($t_{PHL} - t_{PLH}$)	$V_{ID} = -1.5\text{ V to } 1.5\text{ V}$, See Figure 6-7	$C_L = 15\text{ pF}$,			2	6	ns
t_{PZH}	Output enable time to high level	$C_L = 15\text{ pF}$,		See Figure 6-8		7	14	ns
t_{PZL}	Output enable time to low level	$C_L = 15\text{ pF}$,		See Figure 6-8		7	14	ns
t_{PHZ}	Output disable time from high level	$C_L = 15\text{ pF}$,		See Figure 6-8		20	35	ns
t_{PLZ}	Output disable time from low level	$C_L = 15\text{ pF}$,		See Figure 6-8		8	17	ns

(1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

5.9 Typical Characteristics

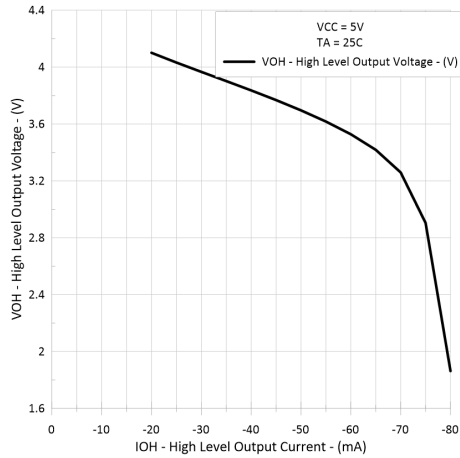


Figure 5-1. Drivers High-Level Output Voltage vs High-Level Output Current

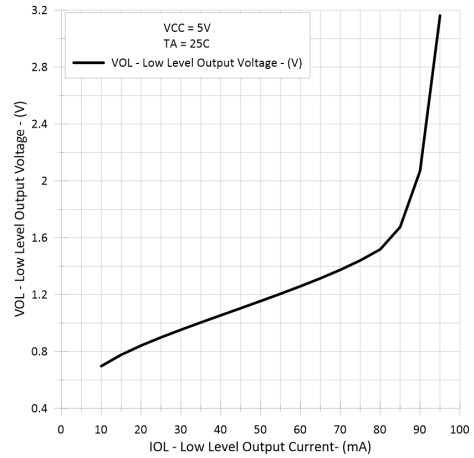


Figure 5-2. Drivers Low-Level Output Voltage vs Low-Level Output Current

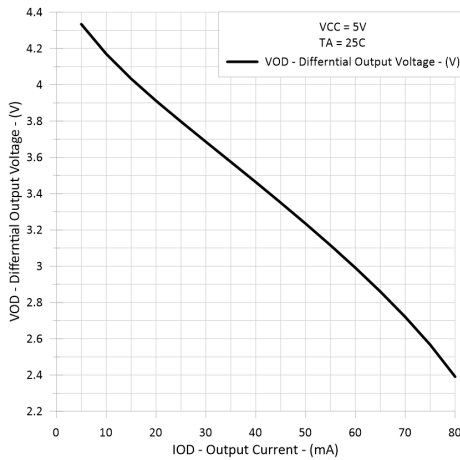


Figure 5-3. Drivers Differential Output Voltage vs Output Current

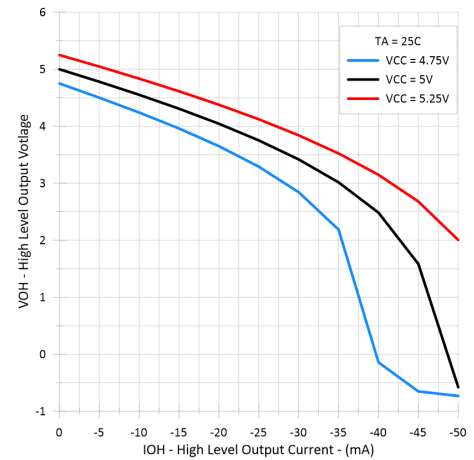


Figure 5-4. Receivers High-Level Output Voltage vs High-Level Output Current

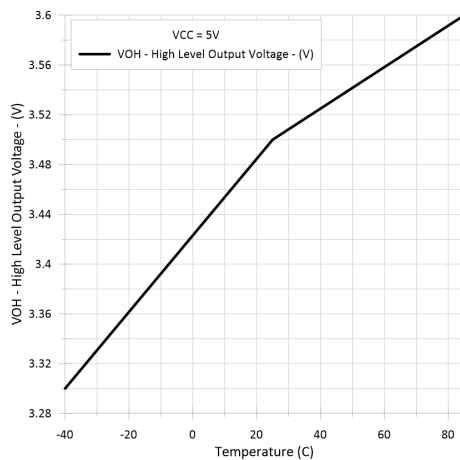


Figure 5-5. Receivers High-Level Output Voltage vs Free-Air Temperature

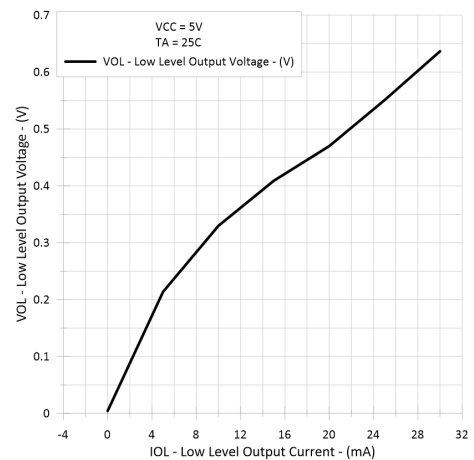
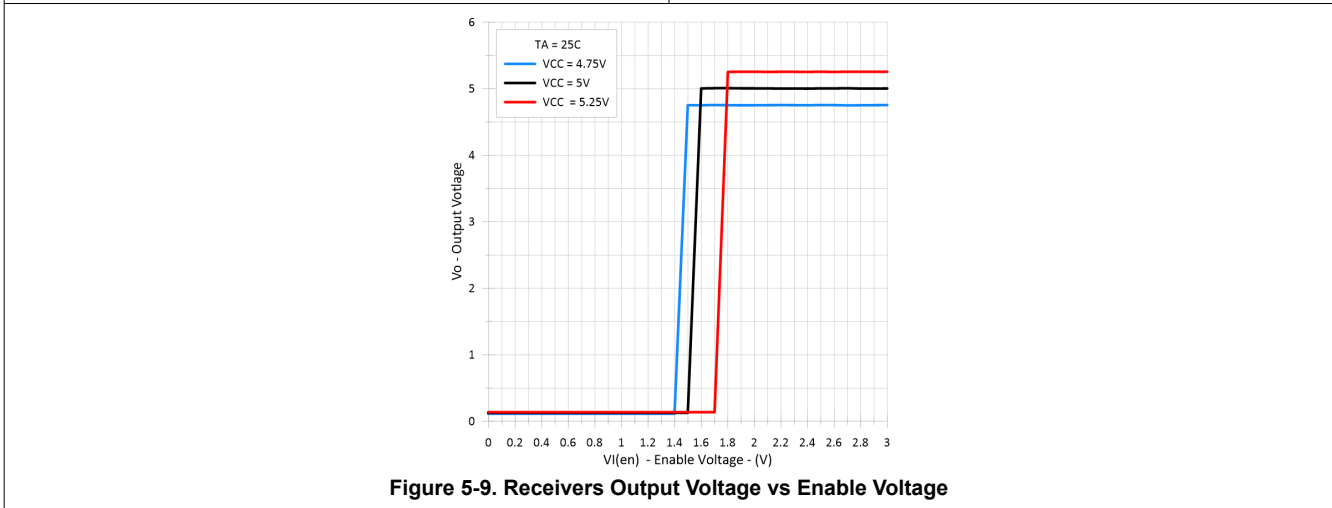
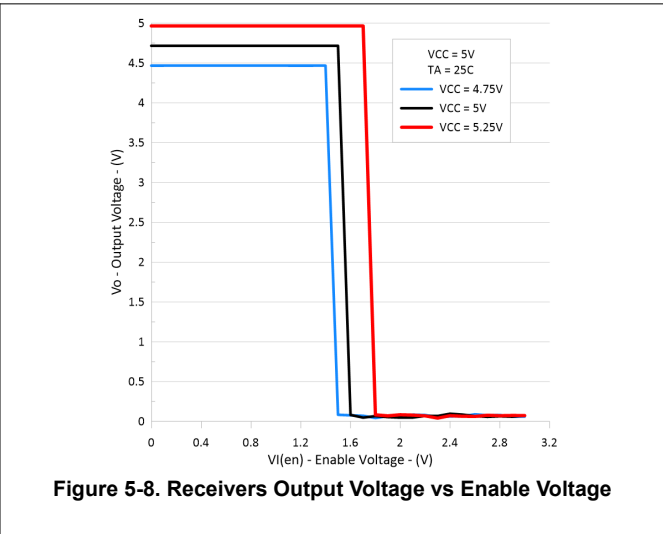
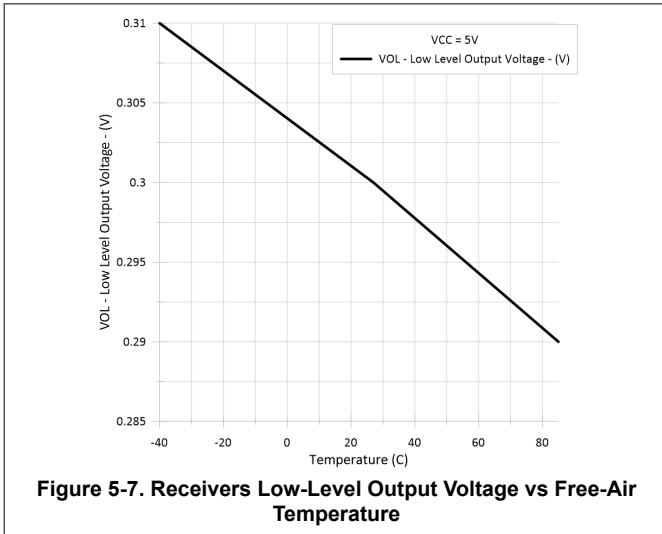


Figure 5-6. Receivers Low-Level Output Voltage vs Low-Level Output Current

5.9 Typical Characteristics (continued)



6 Parameter Measurement Information

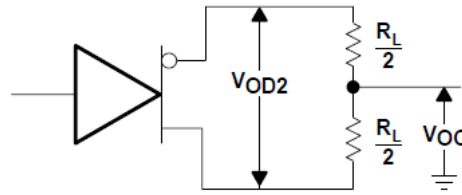


Figure 6-1. Driver V_{OD2} and V_{OC}

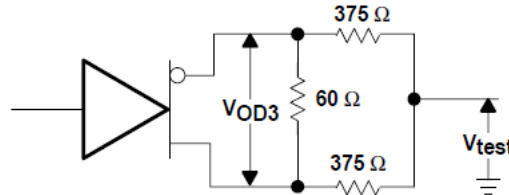
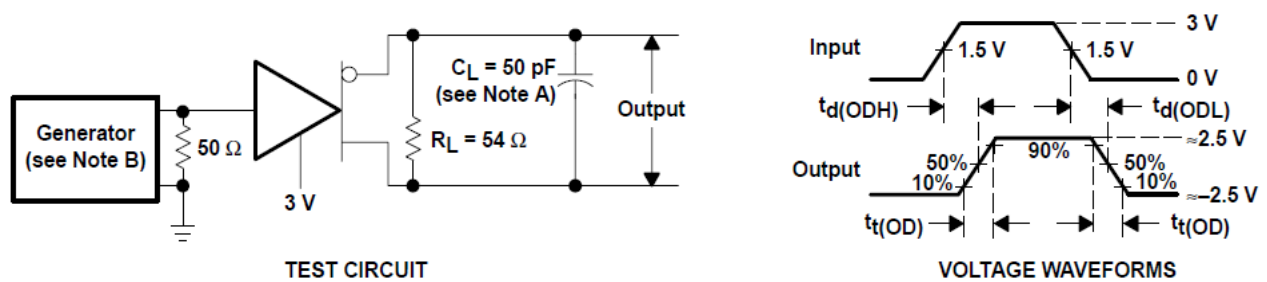
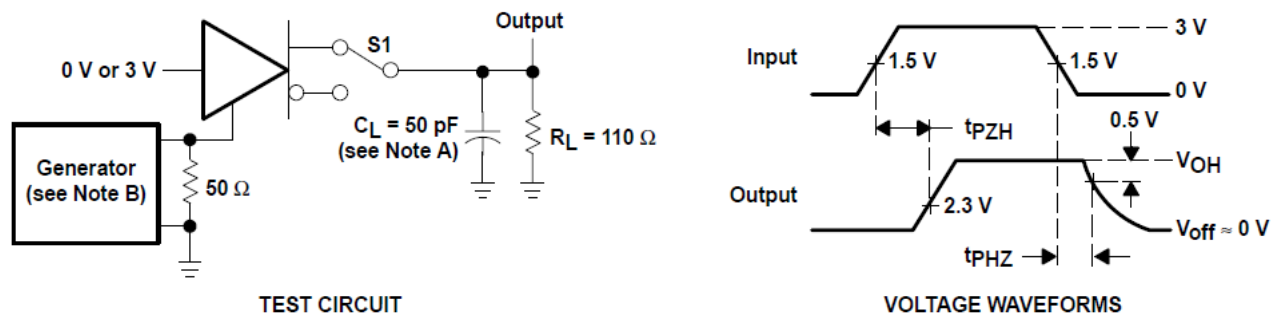


Figure 6-2. Driver V_{OD3}



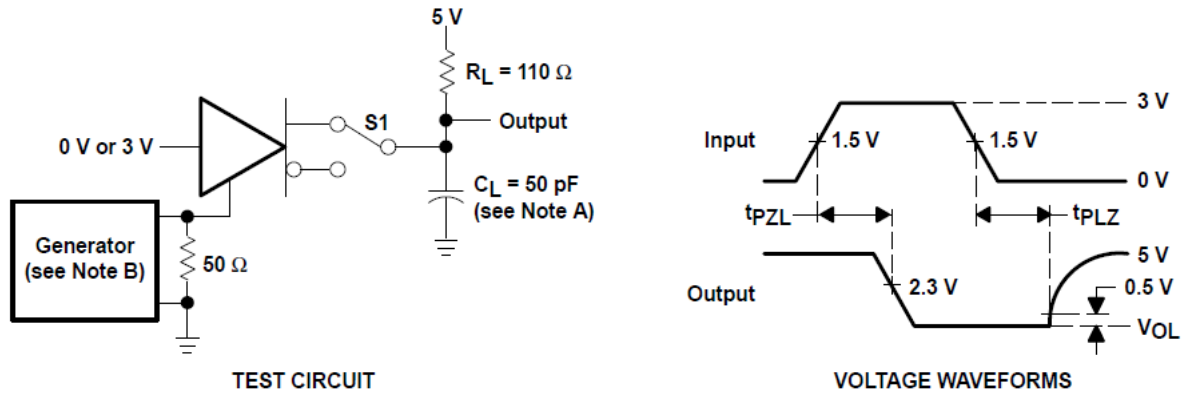
- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 6-3. Driver Test Circuit and Voltage Waveforms



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 6-4. Driver Test Circuit and Voltage Waveforms



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

Figure 6-5. Driver Test Circuit and Voltage Waveforms

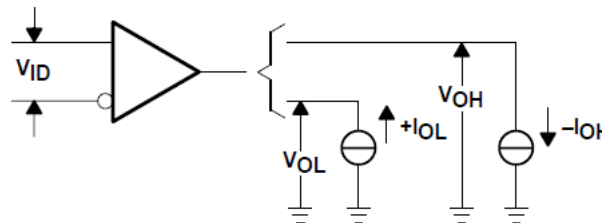
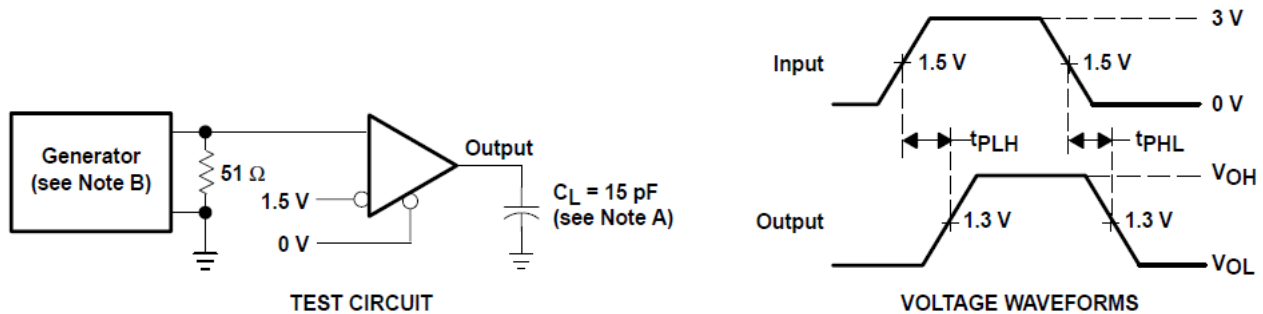
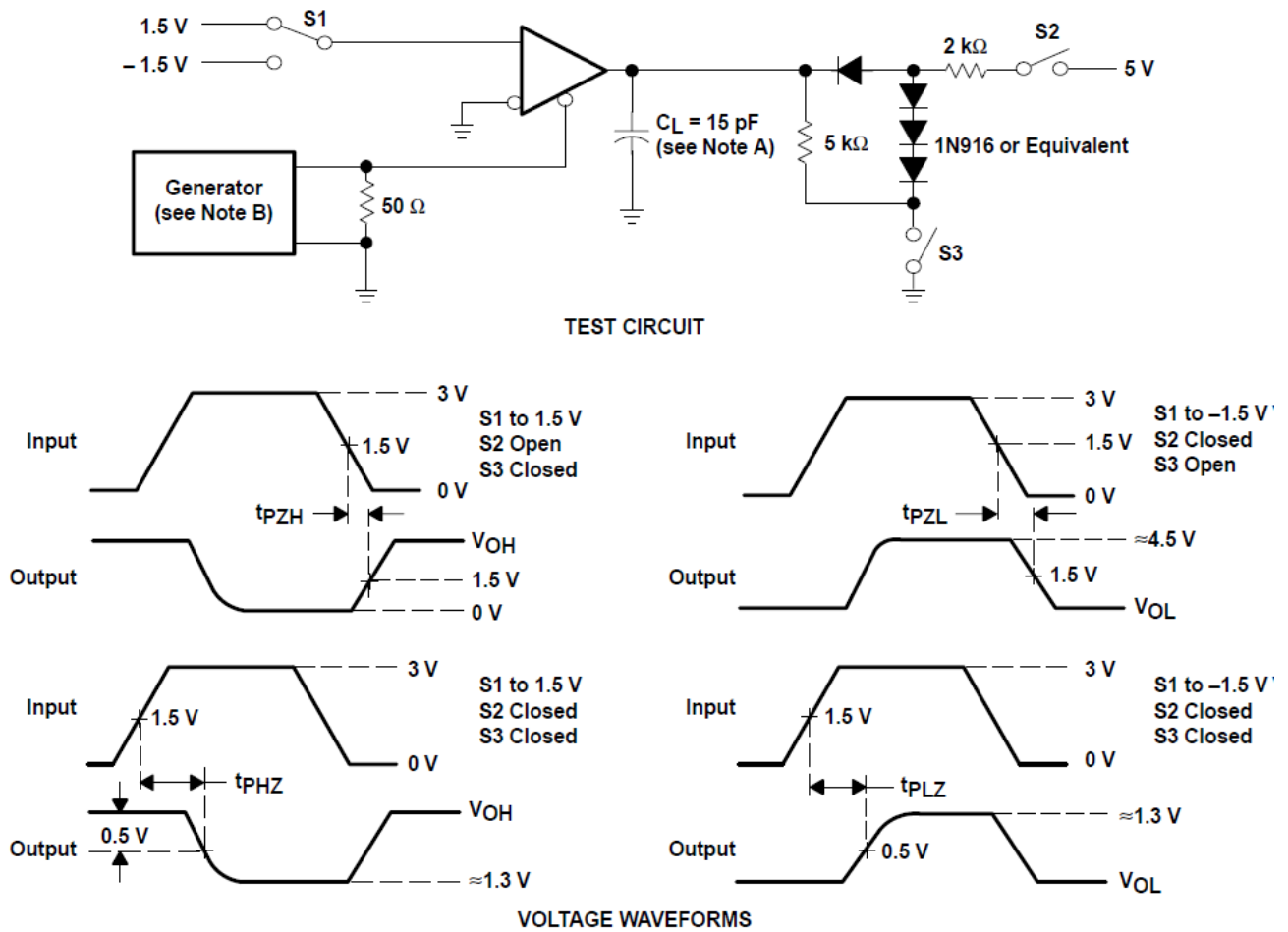


Figure 6-6. Receiver V_{OH} and V_{OL}



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

Figure 6-7. Receiver Test Circuit and Voltage Waveforms



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 6-8. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

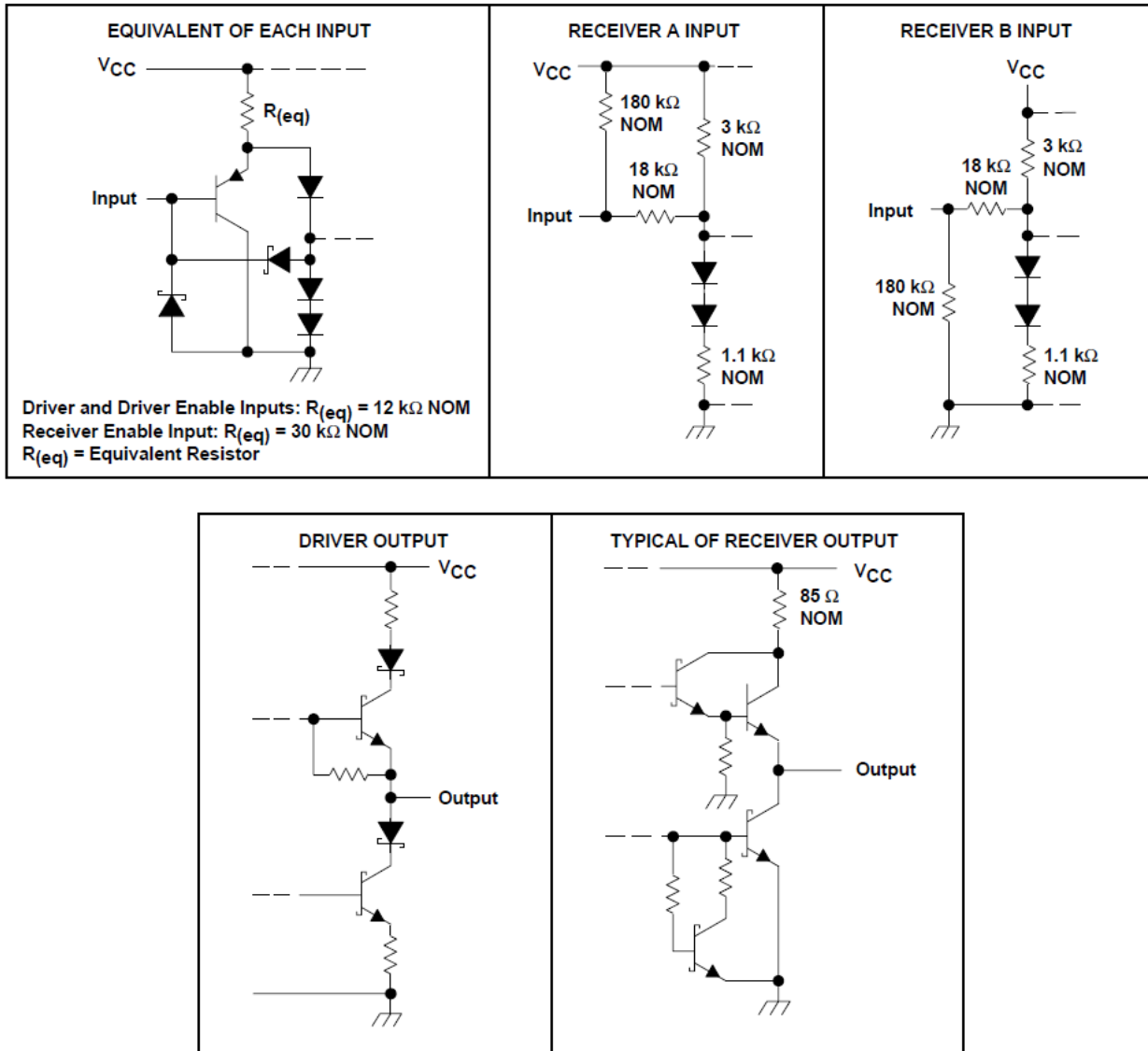


Figure 7-1. Schematic of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

Table 7-1. Driver⁽¹⁾

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

Table 7-2. Receiver⁽¹⁾

DIFFERENTIAL INPUTS A-B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

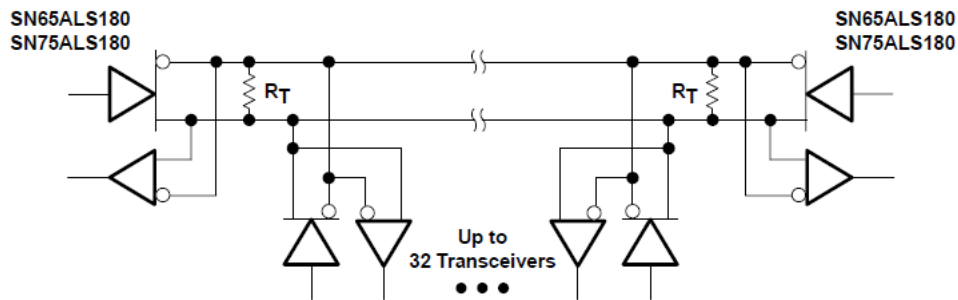
8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application



- A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 8-1. Typical Application Circuit

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS180D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN65ALS180DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN65ALS180DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65ALS180	Samples
SN75ALS180D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS180	Samples
SN75ALS180DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS180	Samples
SN75ALS180N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS180N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN75ALS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS180DR	SOIC	D	14	2500	356.0	356.0	35.0
SN75ALS180DR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65ALS180D	D	SOIC	14	50	506.6	8	3940	4.32
SN75ALS180D	D	SOIC	14	50	506.6	8	3940	4.32
SN75ALS180N	N	PDIP	14	25	506	13.97	11230	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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