DP80390CPU

Pipelined High Performance 8-bit Microcontroller ver 3.10

OVERVIEW

DP80390CPU is an **ultra high performance, speed optimized** soft core of a single-chip 8-bit embedded controller dedicated for operation with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern about **performance to power consumption** ratio. This ratio is extended by an advanced power management unit **PMU**.

DP80390CPU soft core is 100% binary-compatible with the industry standard 80390 & 8051 8-bit microcontroller. There are two configurations of DP80390CPU: **Harward** where internal data and program buses are separated, and **von Neumann** with common program and external data bus. DP80390CPU has Pipelined RISC architecture **10 times faster** compared to standard architecture and executes **85-200 million instructions** per second. This performance can also be exploited to great advantage in **low power** applications where the core can be clocked over ten times more slowly than the original implementation for no performance penalty.

DP80390CPU is delivered with **fully automated testbench** and **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- 100% software compatible with industry standard 80390 & 8051
  - *LARGE mode – 8051 instruction set*
  - *FLAT mode – 80390 instruction set*
- Pipelined RISC architecture enables to execute instructions 10 times faster compared to standard 8051
- 24 times faster multiplication
- 12 times faster addition
- Up to 256 bytes of internal (on-chip) Data Memory
- **Up to 16M bytes of linear Program Memory**
  - *64 kB of internal (on-chip) Program Memory*
  - *16 MB external (off-chip) Program Memory*
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory

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- Dedicated signal for Program Memory writes.
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready
- **2.0 GHz virtual** clock frequency in a 0.35u technological process

PERIPHERALS

- DoCD™ debug unit
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware breakpoints activated at a certain*
    - *Program address (PC)*
    - *Address by any write into memory*
    - *Address by any read from memory*
    - *Address by write into memory a required data*
    - *Address by read from memory a required data*
  - *Three wire communication interface*
- Power Management Unit
  - *Power management mode*
  - *Switchback feature*
  - *Stop mode*
- Interrupt Controller
  - *2 priority levels*
  - *2 external interrupt sources*

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CONFIGURATION

The following parameters of the DP80390CPU core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

• Internal Program Memory type	- synchronous - asynchronous
• Internal Program ROM Memory size	- - 0 - 64kB -
• Internal Program RAM Memory size	- - 0 - 64kB -
• Internal Program Memory fixed size	- true - false
• Interrupts	- subroutines location
• Power Management Mode	- used - unused
• Stop mode	- used - unused
• DoCD™ debug unit	- used - unused

Besides mentioned above parameters all available peripherals and external interrupts can be excluded from the core by changing appropriate constants in package file.

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

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LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
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  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

DESIGN FEATURES

♦ PROGRAM MEMORY:

The DP80390 soft core is dedicated for operation with Internal and External Program Memory. It maximal linear size is equal to 16 MB. Internal Program Memory can be implemented as:

- *ROM located in address range between 0000h ÷ (ROM_{size}-1)*
- *RAM located in address range between (64kB-RAM_{size}) ÷ FFFFh*

External Program Memory can be implemented as ROM or RAM located in address range between ROM_{size} ÷ 16 MB excluding area occupied by RAM_{size}.

♦ INTERNAL DATA MEMORY:

The DP80390CPU can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as Single-Port synchronous RAM.

♦ EXTERNAL DATA MEMORY:

The DP80390CPU soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

♦ USER SPECIAL FUNCTION REGISTERS:

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP80390CPU design. ESFRs are memory mapped into Direct Memory between addresses 80 hex and FF hex in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

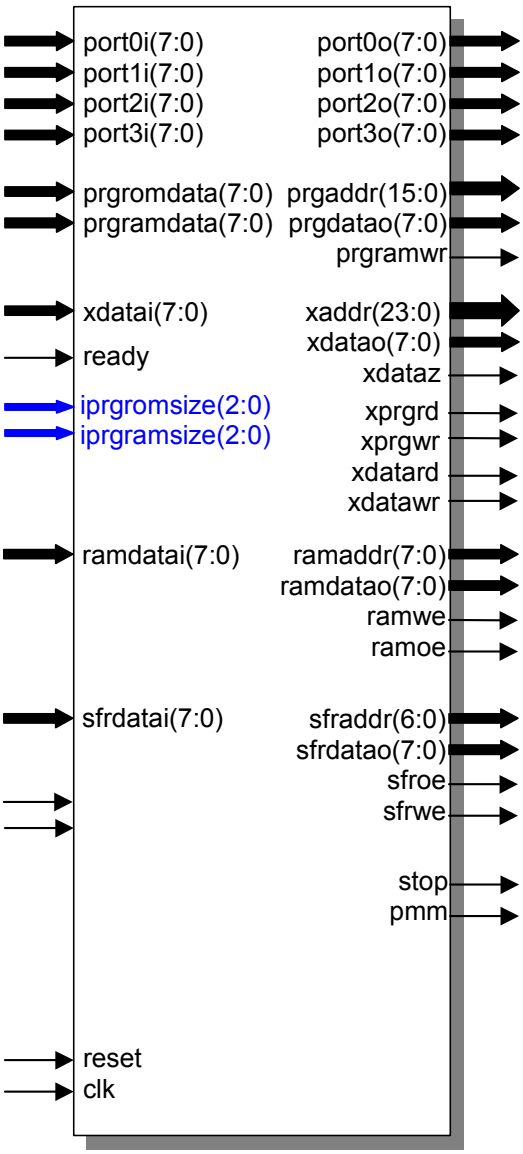
♦ WAIT STATES SUPPORT:

The DP80390CPU soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

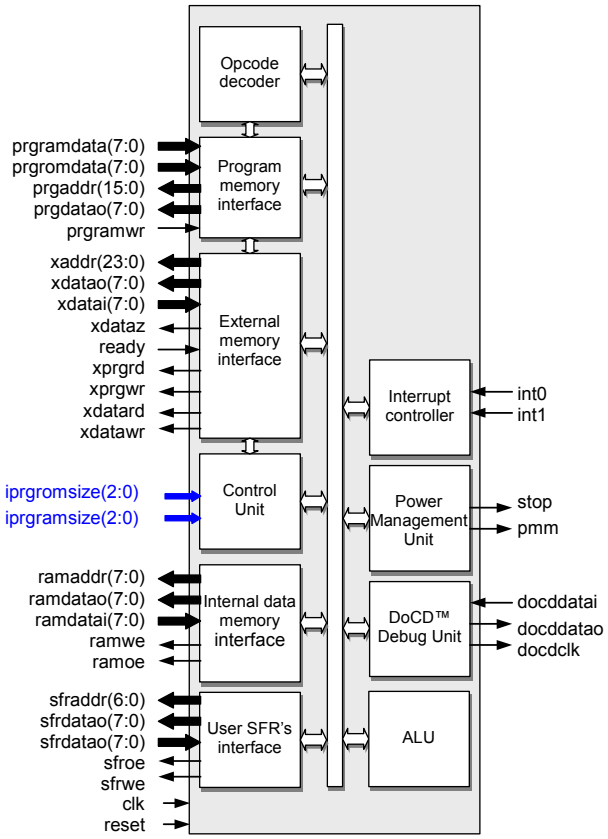
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SYMBOL



BLOCK DIAGRAM



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset
port0i[7:0]	input	Port 0 input
port1i[7:0]	input	Port 1 input
port2i[7:0]	input	Port 2 input
port3i[7:0]	input	Port 3 input
iprgramsize[2:0]	input	Size of on-chip RAM CODE
iprgromsize[2:0]	input	Size of on-chip ROM CODE
prgramdata[7:0]	input	Data bus from int. RAM prog. memory
prgromdata[7:0]	input	Data bus from int. ROM prog. memory
xdatai[7:0]	input	Data bus from external memories
ready	input	External memory data ready
ramdatai[7:0]	input	Data bus from internal data memory
sfrdatai[7:0]	input	Data bus from user SFR's
int0	input	External interrupt 0
int1	input	External interrupt 1
docddatai	input	DoCD™ data input
port0o[7:0]	output	Port 0 output
port1o[7:0]	output	Port 1 output
port2o[7:0]	output	Port 2 output
port3o[7:0]	output	Port 3 output
prgaddr[15:0]	output	Internal program memory address bus

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prgdatao[7:0]	output	Data bus for internal program memory
prgramwr	output	Internal program memory write
xaddr[23:0]	output	Address bus for external memories
xdatao[7:0]	output	Data bus for external memories
xdataz	output	Turn xdata bus into 'Z' state
xprgrd	output	External program memory read
xprgwr	output	External program memory write
xramrd	output	External data memory read
xramwr	output	External data memory write
ramaddr[7:0]	output	Internal Data Memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramoe	output	Internal data memory output enable
ramwe	output	Internal data memory write enable
sfraddr[6:0]	output	Address bus for user SFR's
sfrdatao[7:0]	output	Data bus for user SFR's
sfroe	output	User SFR's read enable
sfrwe	output	User SFR's write enable
docddatao	output	DoCD™ data output
docdclk	output	DoCD™ clock line
pmm	output	Power management mode indicator
stop	output	Stop mode indicator

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic such as arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader loading new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Memory Interface - Contains memory access related registers such as Data Page High (DPH), Data Page Low (DPL) and Data Pointer eXtended (DPX) registers. It performs the external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States, and allows core to work with different speed program memories.

Internal Data Memory Interface – Internal Data Memory interface controls access into the internal 256 bytes memory. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) using all direct addressing mode instructions.

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.

Power Management Unit – Block contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode) to significantly reduce power consumption. Switchback feature allows UARTs, and interrupts to be processed in full speed mode if enabled. It is very desired when microcontroller is planned to use in portable and power critical applications.

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is

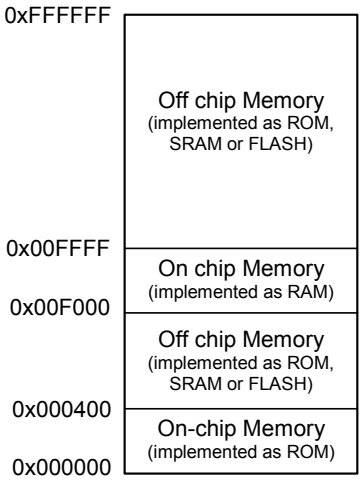
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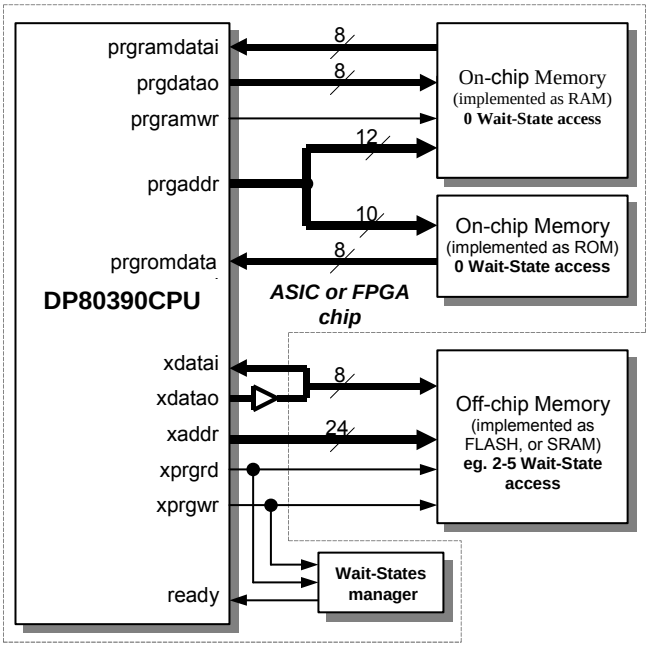
automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

PROGRAM CODE SPACE IMPLEMENTATION

The figure below shows an example Program Memory space implementation in systems with DP80390CPU Microcontroller core. The On-chip Program Memory located in address space between 0kB and 1kB is typically used for BOOT code with system initialization functions. This part of the code is typically implemented as ROM. The On-chip Program Memory located in address space between 60kB and 64kB is typically used for timing critical part of the code e.g. interrupt subroutines, arithmetic functions etc. This part of the code is typically implemented as RAM and can be loaded by the BOOT code during initialization phase from Off-chip memory or through RS232 interface from external device. From the two mentioned above spaces program code is executed without wait-states and can achieve a top performance up to 200 million instructions per second (many instructions executed in one clock cycle). The Off-chip Program Memory located in address space between 1kB and 60kB, and above 64 kB is typically used for main code and constants. This part of the code is usually implemented as ROM, SRAM or FLASH device. Because of relatively long access time the program code executed from mentioned above devices must be fetched with additional Wait-States. Number of required Wait-States depends on memory access time and DP80390CPU clock frequency. In most cases the proper number of Wait-States cycles is between 2-5. The READY pin can be also dynamically modulated e.g. by SDRAM controller.



The figure below shows a typical Program Memories connections in system with DP80390CPU Microcontroller core.



The described above implementation should be treated as an example. All Program Memory spaces are fully configurable. For timing-critical applications whole program code can be implemented as on-chip ROM and (or) RAM and executed without Wait-States, but for some other applications whole program code can be implemented as off-chip ROM or FLASH and executed with required number Wait-State cycles.

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PERFORMANCE

The following tables give a survey about the Core area and performance in ASICs Devices (CPU features and peripherals have been included):

Device	Optimization	F_{max}
0.25u typical	area	100 MHz
0.25u typical	speed	250 MHz

Core performance in ASIC devices

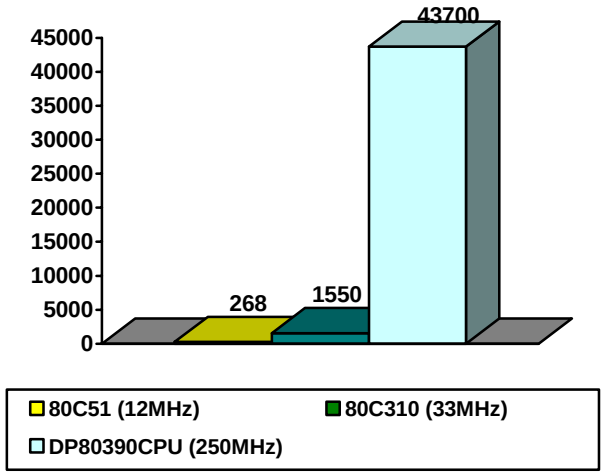
For a user the most important is application speed improvement. The most commonly used arithmetic functions and theirs improvement are shown in table below. Improvement was computed as {80C51 clock periods} divided by {DP80390CPU clock periods} required to execute an identical function. More details are available in core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**9,00**
8-bit addition (*direct addressing*)	**9,00**
8-bit addition (*indirect addressing*)	**9,00**
8-bit addition (*register addressing*)	**12,00**
8-bit subtraction (*immediate data*)	**9,00**
8-bit subtraction (*direct addressing*)	**9,00**
8-bit subtraction (*indirect addressing*)	**9,00**
8-bit subtraction (*register addressing*)	**12,00**
8-bit multiplication	**16,00**
8-bit division	**9,60**
16-bit addition	**12,00**
16-bit subtraction	**12,00**
16-bit multiplication	**13,60**
32-bit addition	**12,00**
32-bit subtraction	**12,00**
32-bit multiplication	**12,60**
Average speed improvement:	**11,12**

Dhrystone Benchmark Version 2.1 was used to measure Core performance. The following table gives a survey about the DP80390CPU performance in terms of Dhrystone/sec and VAX MIPS rating.

Device	Target	Clock frequency	Dhry/sec (VAX MIPS)
80C51	-	12 MHz	268 (0.153)
80C310	-	33 MHz	1550 (0.882)
DP80390CPU	0.25u	250 MHz	43700 (24.872)

Core performance in terms of Dhrystones



Area utilized by the each unit of DP80390CPU core in vendor specific technologies is summarized in table below.

Component	Area [Gates]	[FFs]
CPU*	6500	315
Interrupt Controller	350	40
Power Management Unit	50	5
Total area	6900	360

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

Core components area utilization

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The main features of each DP80390 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I\O Ports	Compare/Capture	Watchdog	Master I^2C Bus Controller	Slave I^2C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DP80390CPU	10	64k	64k	16M	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-
DP80390	10	64k	64k	16M	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-
DP80390XP	10	64k	64k	16M	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

DP80390 family of High Performance Microcontroller Cores

The main features of each DP8051 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I\O Ports	Compare/Capture	Watchdog	Master I^2C Bus Controller	Slave I^2C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DP8051CPU	10	64k	64k	64k	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-
DP8051	10	64k	64k	64k	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-
DP8051XP	10	64k	64k	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

DP8051 family of High Performance Microcontroller Cores

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