Agilent U1084A

Acqiris High-Speed PCIe Digitizers with On-Board Signal Processing

Targeting Embedded OEM Applications

U1084A-001: 8-bit, 2 ch, 1.5 GHz, 2-4 GS/s

U1084A-002: 8-bit, 2 ch, 1.5 GHz, 1-2 GS/s

U1084A-003: 8-bit, 2 ch, 500 MHz, 0.5-1 GS/s

With firmwares for high-speed digitization, simultaneous acquisition and readout, real-time averaging, and real-time signal peak detection

Anticipate ___Accelerate ___Achieve

Agilent Technologies

Main Features

- Highly flexible, high-speed data acquisition card with on-board FPGA for real-time data processing
- Dual- and single-channel acquisition modes
- Up to 4 GS/s sampling rate
- Up to 1.5 GHz bandwidth
- Processing memory options up to 512 MB
- High-speed PCI Express x4 bus transfers data up to 520 MB/s to a host processor
- Fully featured 50 Ω front-end with programmable full-scale, offset, and internal calibration
- Complete pre- and post-triggering
- Six I/O connectors for trigger, clock, reference, and control signals
- Built-in 15 ps Trigger Time Interpolator (TTI) for accurate timing measurements
- Low total power consumption
- Device drivers for 32- and 64-bit Windows® and Linux
- Application code examples for C/C++
- Firmware hot switching for a wider field of applications

INDUSTRY AWARDS

Agilent's high-speed PCIe digitizer with on-board processing received multiple industry awards since its introduction. This level of acknowledgment confirms marketplace recognition and demonstrates excellence in creating value for the customers.

EDN INNOVATION Honoring Excellence in Electronics FINALIST 2009

Test & Measurement World BEST IN TEST FINALIST

GOLDEN MOUSETRAP Best New Products AWARDS FINALIST 2010

Agilent Acqiris High-Speed Digitizers

The proprietary ASICS in Agilent Acqiris high-speed digitizers are designed for the specific purpose of optimizing high-speed ADC performance. The analog front-end technology provides signal conditioning, amplification, and interleaving functions essential for achieving high-speed data acquisition at GS/s rates. The digital data handling components provide vital clock and synchronization signals to capture and memorize acquired data with maximum data throughput. Together these ASICS make low-power, high-fidelity data acquisition much more accessible and provide maximum data throughput to the host PC or processor to reduce the time and cost of measurement.

The Acqiris product line provides a range of high-speed digitizer cards with 8-, 10-, and 12-bit resolution, wide bandwidth, and large acquisition memory. These products, in PCI, PCIe, PXI, cPCI, and VME formats, are used in research, and in ATE and OEM applications in industries such as biotechnology, semiconductors, aerospace, physics, and astronomy.

Embedding Extreme Data Acquisition into your System

The Agilent U1084A Acqiris high-speed data acquisition card allows you to leverage the performance of our leading edge technology and know-how to meet your most demanding requirements.

By integrating our proprietary technology into a standard PCIe card format, we help you reduce the risk associated with new product development, providing a state-of-the-art digitizer front-end that is easily integrated into more complex systems. This principle of using standardized, off-the-shelf, data conversion and signal processing platforms ensures cost-effectiveness, system longevity, and system flexibility, at low risk. Agilent high-speed digitizer products provide consistent quality and reliability you can depend upon.

Compliance, Reliability and Accuracy

As it is designed for OEM use, embedded in equipment that may well fall under RoHS compliance, the U1084A product uses only lead free components and non-toxic methods, to be fully RoHS compliant.

Using Agilent technology and know-how the component count on U1084A is kept to a minimum, increasing the operational reliability of the card, and maximizing analog and digital performance.

Analog performance of the U1084A is such that maximum measurement accuracy performance is obtained over the full bandwidth of the analog front end. Lower noise and more effective bits mean less repeated measurements, reducing measurement time and lowering cost per measurement.

High-Speed Digitizers with Real-Time Analysis

The Agilent U1084A Acqiris high-speed digitizer is a dual-channel, 8-bit PCIe digitizer card with an on-board, high-speed, field programmable gate array (FPGA) component that is used for real-time data processing tasks. Featuring 4 GS/s sampling rates, the digitizer provides on-board real-time signal processing firmware for on-the-fly signal averaging.

Four firmware options allow the digitizer card to perform specific post-processing tasks which are easily uploaded into the FPGA under program control. The firmware options redefine the way in which data acquisition can be performed, allowing extremely flexible and easy reconfiguration for optimum data analysis.

Using the PCI EXPRESS® (PCIe®) bus maximizes the data throughput. Implemented in the base product as a 4-lane PCIe 1.1 card, the U1084A products provide data throughput at up to 520 MB/s.

High-Speed Digitizer with On-Board Signal Processing

Front end mezzanine with ADC

The analog mezzanine contains the analog signal conditioning (amplification, offset, and channel interleaving) as well as the analog-to-digital converter (ADC) component. Impedance on the two input channels (CH1, CH2) is fixed at 50 Ω ± 1%. Either input can be used as a trigger source.

Normally the two channel inputs are sent to their dedicated ADCs and simultaneously sampled at 2 GS/s. Alternatively, with channel interleaving, the signal from either one of the channels can be sent to both ADCs to achieve sampling rates of up to 4 GS/s.

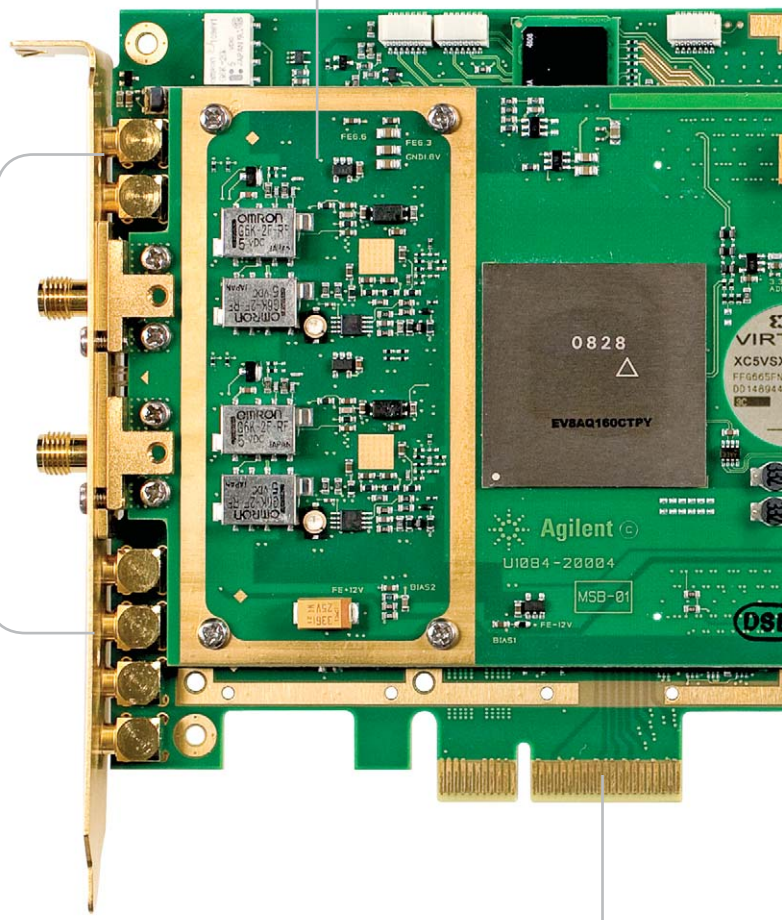
Trigger and clock

The trigger and clock circuitry provides access to trigger input and output as well as reference clock input. The clock circuit provides calibration signals and ADC clock signals for the analog mezzanine as well as the FPGA for data processing. The built-in 15 ps trigger time interpolator (TTI) allows for accurate timing measurements.

I/O control

Control over the trigger, time base, and data processing is made even more flexible by the addition of front-panel input/output connections.

The six MCX-type front-panel connectors can support an external clock (up to 2 GHz) or reference signal (10 MHz), an external trigger input, a trigger output, and three additional I/O digital control lines (I/O A, B, and C). The latter can be used for monitoring or modifying the card' status and configuration. Trigger output can also be used as an I/O control.



PCI Express

The use of the PCIe x4 allows data rates up to 520 MB/s, increasing throughput to reduce measurement time over traditional PCI based technologies.

Flexible data processing

The FPGA provides capacity for real-time processing of the acquired data. The firmware options loaded into the processing FPGA can provide either:

- -DGT/-DGS: Basic high-speed digitization with long acquisition memory or simultaneous acquisition and readout (SAR)
- -AVG: Real-time sampling and averaging
- -TDC: Real-time signal peak detection and analysis

Firmware hot switch

The U1084A is able to hold any two of the available firmware options (-DGT/-DGS, -AVG or -TDC), and can switch between these two in a matter of seconds without powering-off the host computer. This feature adds flexibility and enables the digitizer to be used in a wider field of applications, performing additional measurements on the go.

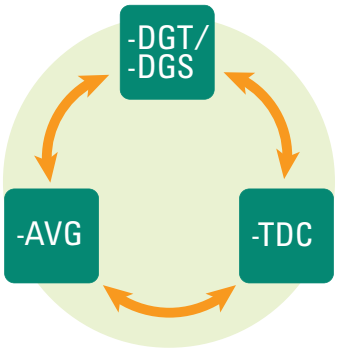


Figure 1a. Switching is permitted between any two of the firmware options.

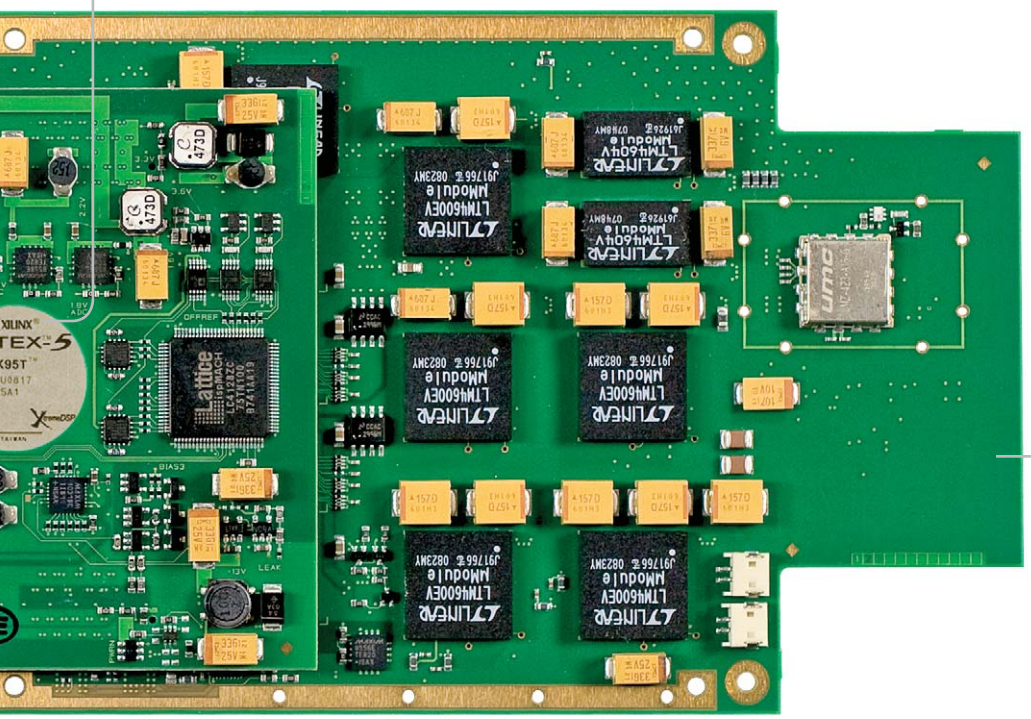


Figure 1. U1084A high-speed digitizer card.

Compliance and reliability

The card uses only lead free components and non-toxic methods, to be fully RoHS compliant. Component count is kept to a minimum, increasing the operational reliability.

Easy integration

Agilent Acqiris high-speed digitizers are supplied with software drivers for Windows®, Linux, and application code examples for C/C++.

These code examples provide card set up and basic acquisition functionality, and are easily modified, so the card can quickly be integrated into a measurement system.

The flexibility of the driver means that, with minimum software adjustments, any Acqiris digitizer can be swapped out, replaced, and upgraded over time, with the latest high-speed Acqiris digitizer.

Acqiris High-Speed PCIe Digitizers

U1084A-001, dual channel, 8-bit, 1.5 GHz, 2 to 4 GS/s
U1084A-002, dual channel, 8-bit, 1.5 GHz, 1 to 2 GS/s
U1084A-003, dual channel, 8-bit, 500 MHz, 0.5 to 1 GS/s

Signal input

Channels
-001: Dual at up to 2 GS/s
Single at up to 4 GS/s
-002: Dual at up to 1 GS/s
Single at up to 2 GS/s
-003: Dual at up to 500 MS/s
Single at up to 1 GS/s

Bandwidth (-3 dB)
-001: DC to 1.5 GHz (1.8 GHz typ.)
-002: DC to 1.5 GHz (1.8 GHz typ.)
-003: DC to 500 MHz (typ.)

Bandwidth limit filter
700 MHz (-001 and -002 only), 200 MHz, and 20 MHz (typ)

Full scale (FS)
50 mV[1], 100 mV, 200 mV, 500 mV, 1 V, 2 V, and 5 V

Offset range
±2 V for 50 mV to 500 mV FS
±5 V for 1 V to 5 V FS

Maximum input voltage
±5 V DC

Coupling
AC, DC

Impedance
50 Ω ± 1%

Connectors
-BNC: two, gold plated
-SMA: two, gold plated

Digital conversion

Sample rate
488.28 kS/s to maximum sample rate, using binary sparsing method

Resolution
8 bits

DNL
± 0.9 LSB

Time base

Clock accuracy
Better than ± 2 ppm

Sampling jitter
< 1 ps rms for 10 µs record length with internal clock and reference (measured)

Trigger (channel and external)

Channel trigger input
Threshold adjust range: FS of channel
Sensitivity, DC to 1.5 GHz: > 15% FS (measured)

Pretrigger
Adjustable to 100% of horizontal full scale

External trigger input (TR IN)
MCX, gold-plated
Impedance: 50 Ω and 1 MΩ ± 2%
Sensitivity (measured):
50 Ω, DC to 1 GHz: > 0.5 V
1 MΩ, DC to 250 MHz: > 0.5 V
Maximum input voltage: ± 5 V DC

Coupling
DC, AC[2], HF reject[2] (50 kHz cutoff) (measured)

Modes
Edge (positive and negative)
Window[2], HF divide by 4[2], spike stretcher[2], dual-source pattern[3] (OR, AND, NOR, NAND)

Trigger output (TR OUT)
MCX, gold-plated
Offset: ± 2.5 V (no load) (typ)
Amplitude: ± 0.8 V (no load), ± 15 mA max (measured)
Rise/fall time: 2.5 ns into 50 Ω (measured)
Coupling: DC
Output impedance: 50 Ω

1) Bandwidth limited to 500 MHz (typ)
2) Channel trigger only.
3) Between either one of the input channels and the external trigger.

Control I/O

Connectors
MCX, gold-plated

Control signals (I/O A, B, and C)
TTL & CMOS compatible (3.3 V)

Control output (I/O A, B, and C)
10 MHz reference clock out with 50 Ω output impedance
Acquisition active
Trigger ready

Control input (I/O A and B)
Trigger enable

External clock (CLK IN)

Connector
MCX, gold-plated

Clock reference
Amplitude: > 1 V pk-pk into 50 Ω (measured)
Threshold: variable between - 2 V and + 2 V (typ)
Maximum input voltage: ± 5 V DC

Clock input
1 GHz or 2 GHz

Reference frequency
10 MHz ± 0.3% (measured)

Real-time FGPA control (I/O A, B, and C)

FPGA
Virtex 5-5SX95T

Control Signals
TTL & CMOS compatible (3.3 V)

Memory [1]
72 Mbit SRAM
-STD: 512 MB DRAM
-256: 256 MB DRAM
-128: 128 MB DRAM

General

Host computer and operating system
PC compatible (x86) systems running 32-and 64-bit Microsoft Windows, and Linux.

Transfer speed
High-speed PCIe 1.1 x4 bus transfers data at sustained rates up to 520 MB/s (measured) to host PC

1) Available data point capacity of processing memory varies depending on the firmware option chosen.

Warranty

1 year
3 years (optional)

Environmental and physical [2]

Operating temperature
5° to 40 °C (PC internal ambient temperature)

Relative humidity
Type-tested at 80 % (non-condensing)

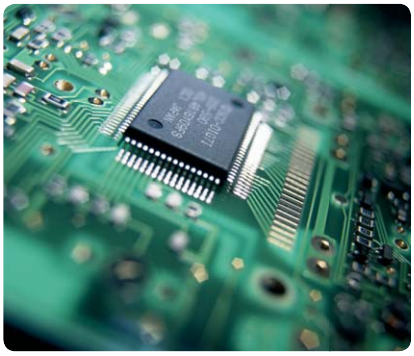
Dimensions
PCIe full-length standard

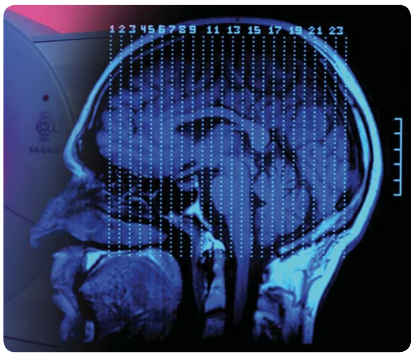
EMC
Complies with European EMC directive 2004/108/EC
· IEC/EN 61326-2-1
· CISPR Pub 11 Group 1, class A
· AS/NZS CISPR 11
· ICES/NMB-001

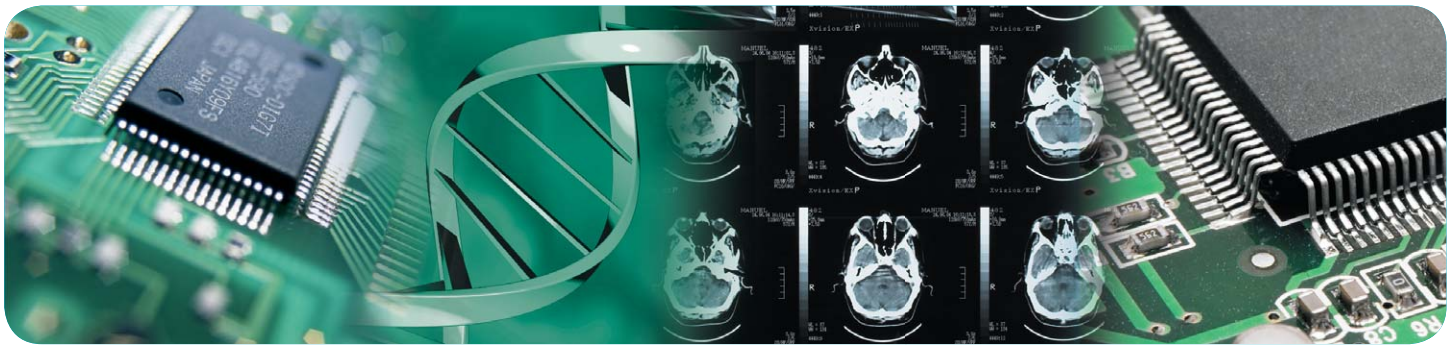
This ISM device complies with Canadian ICES-001.
Cet appareil ISM est conforme a la norme NMB-001 du Canada.

Power consumption
See firmware option specifications

2) Samples of this product have been type tested in accordance with the Agilent Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions.







Firmware for High-Speed Digitizers
U1084A-DGT with long acquisition memory
U1084A-DGS with simultaneous acquisition and readout

Main Features

- **High-speed digitizer firmwares with dual- and single-channel acquisition modes**
- **Up to 4 GS/s sampling rate on either channel**
- **Segmented acquisition**
- **Simultaneous acquisition and readout (SAR) mode for maintained high measurement throughput (with Option U1084A-DGS)**
- **Up to 512 MSamples of acquisition memory with Option U1084A-DGT, 256 MSamples with Option U1084A-DGS**
- **15 ps Trigger Time Interpolator (TTI) for accurate timing measurements**
- **High-speed PCI Express x4 bus transfers data up to 520 MB/s to a host processor**

The on-board processing engine of the U1084A provides extended performance for high speed data acquisition. Smart memory handling with sustained sequential recording mode, allows continuous data acquisition and readout of high-trigger rate signals.

Digitizer firmware options

Two digitizer firmwares are available for the U1084A.

Digitizer firmware U1084A-DGT allows the platform to perform as a high-speed analog to digital data acquisition module with long acquisition memories, up to 512 MSamples.

Digitizer firmware U1084A-DGS in addition to the -DGT functionality includes a ping-pong memory buffer architecture. The processing memory is split in two so that module can continuously acquire data into one memory bank while the other bank is read into the host processor. This technique is particularly useful for continuous acquisition of data bursts at a sustained trigger rate.

Sequence acquisition

Digitizers acquire waveforms in association with triggers. Each waveform is made of a series of measured voltage values (sample points) that are acquired by the ADC at a uniform clock rate. To maximize sampling rates and utilize memory as efficiently as possible, the U1084A digitizer firmwares include both single and sequential storage modes.

The single acquisition mode is the normal operation of most digitizer products. In this mode an acquisition consists of a waveform recorded with a single trigger.

The sequence acquisition mode allows the capture and storage of consecutive "single" waveforms in up to 64 thousand segments within the memory. Sequence acquisition mode is useful as it can optimize the digitizer's sampling rate and memory requirements for applications where only portions of the signal being analyzed are important. This mode is extremely useful in almost all impulse-response type applications.

Sequence acquisition with segments acquires only the specified data, and so enables successive events, which can occur within a very short time, to be captured and stored without loss.

Minimum bank switching dead time for remarkable sustained rates

The sustained sequential recording (SSR) mode of the U1084A-DGS digitizer maximizes the available data throughput allowing data acquisition to run in parallel to the data readout through the PCIe interface.

Simultaneous acquisition and readout (SAR) uses a semaphore-based technique to automatically switch and redirect the digitized data to the second bank once the first has been filled. Rapid switching combined with state-of-the-art trigger circuitry dramatically reduces dead time between successive acquisitions, and allows automatic sequential waveform recording at remarkably high sustained trigger rates. This data handling mode is ideal for situations where fast sequential or burst-style repetitive signals (or pulses) are being acquired and recorded. Applications include signal intelligence, synthetic aperture radar, ultrasound, radar, and lidar.

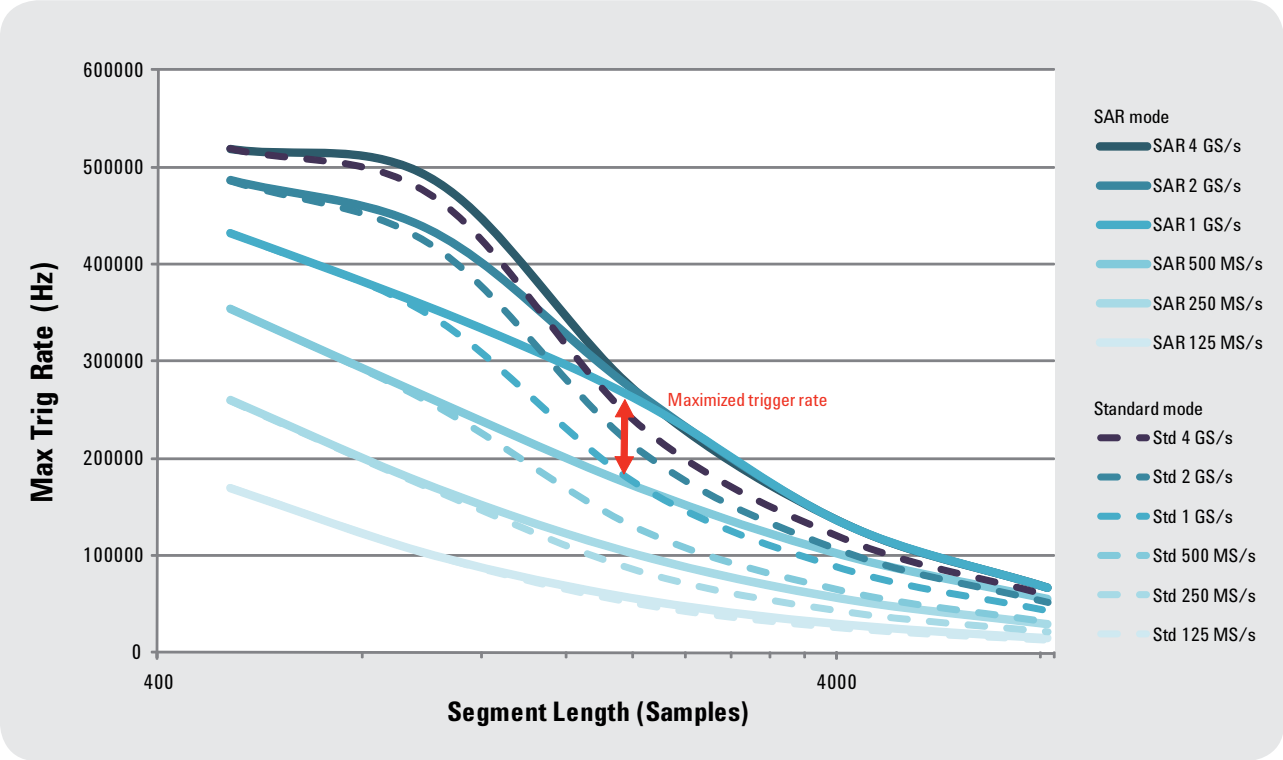


Figure 2. With SAR function the trigger rate is maximized, the figure shows the maximum trigger rate as a function of segment size for a large number of segments[1].

1. *The maximum trigger rate can be affected by operating system interrupts, PCIe bus activity and other system hardware components.*

Firmware for High-Speed Digitizers
U1084A-DGT with long acquisition memory
U1084A-DGS with simultaneous acquisition and readout

Running on U1084A card

Digital conversion

Sample rate
4 GS/s (-001 only), 2 GS/s (-001 and -002 only), 1 GS/s, 500 MS/s, 250 MS/s, 125 MS/s, 62.5 MS/s, 31.25 MS/s, 15.6 MS/s, 7.8 MS/s, 3.9 MS/s, 1.95 MS/s, 977 kS/s, 488 kS/s

Optional memory
-DGT:
-STD: 512 MS or 256 MS/channel
-256: 256 MS or 128 MS/channel
-128: 128 MS or 64 MS/channel

-DGS:
-STD: 256 MS or 128 MS/channel
-256: 128 MS or 64 MS/channel
-128: 64 MS or 32 MS/channel

Effective bits (at maximum dual channel sampling rate, 500 mV FSR and full bandwidth)
> 6.5 at 10 MHz
> 6.2 at 100 MHz
> 5.9 at 410 MHz
> 4.9 at 910 MHz

Time base

Clock accuracy
Better than ± 2 ppm

Sampling jitter
< 1 ps rms for 10 µs record length with internal clock and reference (measured)

Acquisition modes
Single shot
Sequence: 1 to 64 Ksegments
Dead time: < 1.8 µs (measured)

Trigger (channel and external)

Channel trigger
Threshold adjust range: FS of channel
Sensitivity, DC to 1.5 GHz: > 15% FS (measured)

Pretrigger
Adjustable to 100% of horizontal full scale

External trigger input
MCX, gold-plated
Impedance: 50 Ω / 1 MΩ ± 2%
Sensitivity (measured):
50 Ω, DC to 1 GHz: > 0.5 V
1 MΩ, DC to 250 MHz: > 0.5 V
Maximum input voltage: ± 5 V DC

Coupling
DC, AC, HF reject (50 kHz cutoff) (measured)

Modes
Edge (positive and negative)
Window[1], HF divide by 4[1], spike stretcher[1], dual-source pattern[2] (OR, AND, NOR, NAND)

Trigger output (TR OUT)
Offset: ± 2.5 V (no load) (typ)
Amplitude: ± 0.8 V (no load), ± 15 mA max (measured)
Rise/fall time: 2.5 ns into 50 Ω (measured)
Coupling: DC
Output impedance: 50 Ω

1) Channel trigger only.

2) Between either one of the input channels and the external trigger.

Control I/O (MCX)

Control signals (I/O A, B, and C)
TTL & CMOS compatible (3.3 V)

Control output (I/O A, B, and C)
Acquisition active
Acquisition skipping to next segment

Control input (I/O A and B)
Trigger enable

External clock (CLK IN)

Connectors
MCX, gold-plated

Clock reference
Amplitude: > 1 V pk-pk into 50 Ω (measured)
Threshold: variable between - 2 V and + 2V (typ)
Maximum input voltage: ± 5 V DC

Clock input
1 GHz or 2 GHz

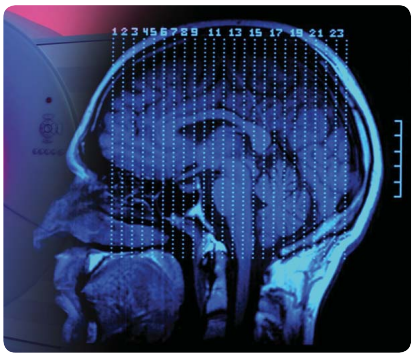
Reference frequency
10 MHz ± 0.3% (measured)

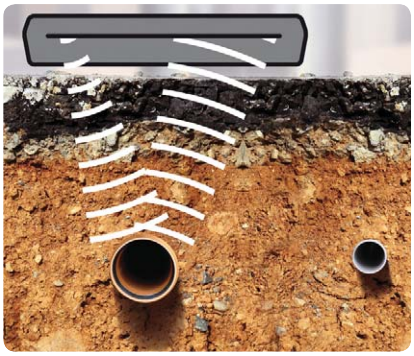
Environmental and physical

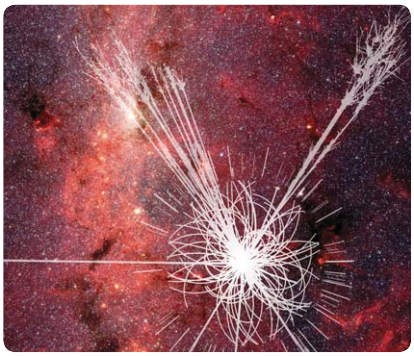
Power consumption
< 45 W (40 W typ)

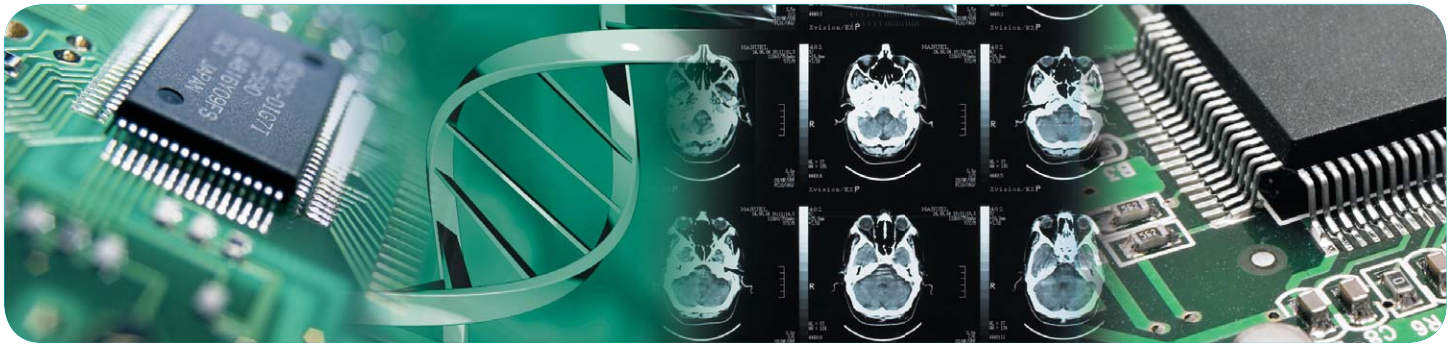
Current requirements (typ.)
Sampling at 4 GS/s

+ 12 V	2.5 A
+ 3.3 V	3 A









Firmware for Real-Time Sampling and Averaging U1084A-AVG

- **Synchronous, dual-channel, real-time sampling and averaging with a maximum trigger rate of up to 500 kHz**
- **Averaging from 1 to over 16 million triggers per segment**
- **Trigger and clock synchronization modes for improved accuracy**
- **Noise Suppressed Accumulation (NSA)**

As a signal averager, the U1084A takes full advantage of the high-speed signal processing performance of the module to create real-time averaged signals to reduce random noise levels in repetitive signals.

Low noise, high dynamic range

The U1084A real-time averaging firmware (U1084A-AVG option) allows real-time acquisition at up to 4 GS/s down to 488.28 kS/s with binary sparsing (4 GS/s divided by 2^n).

Averaging signals reduces random noise effects, improving the signal-to-noise ratio, as well as increasing resolution and dynamic range. The fast sampling rate is achieved with a single trigger and acquisition, and does not require the use of equivalent-time sampling techniques.

Full-speed averaging

In contrast to Averagers that use equivalent-time sampling, the U1084A maintains maximum averaging speed and does not require additional triggers that reduce the total measurement throughput.

Noise suppressed accumulation

In some applications, such as time-of-flight spectroscopy, the signal is a rare event sitting on top of a noisy baseline and the averaging process reduces the random noise. As a consequence, to enhance the digitizers ability to detect such signals in the presence of synchronous noise, the averaging firmware allows the user to set a threshold that must be exceeded for each data value to be entered into the sum.

Furthermore, to simplify overall system design in order to avoid overflow in the summed data, the noise base can be subtracted from each data value before the summation is done. A similar capability is implemented for negative-going signals.

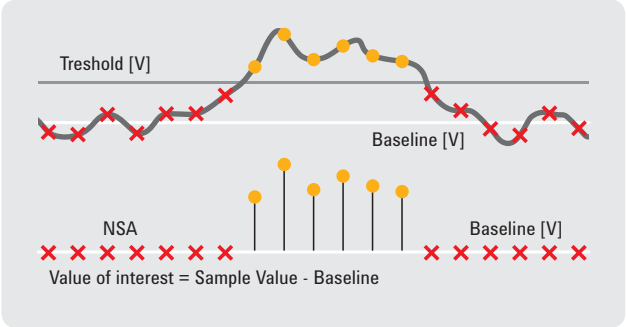


Figure 3. Signal detection using noise suppressed accumulation

Segment accumulation

In time-resolved applications where multiple averaged waveforms must be acquired with very low dead time, the averaging memory can also be segmented. This allows the user to store from 1 up to 128 K separate accumulations of summed data. The segment length is user-programmable.

In standard segment accumulation mode the user selects the desired number of triggers per segment, N, up to over 16 million. The next segment accumulation will be started after the previous N triggers have been processed.

The memory in the U1084A averager is optimized to allow real-time acquisition and averaging. At the end of each average segment, a dead time exists before a new average can be stored. The dead time duration depends on the size of the segment, a 162 KS segment will incur a 1 ms dead time.

Ping-pong accumulation

To increase measurement rates the U1084A with AVG firmware will allow ping-pong accumulation and processing.

After the dead time, at the end of each segment accumulation, a new accumulation can be started before readout of the previous accumulation. While accumulation continues, the previous segment can be read out through the high speed PCIe bus at up to 520 MB/s.

Firmware for Real-Time Sampling and Averaging U1084A-AVG

Running on U1084A card

Digital conversion

Sample rate
4 GS/s (-001 only), 2 GS/s (-001 and -002 only), 1 GS/s, 500 MS/s, 250 MS/s, 125 MS/s, 62.5 MS/s, 31.25 MS/s, 15.6 MS/s, 7.8 MS/s, 3.9 MS/s, 1.95 MS/s, 977 kS/s, 488 kS/s

Resolution
8 bits

Time base

Clock accuracy
Better than ± 2 ppm

Acquisition modes
Single shot
Sequence

Averaging memory

Acquisition length
-STD: 1 to 524,288
-256: 1 to 262144
-128: 1 to 131072

Dead time:
< 1.8 µs for successive triggers

Averaging speed
-001: Up to 4 GS/s
-002: Up to 2 GS/s
-003: Up to 1 GS/s

System performance

Averaging resolution
32 bits

Transfer to PCI Express
130 MSamples/s

Coherent noise (typical)
< 0.02 LSB RMS (73 dB SNR)

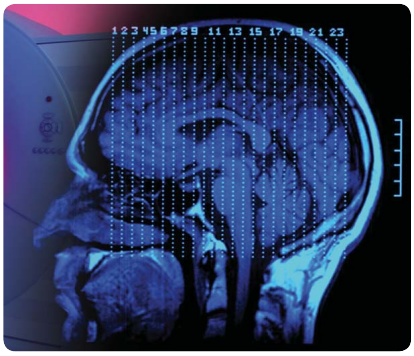
Conditions: 10,000 accumulated triggers, 10 KSamples, no input signal, ext. TRG, 100 mV FS, zero offset

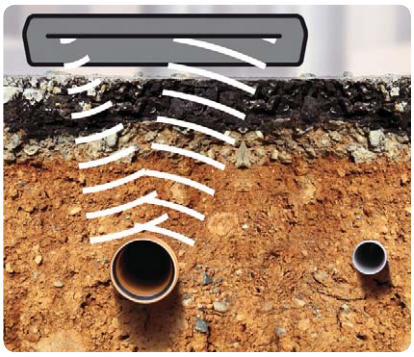
Environmental and physical

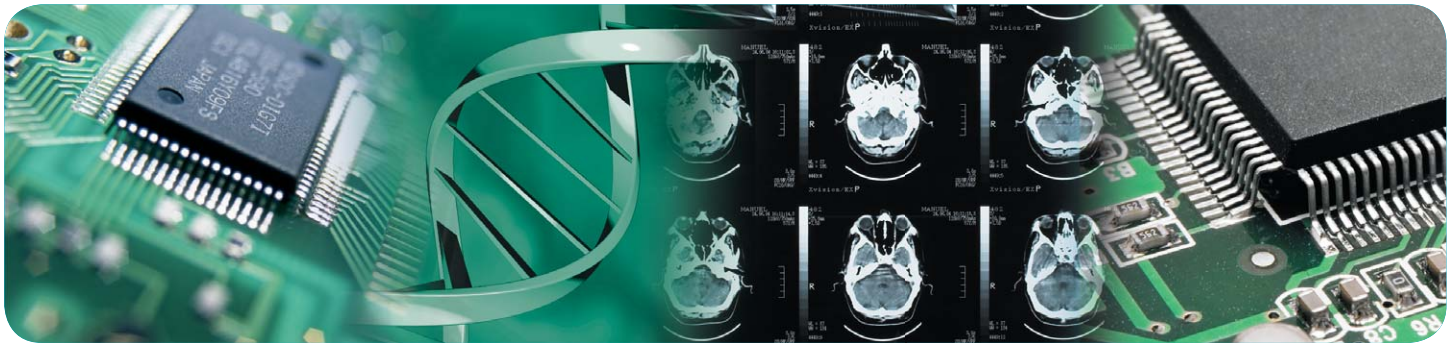
Power consumption
< 50 W (43 W typ)

Current requirements (typ.)
Sampling at 4 GS/s

+ 12 V	2.5 A
+ 3.3 V	4 A







Firmware for Real-Time Signal Peak Detection, Time-to-Digital Conversion and Analysis U1084A-TDC

- **Single-channel sampling and processing at up to 4 GS/s, on either input [1]**
- **Effective acquisition length of 580 KSamples per channel**
- **Peak interpolation with time resolution down to 1/16th of the sampling period**
- **Programmable on-board TDC histogram creation with up to 4 billion counts per bin, peak count or summed amplitude**

The U1084A peak detection and analysis firmware (U1084A-TDC option) allows real-time acquisition and peak detection at up to 4 GS/s (down to 488.28 kS/s with binary sparsing). The firmware enables the creation of a histogram of peak position versus time for successive acquisitions, the histogram bins containing peak counts or summed peak amplitudes.

A large FIFO is used to provide a peak overflow protection: In the event that a burst of peaks causes congestion in the data flow, none of the previously acquired data is lost.

Large memory, high throughput

With 580 KSamples of peak analysis memory, the acquired peak data can be transferred to the host PC at up to 130 Mbins/s, with each time bin as 32 bits.

1) U1084A-TDC firmware does not support synchronous dual-channel sampling.

Powerful peak detection algorithm

Due to the incredible sampling speeds of the U1084A, the peak analysis firmware uses a very simple yet powerful algorithm to detect signal peaks at up to the full 4 GS/s sampling rate.

Nine samples are used to validate if a sample corresponds to a peak; the sample itself, along with the four samples before and after that sample are considered.

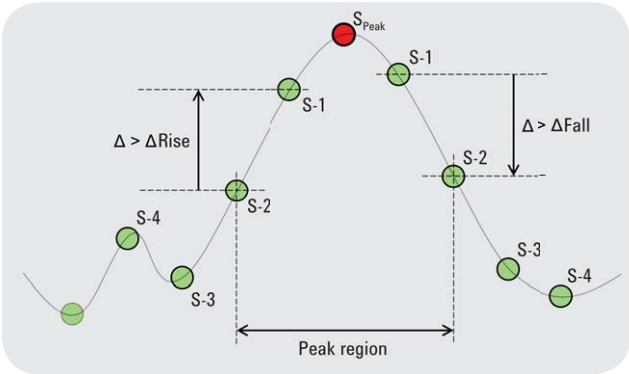


Figure 4. Peak detection algorithm in action

The sample will be considered as a peak, if within the 9 samples analyzed: a rising edge is found before the sample that exceeds the programmable delta ΔRise, a falling edge is found after the sample that exceeds the programmable delta ΔFall, and the sample is the maximum of all points between the two defined rising and falling edges. There is additional verification to make sure that only one peak is found within the rising and falling edge region.

Using this algorithm, peaks can be found on-the-fly in signals with frequencies up to half the sample rate.

Peak interpolation

To improve the measurement, peak time and amplitude are determined using an interpolation routine. Fitting a 12-bit quadratic spline to the 3 points around the extrema found by the peak detection algorithm, the position of a peak maximum is found and defined by its time (Tmax) and amplitude (Vmax).

This interpolation method provides measurement with improved time and vertical resolution. The resulting histogram that is created, can contain up to 2 Mbins of data, with each bin width down to 1/16th of the sampling period, peak amplitudes encoded with the bins, to 1/16th of the ADC resolution.

Adjustable through software commands, the user can balance the increased timing and vertical resolution against increased memory usage and reduced measurement throughput, to best fit requirements.

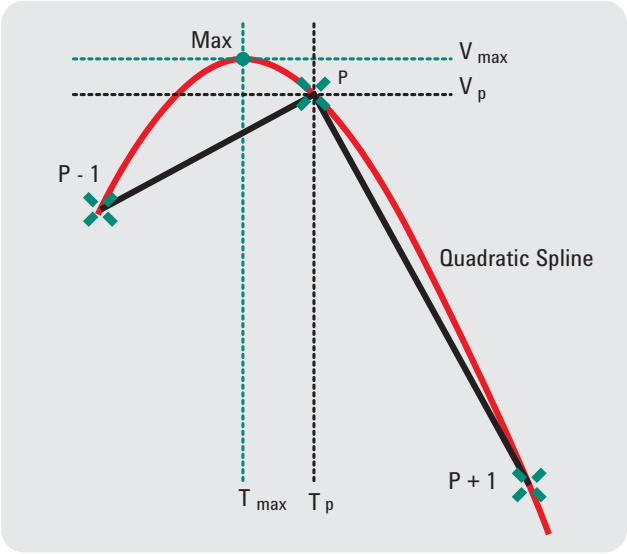


Figure 5. Peak interpolation with quadratic spline

Firmware for Real-Time Signal Peak Detection, Time-to-Digital Conversion and Analysis U1084A-TDC

Running on U1084A card

Digital conversion

Sample rate
4 GS/s (-001 only), 2 GS/s (-001 and -002 only), 1 GS/s, 500 MS/s, 250 MS/s, 125 MS/s, 62.5 MS/s, 31.25 MS/s, 15.6 MS/s, 7.8 MS/s, 3.9 MS/s, 1.95 MS/s, 977 kS/s, 488 kS/s

Resolution
8 bits

Time base

Clock accuracy
Better than ± 2 ppm

Sampling jitter
< 1 ps rms for 10 µs record length with internal clock and reference (measured)

Acquisition modes
Single segment
Single input (Input 1 or 2)

Peak histogram

Acquisition length
Programmable from 1 to 589,824 Samples

Double-pulse resolution
0.5 ns at 4 GS/s

Maximum sustained analysis rate
60 Mpeak/s (measured)

System performance

Histogram
Count by peak value or event
Vertical count 32 bits/bin
Horizontal resolution down to 1/16th of sample rate
Readout 130 Mbins/s

Environmental and physical

Power consumption
< 40 W (32 W typ)

Current requirements (typ.)
Sampling at 4 GS/s

+ 12 V	2.3 A
+ 3.3 V	1.2 A

Contacts

Americas	
Canada	(877) 894 4414
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United States	(800) 829 4444

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Korea	080 769 0800
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Revised: January 6, 2012

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Published in USA, September 21, 2012
5990-4316EN

Ordering Information

Model	**Description**
U1084A	8-bit PCIe high-speed digitizer with on-board signal processing
U1084A-001	Dual channel, 2-4 GS/s digitizer with on-board signal processing
U1084A-002	Dual channel, 1-2 GS/s digitizer with on-board signal processing
U1084A-003	Dual channel, 0.5-1 GS/s digitizer with on-board signal processing
U1084A-STD	Standard 512 MB processing memory
U1084A-256	Processing memory, 256 MB
U1084A-128	Processing memory, 128 MB
U1084A-BNC	BNC connectors
U1084A-SMA	SMA connectors

Choice of firmware options

U1084A-DGT	Digitizer firmware
U1084A-DGS	Digitizer firmware with simultaneous acquisition and readout
U1084A-AVG	Real-time sampling and averaging
U1084A-TDC	Time-to-digital conversion and peak analysis

Accessories

U1084A-UK6	Calibration certificate and data
U1092A-CB5	MCX to BNC, 1 m cable

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