78M6613
Single-Phase AC Power Measurement IC

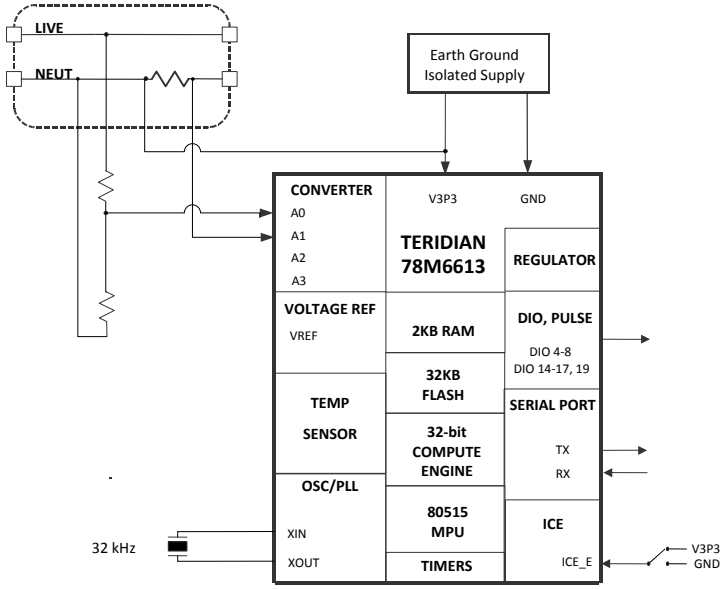
DATA SHEET

DESCRIPTION

The Teridian™ 78M6613 is a highly integrated IC for simplified implementation of single-phase AC power measurement into power supplies, smart appliances, and other applications with embedded AC load monitoring and control. It is packaged in a small, 5mm x 5mm, 32-pin QFN package for optimal space savings.

At the measurement interface, the device provides four analog inputs for interfacing to voltage and current sensors. Voltages from the sensors are fed to our Single Converter Technology® that uses a 22-bit delta-sigma ADC, independent 32-bit compute engine (CE), digital temperature compensation, and precision voltage references to provide better than 0.5% power measurement accuracy over a wide 2000:1 dynamic range.

The integrated MPU core and 32 KB of flash memory provides a flexible means of configuration, post-processing, data formatting, and interfacing to any host processor through the UART interface and/or DIO pins. Complete application firmware is available and can be preloaded into the IC during manufacturing test. Alternatively, a complete array of ICE, development tools, and programming libraries are available to allow customization for each application.



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FEATURES

- < 0.5% Wh Accuracy Over Wide 2000:1 Current Range and Over Temperature
- Voltage Reference < 40ppm/°C
- Four Sensor Inputs—V3P3A Referenced
- 22-Bit Delta-Sigma ADC with Independent 32-Bit Compute Engine (CE)
- 8-Bit MPU (80515), One Clock Cycle per Instruction with 2KB MPU XRAM
- 32KB Flash with Security
- Integrated In-Circuit Emulator (ICE) Interface for MPU Debug
- 32kHz Time Base with Hardware Watchdog Timer
- UART Interface and Up to 10 General-Purpose 5V Tolerant I/O Pins
- Packaged in a RoHS-Compliant (6/6) Lead(Pb)-Free, 32-Pin QFN (5mm x 5mm)
- Complete Application Firmware Provides:
  - True RMS Calculations for Current, Voltage, Line Frequency, Real Power, Reactive Power, Apparent Power, and Power Factor
  - Accumulated Watt-Hours, Kilowatt-Hours
  - Intelligent Switch Control at Zero Crossings
  - Digital Temperature Compensation
  - Phase Compensation (±15°)
  - Quick Calibration Routines
  - 46–64Hz Line Frequency Range with Same Calibration

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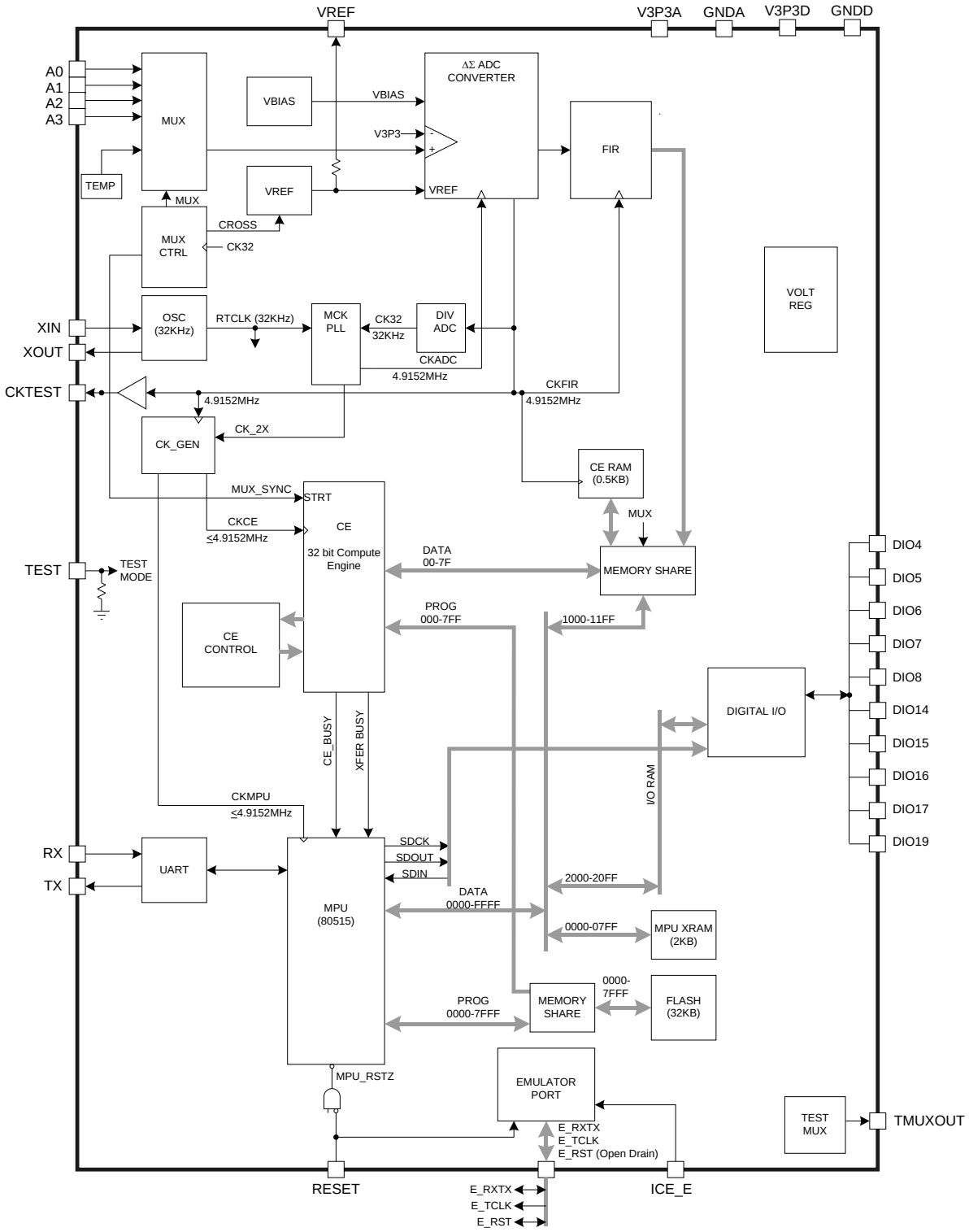


Figure 1: IC Functional Block Diagram

1 Hardware Description

1.1 Hardware Overview

The Teridian 78M6613 single-chip measurement unit integrates all primary functional blocks required to embed solid-state AC power and energy measurement. Included on chip are:

- An analog front end (AFE)
- An independent digital computation engine (CE)
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A voltage reference
- A temperature sensor
- RAM and Flash memory
- A variety of I/O pins

Current sensor technologies supported include Current Transformers (CT) and Resistive Shunts.

In a typical application, the 32-bit compute engine (CE) of the 78M6613 sequentially processes the samples from the voltage inputs on pins A0, A1, A2, A3 and performs calculations to measure active energy (Wh), reactive energy (VARh), A^2h, and V^2h for four-quadrant measurement. These measurements are then accessed by the MPU, processed further and output using the peripheral interfaces available to the MPU.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement. Temperature dependent external components such as crystal oscillator, current transformers (CTs), and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce measurements with exceptional accuracy over the industrial temperature range, if desired.

A block diagram of the IC is shown in Figure 1. A detailed description of various functional blocks follows.

1.2 Analog Front End (AFE)

The AFE of the 78M6613 is comprised of an input multiplexer, a delta-sigma A/D converter and a voltage reference.

1.2.1 Input Multiplexer

The input multiplexer supports up to four input signals that are applied to pins A0, A1, A2 and A3 of the device. Additionally, using the alternate mux selection, it has the ability to select the on-chip temperature sensor. The multiplexer can be operated in two modes:

- During a normal multiplexer cycle, the signals from the A0, A2, A1, and A3 pins are selected.
- During the alternate multiplexer cycle, the temperature signal (TEMP) is selected, along with the signal sources shown in Table 1.

The alternate mux cycles are usually performed infrequently (e.g. every second) by the MPU. Table 1 details the regular and alternative MUX sequences. Missing samples due to an ALT multiplexer sequence are filled in by the CE.

Table 1: Inputs Selected in Regular and Alternate Multiplexer Cycles

Regular MUX Sequence				ALT MUX Sequence			
Mux State				Mux State			
0	**1**	**2**	**3**	**0**	**1**	**2**	**3**
A0	A1	A2	A3	TEMP	A1	V3P3D	A3

In a typical application, A1 and A3 are connected to current sensors that sense the current on each branch of the line voltage. A0 and A2 are typically connected to voltage sensors through resistor dividers. The multiplexer control circuit is clocked by CK32, the 32.768 kHz clock from the PLL block, and launches with each new pass of the CE program.

1.2.2 A/D Converter (ADC)

A single delta-sigma A/D converter digitizes the voltage and current inputs to the 78M6613. The resolution of the ADC is 22 bits. Conversion time is two cycles of the CK32 clock.

Initiation of each ADC conversion is controlled by the multiplexer control circuit as described previously. At the end of each ADC conversion, the FIR filter output data is stored into the CE DRAM location.

1.2.3 FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE DRAM location determined by the multiplexer selection.

1.2.4 Voltage References

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques. The reference is trimmed to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

1.2.5 Temperature Sensor

The 78M6613 includes an on-chip temperature sensor implemented as a bandgap reference. It is used to determine the die temperature. The MPU reads the temperature sensor output during alternate multiplexer cycles. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see Section 3.3 Temperature Compensation).

1.2.6 Functional Description

The AFE functions as a data acquisition system, controlled by the MPU. The input signals (A0, A1, A2, and A3) are sampled and the ADC counts obtained are stored in CE DRAM where they can be accessed by the CE and, if necessary, by the MPU. Alternate multiplexer cycles are initiated less frequently by the MPU to gather access to the slow temperature signal.

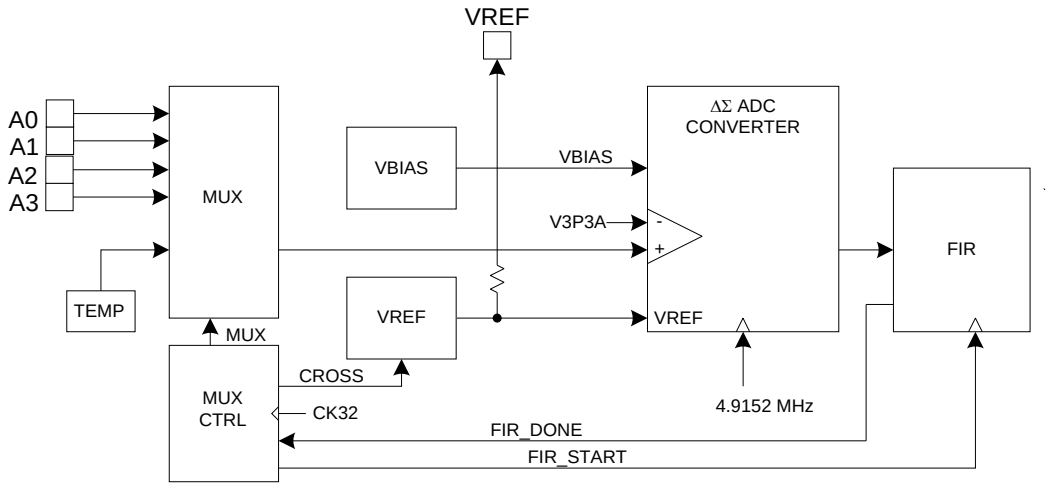


Figure 2: AFE Block Diagram

1.3 Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for narrowband VARh calculations).
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.

CE code is provided by Silergy as a part of the application firmware available. The CE is not programmable by the user. Measurement algorithms in the CE code can be customized by Silergy upon request.

The CE program resides in Flash memory. Common access to Flash memory by CE and MPU is controlled by a memory share circuit. Allocated Flash space for the CE program cannot exceed 1024 words (2KB).

The CE DRAM can be accessed by the CE and the MPU. Holding registers are used to convert 8-bit wide MPU data to/from 32-bit wide CE DRAM data, and wait states are inserted as needed, depending on the frequency of CKMPU. The CE DRAM contains 128 32-bit words. The MPU can read and write the CE DRAM as the primary means of data communication between the two processors. CE hardware issues an interrupt when accumulation is complete.

1.4 80515 MPU Core

The 78M6613 includes an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 5 MHz (4.9152 MHz) clock results in a processing throughput of 5 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (in average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency. Actual processor clocking speed can be adjusted to the total processing demand of the application (measurement calculations, memory management and I/O management).

Typical power and energy measurement functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of Silergy's standard library. MPU Memory Organization, Special Function Registers, Interrupts, Counters, and other controls are described in the applicable firmware documentation.

1.4.1 UART

The 78M6613 includes a UART that can be programmed to communicate with a variety of external devices. The UART is a dedicated 2-wire serial interface, which can communicate with an external device at up to 38,400 bits/s. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38,400 bps.

1.4.2 Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from certain DIO pins, see the DIO Ports section). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

1.5 On-Chip Resources

1.5.1 Oscillator

The 78M6613 oscillator drives a standard 32.768 kHz watch crystal. These crystals are accurate and do not require a high-current oscillator circuit. The 78M6613 oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability.

1.5.2 PLL and Internal Clocks

Timing for the device is derived from the 32.768 kHz oscillator output. On-chip timing functions include the MPU master clock and the delta-sigma sample clock. In addition, the MPU has two general counter/timers.

The ADC master clock, CKADC, is generated by an on-chip PLL. It multiplies the oscillator output frequency (CK32) by 150.

The CE clock frequency is always CK32 * 150, or 4.9152 MHz, where CK32 is the 32 kHz clock. The MPU clock frequency is scalable from 4.9152 MHz down to 38.4 kHz. The circuit can also generate a 2x MPU clock for use by the emulator.

1.5.3 Temperature Sensor

The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see Section 3.3 Temperature Compensation).

1.5.4 Flash Memory

The 78M6613 includes 32 KB of on-chip Flash memory. The Flash memory primarily contains MPU and CE program code. It also contains images of the CE DRAM, MPU RAM, and I/O RAM. On power-up, before enabling the CE, the MPU copies these images to their respective locations. Allocated Flash space for the CE program cannot exceed 1024 words (2 KB).

MPU RAM: The 78M6613 includes 2KB of static RAM memory on-chip (XRAM) plus 256B of internal RAM in the MPU core. The 2KB of static RAM are used for data storage during normal MPU operations.

CE DRAM: The CE DRAM is the working data memory of the CE (128 32-bit words). The MPU can read and write the CE DRAM as the primary means of data communication between the two processors.

1.5.5 Digital I/O

The device includes up to 10 pins of general purpose digital I/O. When configured as inputs, these pins are 5V compatible (no current-limiting resistors are needed). On reset or power-up, all DIO pins are inputs until they are configured for the desired direction under MPU control.

When driving LEDs, relay coils etc., the DIO pins should sink the current into ground (as shown in Figure 3, right), not source it from V3P3 (as in Figure 3, left).

If more than one input is connected to the same resource, the resources are combined using a logical OR.

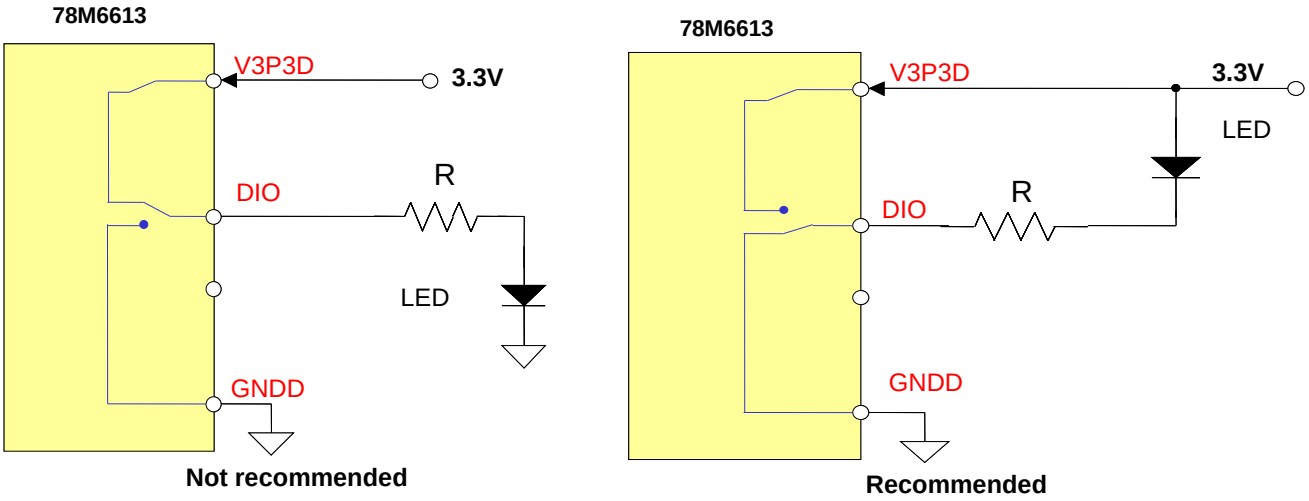


Figure 3: Connecting an External Load to DIO Pins

1.5.6 Hardware Watchdog Timer

In addition to the basic watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, watchdog timer (WDT) is included in the device. It uses the crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time the WDT overflows, and the part is reset as if the RESET pin were pulled high, except that the I/O RAM bits will be maintained. 4096 oscillator cycles (or 125 ms) after the WDT overflow, the MPU will be launched from program address 0x0000. Asserting ICE_E will deactivate the WDT.

1.5.7 Program Security

When enabled, the security feature limits the ICE to global Flash erase operations only. All other ICE operations are blocked. This guarantees the security of the user's MPU and CE program code. Security is enabled by MPU code that is executed in a 32 cycle preboot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the Flash, followed by a chip reset.

1.5.8 Test Ports

TMUXOUT Pin: One out of 16 digital or 8 analog signals can be selected to be output on the TMUXOUT pin. The function of the multiplexer is described in the applicable firmware documentation.

2 Functional Description

2.1 Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t)I(t)dt$$

The following formulae apply for wide band mode (true RMS):

- P = ∑ (i(t) * v(t))
- Q = √(S² – P²)
- S = V * I
- V = √∑v(t)²
- I = √∑i(t)²

For a practical measurement, not only voltage and current amplitudes, but also phase angles and harmonic content may change constantly. Thus, simple RMS measurements are inherently inaccurate, and true RMS measurements must be utilized. A modern solid-state electricity Power and Energy Measurement IC such as the 78M6613 functions by emulating the integral operation above, i.e. it processes current and voltage samples through an ADC at a constant frequency. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied with the time period of sampling will yield an accurate quantity for the momentary energy. Summing up the momentary energy quantities over time will result in accumulated energy.

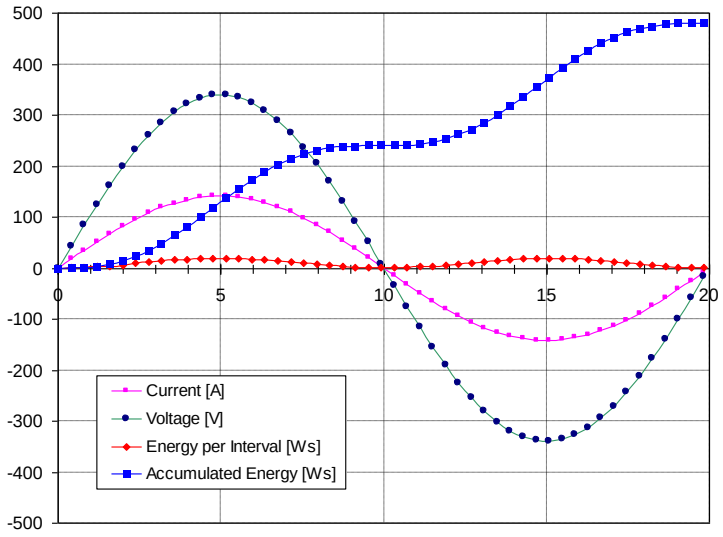


Figure 4: Voltage. Current, Momentary and Accumulated Energy

Figure 4 shows the shapes of V(t), I(t), the momentary power and the accumulated power, resulting from 50 samples of the voltage and current signals over a period of 20 ms. The application of 240 VAC and 100 A results in an accumulation of 480 Ws (= 0.133 Wh) over the 20 ms period, as indicated by the Accumulated Power curve. The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

For actual measurement equations, refer to the applicable firmware documentation.

2.2 Reset Behavior

Reset Mode: When the RESET pin is pulled high all digital activity stops. The oscillator continues to run. Additionally, all I/O RAM bits are set to their default states.

Once initiated, the reset mode will persist until the reset timer times out. This will occur in 4096 CK32 clock cycles (32768 Hz clock cycles from PLL block) after RESET goes low, at which time the MPU will begin executing its preboot and boot sequences from address 00.

2.3 Data Flow

The data flow between CE and MPU is shown in Figure 5. In a typical application, the 32-bit compute engine (CE) sequentially processes the samples from the voltage inputs on pins A0, A1, A2, and A3, performing calculations to measure active power (Wh), reactive power (VARh), A^2h, and V^2h for four-quadrant measurements. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

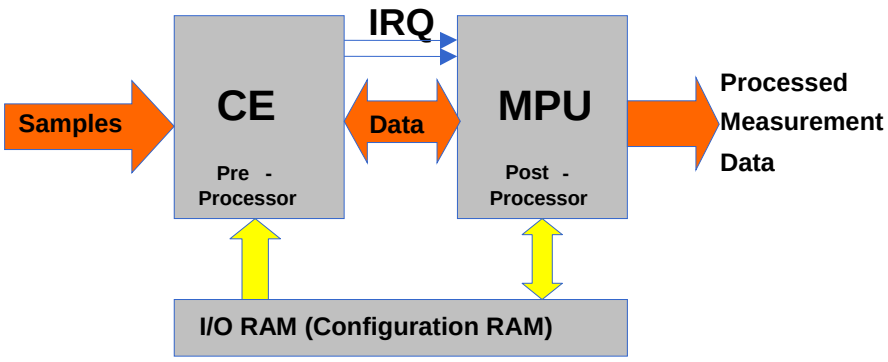


Figure 5: MPU/CE Data Flow

2.4 CE/MPU Communication

Figure 6 shows the functional relationship between CE and MPU. The CE is controlled by the MPU via shared registers in the I/O RAM and by registers in the CE DRAM. The CE outputs two interrupt signals to the MPU to indicate when the CE is actively processing data and when the CE is updating data to the output region of the CE DRAM.

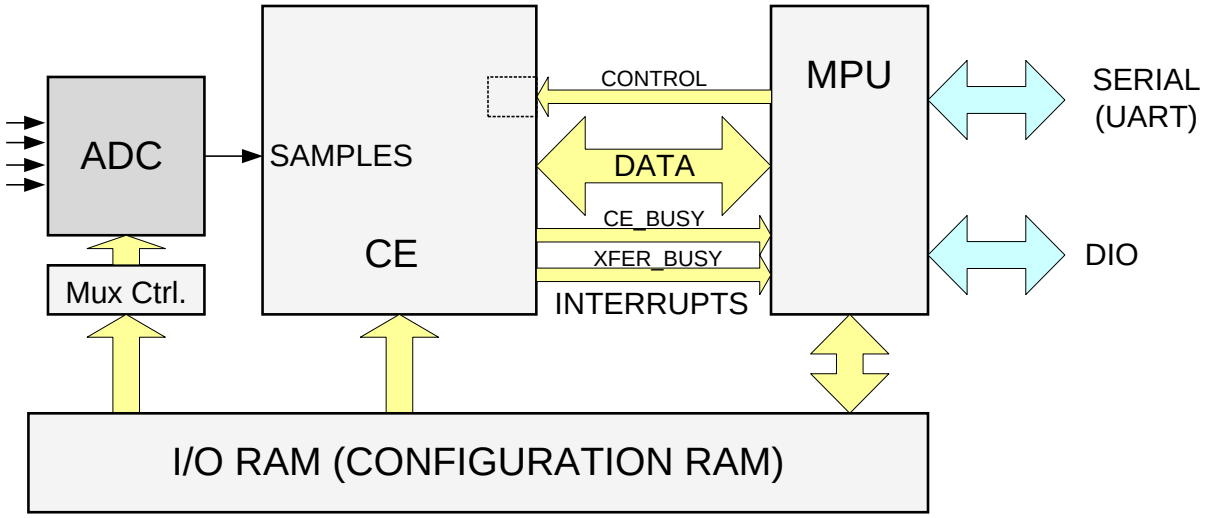


Figure 6: MPU/CE Communication

3 Application Information

3.1 Connection of Sensors (CT, Resistive Shunt)

Figure 7, Figure 8, and Figure 9 show how resistive voltage dividers, resistive current shunts, and current transformers are connected to the voltage and current inputs of the 78M6613.

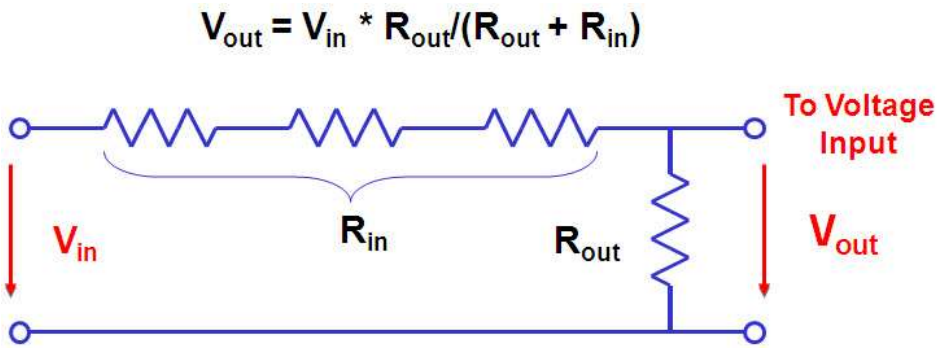


Figure 7: Resistive Voltage Divider

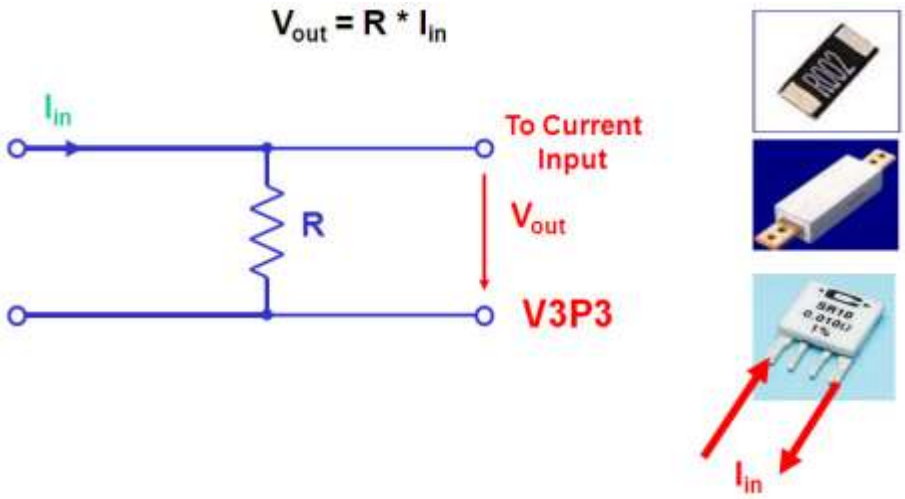


Figure 8: Resistive Current Shunt

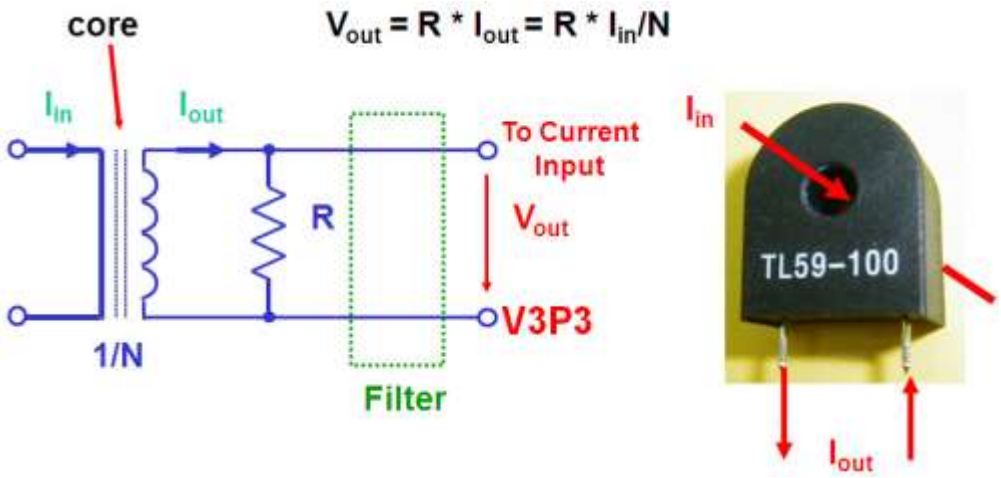


Figure 9: Current Transformer

3.2 Temperature Measurement

Measurement of absolute temperature uses the on-chip temperature sensor while applying the following formula:

$$T = \frac{(N(T) - N_n)}{S_n} + T_n$$

In the above formula, T is the temperature in °C, N(T) is the ADC count at temperature T, N_n is the ADC count at 25°C, S_n is the sensitivity in LSB/°C and T_n is +25°C.

Example: At 25°C a temperature sensor value of 518,203,584 (N_n) is read by the ADC by a 78M6613 in the 32-pin QFN package. At an unknown temperature T the value 449,648,000 is read at (N(T)). The absolute temperature is then determined by dividing both N_n and N(T) by 512 to account for the 9-bit shift of the ADC value and then inserting the results into the above formula, using –2220 for LSB/°C:

$$T = \frac{449{,}648{,}000 - 518{,}203{,}584}{512 \cdot (-2220)} + 25C = 85.3°C$$

3.3 Temperature Compensation

Temperature Coefficients: The internal voltage reference is calibrated during device manufacture.

The temperature coefficients TC1 and TC2 are given as constants that represent typical component behavior (in μV/°C and μV/°C^2, respectively).

Since TC1 and TC2 are given in μV/°C and μV/°C^2, respectively, the value of the VREF voltage (1.195V) has to be taken into account when transitioning to PPM/°C and PPM/°C^2. This means that PPMC = 26.84*TC1/1.195, and PPMC2 = 1374*TC2/1.195).

Temperature Compensation: The CE provides the bandgap temperature to the MPU, which then may digitally compensate the power outputs for the temperature dependence of VREF.

The MPU, not the CE, is entirely in charge of providing temperature compensation. The MPU applies the following formula to determine any gain adjustments. In this formula $TEMP\_X$ is the deviation from nominal or calibration temperature expressed in multiples of 0.1°C:

$$GAIN\_ADJ = 16385 + \frac{TEMP\_X \cdot PPMC}{2^{14}} + \frac{TEMP\_X^2 \cdot PPMC2}{2^{23}}$$

In a power and energy measurement unit, the 78M6613 is not the only component contributing to temperature dependency. A whole range of components (e.g. current transformers, resistor dividers, power sources, filter capacitors) will contribute temperature effects. Since the output of the on-chip temperature sensor is accessible to the MPU, temperature-compensation mechanisms with great flexibility are possible (e.g. system-wide temperature correction over the entire unit rather than local to the chip).

3.4 Connecting 5V Devices

All digital input pins of the 78M6613 are compatible with external 5V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5V devices.

3.5 UART (TX/RX)

The RX pin should be pulled down by a 10 kΩ resistor and optionally protected by a 100 pF ceramic capacitor, as shown in Figure 10.

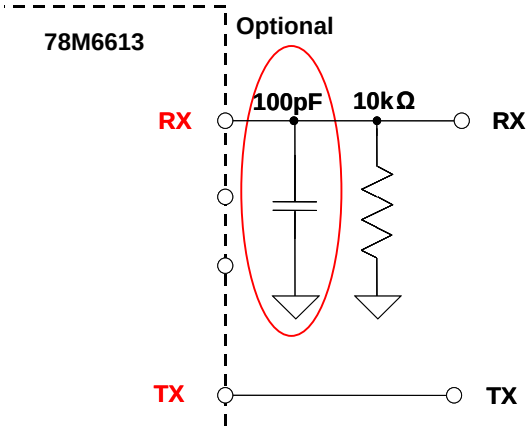


Figure 10: Connections for the RX Pin

3.6 Reset Function and Reset Pin Connections

The 78M6613 requires an external reset circuit to drive the RESET input pin. The reset is used to prevent the 78M6613 from operating at supply voltages outside the recommended operating conditions. Reset ensures the device is set to a known set of initial conditions and that it begins executing instructions from a predetermined starting address.

The reset can be forced by applying a high level to the RESET pin. The reset input is internally filtered (low-pass filter) in order to eliminate spurious reset conditions that can be triggered in a noisy environment. For this reason the RESET pin must be asserted (high) for at least 1µs in order to initiate a reset sequence.

The external reset circuitry should be designed in order to hold the RESET pin high (active) whenever V3P3D is below normal operating level. Refer to Section 4.3, Recommended Operating Conditions. Figure 11 shows the behavior of the external reset circuitry.

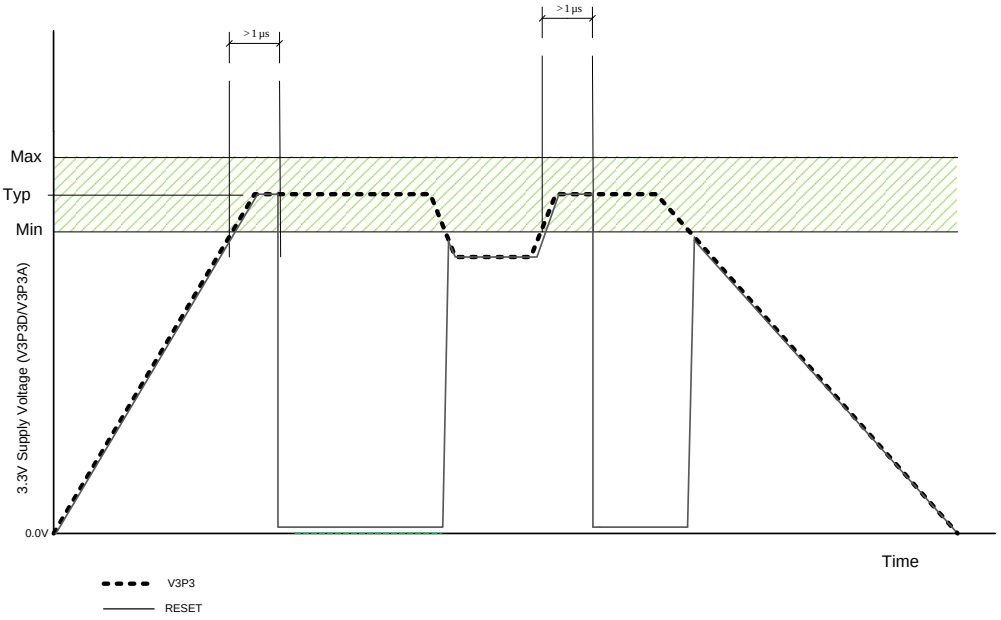


Figure 11: 78M6613 External Reset Behavior

The RESET signal can be generated in a number of different ways. For example, a voltage supervisory device such as Maxim's MAX810S can be used to implement the reset/supply voltage supervisory function as shown in Figure 12.

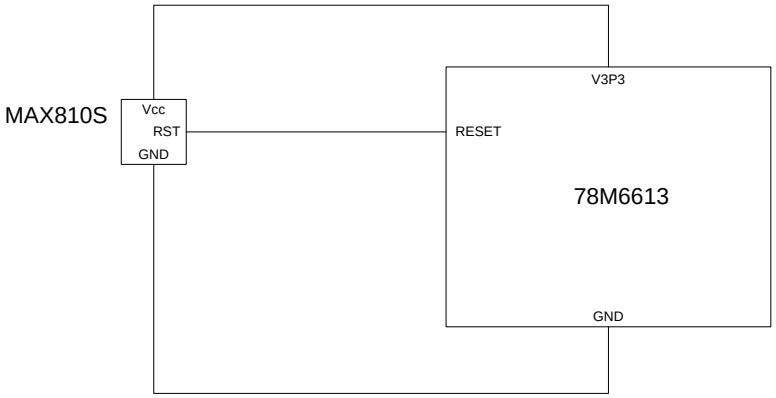


Figure 12: MAX810S Connections to the 78M6613

An alternate solution using discrete components can be used. Figure 13 shows an implementation using a shunt regulator and two transistors.

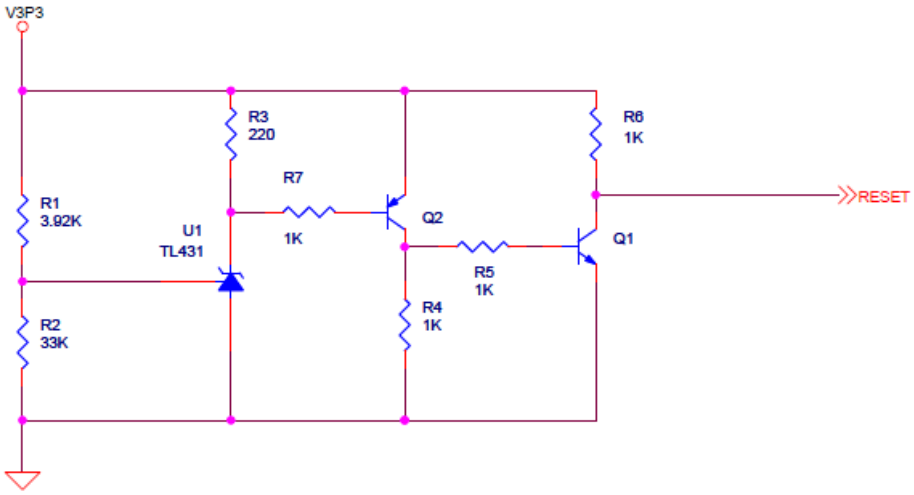


Figure 13: Reset Generator Based On TL431 Shunt Regulator

As long as V3P3 is below the 2.79V threshold set by the voltage divider of R1 and R2, U1 will not conduct current, the base of Q2 will be at the same potential as its emitter, so Q1 will be turned off. With no current flowing in the collector of Q2, the base of Q1 will be low, Q1 will be turned off, and RESET will track V3P3. When the V3P3 rises above 2.79V, the TL431 starts to conduct, the base of Q2 is be pulled low, turning on Q2. This drives the base of Q1 high, turning Q1 on and pulling RESET low. The inherent turn-on and turn-off delays of the TL4313 provide the ~1µs delay required to ensure proper resetting of the 78M6613.

3.7 Connecting the Emulator Port Pins

It is important to bring out the ICE_E pin to the programming interface in order to create a way for reprogramming parts that have the Flash *SECURE* bit (SFR 0xB2[6]) set. Providing access to ICE_E ensures that the part can be reset between erase and program cycles, which will enable programming devices to reprogram the part. The reset required is implemented with a watchdog timer reset (i.e. the hardware WDT must be enabled).

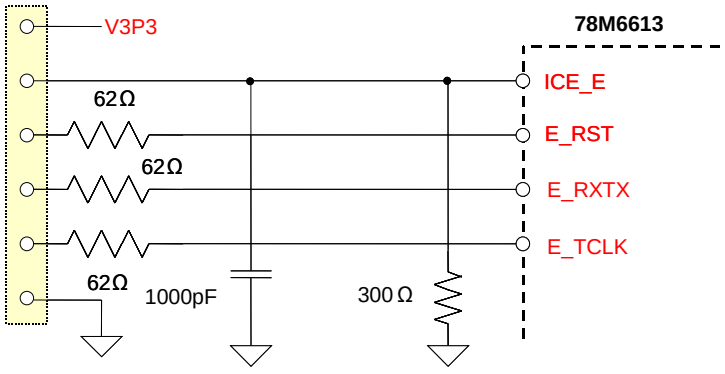


Figure 14: External Components for the Emulator Interface

3.8 Crystal Oscillator

The oscillator of the 78M6613 drives a standard 32.768 kHz watch crystal. The oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability. Good layouts will have XIN and XOUT shielded from each other.

Since the oscillator is self-biasing, an external resistor must not be connected across the crystal.

3.9 Flash Programming

Operational or test code can be programmed into the Flash memory using either an in-circuit emulator or the Flash Programmer Module (TFP-2) available from Silergy. The Flash programming procedure uses the E_RST, E_RXTX, and E_TCLK pins.

3.10 MPU Firmware Library

Any application-specific MPU functions mentioned above are available from Silergy as a standard ANSI C library and as ANSI “C” source code. The code is pre-programmed in Demonstration and Evaluation Kits for the 78M6613 IC and can be pre-programmed into engineering IC samples for system evaluation. The application code allows for quick and efficient evaluation of the IC without having to write firmware or having to purchase an in-circuit emulator (ICE). A Software Licensing Agreement (SLA) can be signed to receive either the source Flash HEX file for use in a production environment or (partial) source code and SDK documentation for modification.

3.11 Measurement Calibration

Once the 78M6613 Power and Energy Measurement device has been installed in a measurement system, it is typically calibrated for tolerances of the current sensors, voltage dividers and signal conditioning components. The device can be calibrated using a single gain and a single phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by certain types of current sensors.

Due to the flexibility of the MPU firmware, any calibration method, such as calibration based on energy, or current and voltage can be implemented. It is also possible to implement segment-wise calibration (depending on current range). Silergy software supports a “quick cal” method.

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Supplies and Ground Pins:	
V3P3	-0.5 V to 4.6 V
GNDD, GNDA	-0.5 V to +0.5 V
Analog Output Pins:	
VREF	-10 mA to +10 mA, -0.5 V to V3P3+0.5 V
Analog Input Pins:	
A0, A1, A2, A3	-10 mA to +10 mA -0.5 V to V3P3+0.5 V
XIN, XOUT	-10 mA to +10 mA -0.5 V to 3.0 V
All Other Pins:	
Configured as Digital Inputs	-10 mA to +10 mA, -0.5 to 6 V
Configured as Digital Outputs	-15 mA to +15 mA, -0.5 V to V3P3D+0.5 V
All other pins	-0.5 V to V3P3D+0.5 V
Operating junction temperature (peak, 100 ms)	+140 °C
Operating junction temperature (continuous)	+125 °C
Storage temperature	-45 °C to +165 °C
Soldering temperature (10 second duration)	+250 °C
ESD stress on all pins	±4 kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

4.2 Recommended External Components

Name	From	To	Function	Value	Unit
C1	V3P3A	GNDA	Bypass capacitor for 3.3V supply.	≥0.1±10%	µF
CSYS	V3P3D	GNDD	Bypass capacitor for V3P3D.	≥0.1±10%	µF
XTAL	XIN	XOUT	32.768 kHz crystal – electrically similar to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5 pF.	32.768	kHz
CXS †	XIN	GND	Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board).	27±10%	pF
CXL †	XOUT	GND		27±10%	pF

† Depending on trace capacitance, higher or lower values for CXS and CXL must be used. Capacitance from XIN to GND and XOUT to GND (combining pin, trace and crystal capacitance) should be 35 pF to 37 pF.

4.3 Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
3.3V Supply Voltage (V3P3)	Normal Operation	3.0	3.3	3.6	V
Operating Temperature		-40		+85	ºC

4.4 Performance Specifications

4.4.1 Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage, V_{IH}		2			V
Digital low-level input voltage, V_{IL}				0.8	V
Input pull-up current, I_{IL} E_RXTX, E_RST, CKTEST Other digital inputs	VIN=0V, ICE_E=1	 10 10 -1	 0	 100 100 1	 µA µA µA
Input pull down current, I_{IH} ICE_E Other digital inputs	VIN=V3P3	 10 -1	 0	 100 1	 µA µA

4.4.2 Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V3P3 –0.4			V
	I_{LOAD} = 15 mA	V3P3-0.6[1]			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0		0.4	V
	I_{LOAD} = 15 mA			0.8[1]	V

[1] Guaranteed by design; not production tested.

4.4.3 Supply Current

Parameter	Condition	Min	Typ	Max	Unit
V3P3A + V3P3D current	Normal Operation, **V3P3**=3.3V, ICE Disabled		8.1	10.3	mA
V3P3A + V3P3D current vs. MPU clock frequency	Same conditions as above		0.5		mA/ MHz
V3P3A + V3PD current, Write Flash	Normal Operation as above, except write Flash at maximum rate, ADC & CE Disabled		9.1	10	mA

4.4.4 Crystal Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power to Crystal	Crystal connected			1	μW
XIN to XOUT Capacitance			3		pF
Capacitance to GND XIN XOUT			 5 5		 pF pF

4.4.5 VREF

Unless otherwise specified, *VREF_DIS*=0

Parameter	Condition	Min	Typ	Max	Unit
VREF output voltage, VNOM(25)	Ta = 22ºC	1.193	1.195	1.197	V
VREF chop step				50	mV
VREF output impedance	*VREF_CAL* =1, I_{LOAD} = 10 μA, -10 μA			2.5	kΩ
VNOM definition*	$VNOM(T) = VREF(22) + (T-22)TC1 + (T-22)^2 TC2$				V
VREF temperature coefficients TC1 TC2		124.4 - 2.435*TRIMT -0.265 + 0.00106*TRIMT			 μV/ºC μV/°C²
VREF aging			±25		ppm/ year
VREF(T) deviation from VNOM(T) $\frac{VREF(T) - VNOM(T)}{VNOM} \frac{10^6}{62}$	Ta = -40ºC to +85ºC	-40[1]		+40[1]	ppm/º C

* This relationship describes the nominal behavior of VREF at different temperatures.

4.4.6 ADC Converter, V3P3 Referenced

VREF_DIS=0, LSB values do not include the 9-bit left shift at CE input.

Parameter	Condition	Min	Typ	Max	Unit
Recommended Input Range (Vin-**V3P3A**)		-250		250	mV peak
Voltage to Current Crosstalk: $\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$	*Vin* = 200 mV peak, 65 Hz, on A0 *Vcrosstalk* = largest measurement on A1 or A3	-10[1]		10[1]	µV/V
THD (First 10 harmonics) 250 mV-pk 20 mV-pk	Vin=65 Hz, 64 kpts FFT, Blackman-Harris window		 -75 -90		 dB dB
Input Impedance	Vin=65 Hz	40		90	kΩ
Temperature coefficient of Input Impedance	Vin=65 Hz		1.7		Ω/°C
LSB size	*FIR_LEN=0* *FIR_LEN=1*		357 151		nV/LSB
Digital Full Scale	*FIR_LEN=0* *FIR_LEN=1*		±884736 ±2097152		LSB
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\ 357nV/V_{IN}}{100\Delta V3P3A/3.3}$	Vin=200 mV pk, 65 Hz V3P3=3.0V, 3.6V			50	ppm/%
Input Offset (Vin-**V3P3A**)		-10		10	mV

4.4.7 Temperature Sensor

Parameter	Condition	Min	Typ	Max	Unit
Nominal Sensitivity (S_n)	*FIR_LEN=0* *FIR_LEN=1*		-669 -1585		LSB/ºC
Nominal (N_n) †	*FIR_LEN=0* *FIR_LEN=1*		+429301 +1017558		LSB
Temperature Error $ERR = T - \left(\frac{(N(T) - N_n)}{S_n} + T_n\right)$	T_A = -40ºC to +85ºC Tn = 25°C	-10[1]		+10[1]	ºC

† N_n is measured at T_n during calibration and is stored in MPU or CE for use in temperature calculations.

[1] Guaranteed by design; not production tested.

4.5 Timing Specifications

4.5.1 RAM and Flash Memory

Parameter	Condition	Min	Typ	Max	Unit
CE DRAM wait states	CKMPU = 4.9152 MHz	5			Cycles
	CKMPU = 1.25 MHz	2			Cycles
	CKMPU = 614 kHz	1			Cycles
Flash write cycles	-40 °C to +85 °C	20,000			Cycles
Flash data retention	25 °C	100			Years
Flash data retention	85 °C	10			Years
Flash byte writes between page or mass erase operations				2	Cycles

4.5.2 RESET

Parameter	Condition	Min	Typ	Max	Unit
Reset pulse fall time				1	µs
Reset pulse width		5			µs

4.5.3 Typical Performance Data

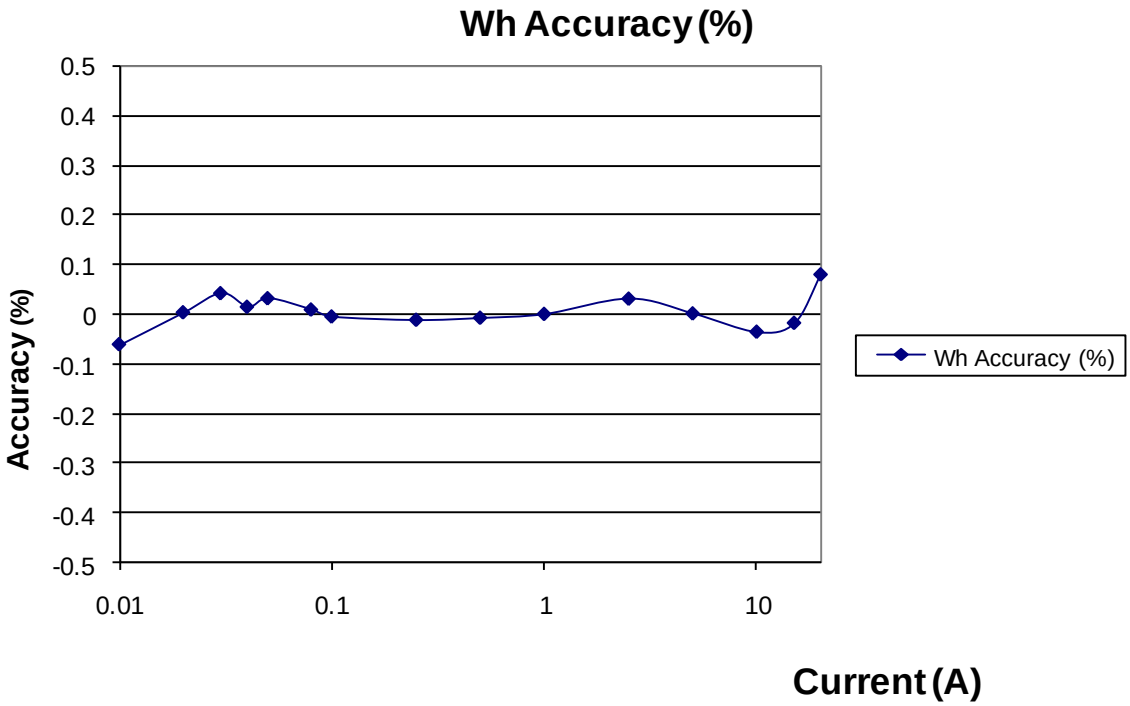


Figure 15: Wh Accuracy, 10 mA to 20 A at 120 V/60 Hz and Room Temperature Using a 4 mΩ Current Shunt

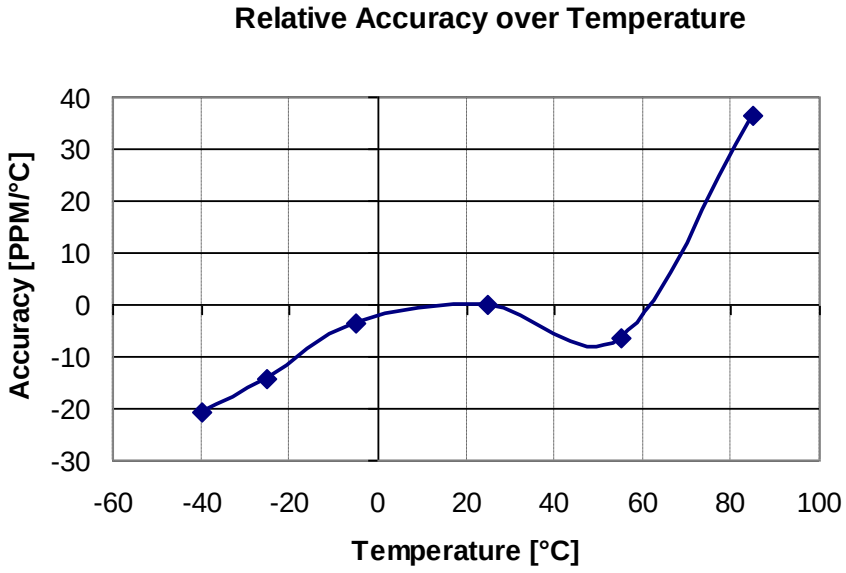


Figure 16: Typical Measurement Accuracy over Temperature Relative to 25°C

5 Packaging

5.1 Pinout

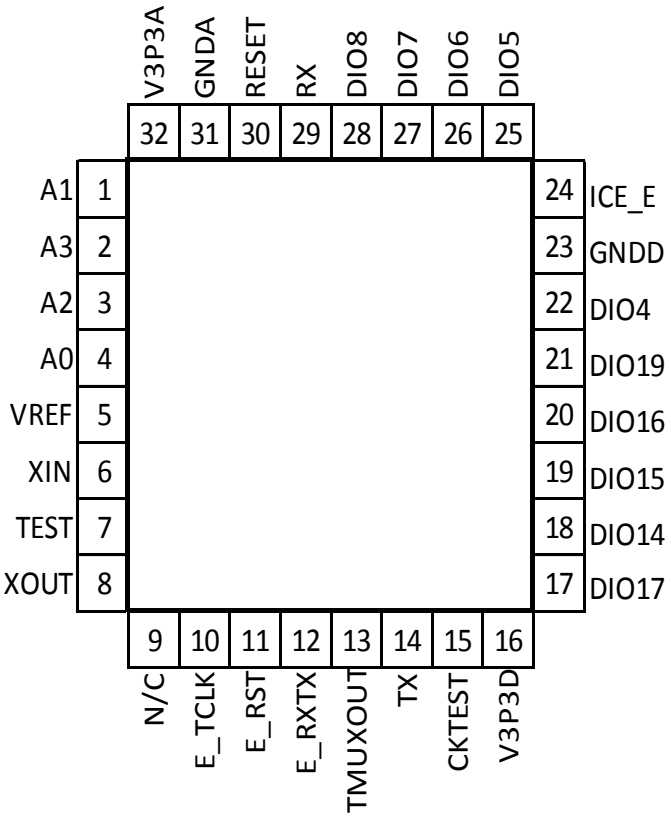
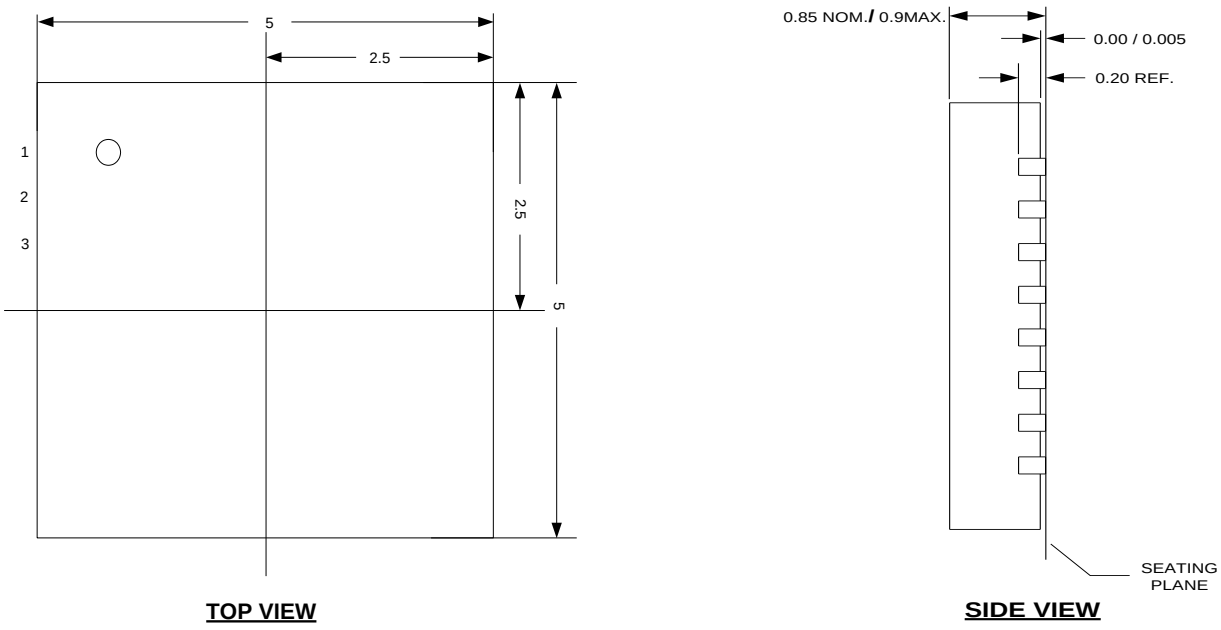
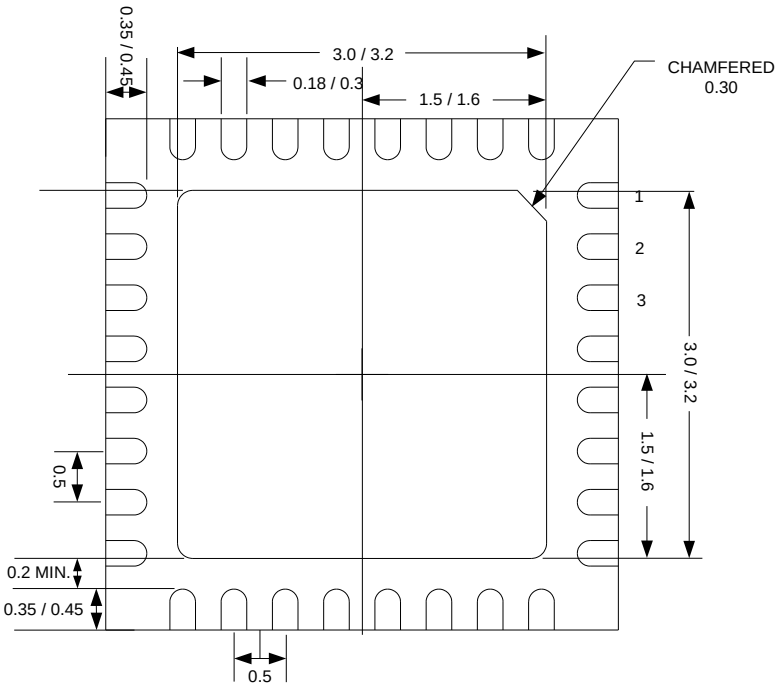


Figure 17: 32-Pin QFN Pinout

5.2 Package Outline (QFN 32)

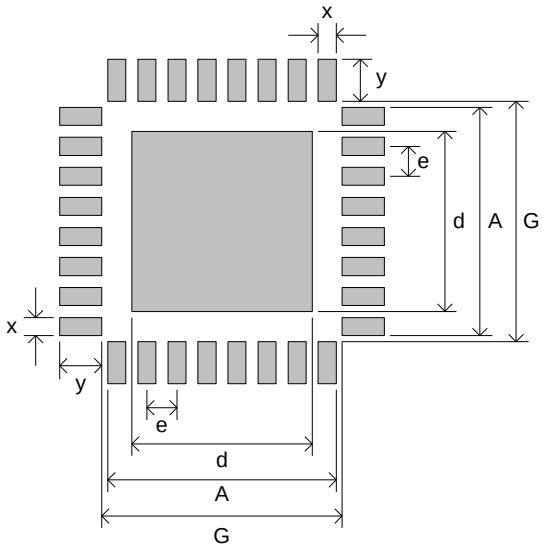




NOTE: Controlling dimensions are in mm.

Figure 18: Package Outline (QFN 32)

5.3 Recommended PCB Land Pattern for the QFN-32 Package



Symbol	Description	Min	Typ	Max
e	Lead pitch		0.50 mm	
x			0.28 mm	0.28 mm
y			0.69 mm	
d	See Note 1		3.00 mm	
A				3.78 mm
G		3.93 mm		

Note 1: Do not place unmasked vias in region denoted by dimension “d”.

Note 2: Soldering of bottom internal pad not required for proper operation of either commercial or industrial temperature rated versions.

Figure 19: Recommended PCB Land Pattern Dimensions

6 Pin Descriptions

6.1 Power/Ground Pins

Name	Type	Circuit	Description
GNDA GNDD	P	–	These pins should be connected directly to the ground plane.
V3P3A V3P3D	P	–	A 3.3V power supply should be connected to these pins.

6.2 Analog Pins

Name	Type	Circuit	Description
A0, A1, A2, A3	I	5	Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to either the outputs of current sensors or the outputs of resistor dividers (voltage sensors). **Unused pins must be connected to V3P3.**
VREF	O	8	Voltage Reference for the ADC. This pin is left unconnected. Never use as an external reference.
XIN XOUT	I	7	Crystal Inputs. A 32 kHz crystal should be connected across these pins. Typically, a 27 pF capacitor is also connected from each pin to GND. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details.

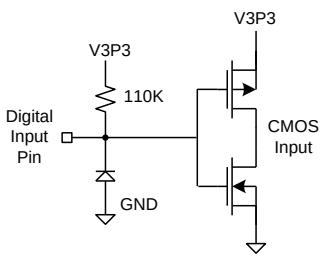
Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under “I/O Equivalent Circuits”.

6.3 Digital Pins

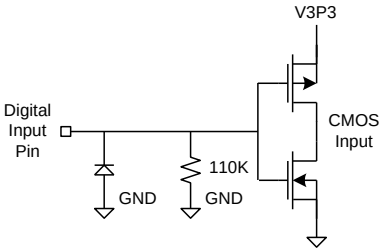
Name	Type	Circuit	Description
DIO4 DIO5 DIO6 DIO7 DIO8 DIO14 DIO15 DIO16 DIO17 DIO19	I/O	3, 4	DIO pins. **If unused, these pins must be configured as DIOs and set to outputs by the firmware.**
E_RXTX, E_RST	I/O	1, 4	Emulator port pins (when ICE_E pulled high) .
E_TCLK	O	4	
ICE_E	I	2	ICE enable. When zero, E_RST, E_TCLK, and E_RXTX are disabled. For production units, this pin should be pulled to GND to disable the emulator port. This pin should be brought out to the programming interface in order to create a way for reprogramming parts that have the *SECURE* bit set.
CKTEST	O	4	Clock PLL output.
TMUXOUT	O	4	Digital output test multiplexer.
RESET	I	3	This input pin resets the chip into a known state. For normal operation, this pin should be pulled low. To force the device into reset state, it should be pulled high. Refer to Section 3.6 for RESET pin connections, use, and relevant external circuitry.
RX	I	3	UART input. **If unused, this pin must be terminated to V3P3 or GND.**
TX	O	4	UART output.
TEST	I	7	Enables Production Test. **Must be grounded in normal operation.**

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified on the following page.

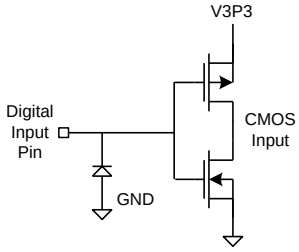
7 I/O Equivalent Circuits



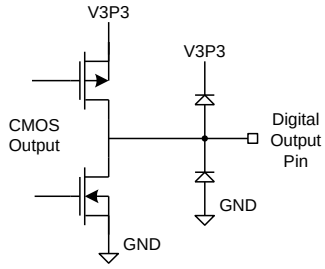
Digital Input Equivalent Circuit
Type 1:
Standard Digital Input or
pin configured as DIO Input
with Internal Pull-Up



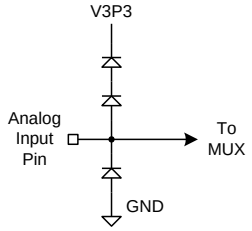
Digital Input
Type 2:
Pin configured as DIO Input
with Internal Pull-Down



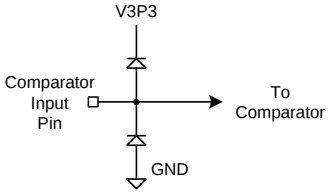
Digital Input Type 3:
Standard Digital Input or
pin configured as DIO Input



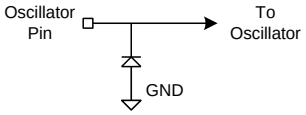
Digital Output Equivalent Circuit
Type 4:
Standard Digital Output or
pin configured as DIO Output



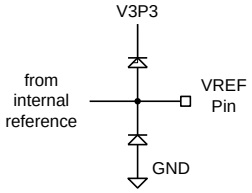
Analog Input Equivalent Circuit
Type 5:
ADC Input



Comparator Input Equivalent Circuit
Type 6:
Comparator Input



Oscillator Equivalent Circuit
Type 7:
Oscillator I/O



VREF Equivalent Circuit
Type 8:
VREF

Figure 20: I/O Equivalent Circuits

8 Ordering Information

Part	Package	Option	Ordering Number	IC Marking
78M6613	32-pin QFN (Lead(Pb)-Free)	Bulk	78M6613-IM/F	78M6613-IM
		Tape & Reel	78M6613-IMR/F	
		*Programmed, Bulk	78M6613-IM/F/P	
		*Programmed, Tape & Reel	78M6613-IMR/F/P	

*Contact the factory for more information on programmed part options.

9 Contact Information

For more information about the 78M6613 or other Silergy products, contact technical support at support.em@silergy.com

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1.0	11/10	First publication.	—
1.1	3/11	In Section 6.3, corrected the description of the RESET pin.	30
2	1/12	Rebrand only.	1
3	4/16	Rebrand only	