Ideal Diode Controller with Reverse Input Protection

FEATURES

- **Reduces Power Dissipation by Replacing a Power Schottky Diode**
- **Wide Operating Voltage Range: 4V to 80V**
- **Reverse Input Protection to –40V**
- **Low 9µA Shutdown Current**
- Low 150µA Operating Current
- Smooth Switchover without Oscillation
- Controls Single or Back-to-Back N-Channel MOSFETs
- Available in 6-Pin (2mm × 3mm) DFN, 8-Lead MSOP and 8-Lead SO Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive Battery Protection
- Redundant Power Supplies
- Supply Holdup
- Telecom Infrastructure
- Computer Systems/Servers
- Solar Systems

DESCRIPTION

The LTC®4359 is a positive high voltage ideal diode controller that drives an external N-channel MOSFET to replace a Schottky diode. It controls the forward-voltage drop across the MOSFET to ensure smooth current delivery without oscillation even at light loads. If a power source fails or is shorted, a fast turn-off minimizes reverse current transients. A shutdown mode is available to reduce the quiescent current to 9µA for load switch and 14µA for ideal diode applications.

When used in high current diode applications, the LTC4359 reduces power consumption, heat dissipation, voltage loss and PC board area. With its wide operating voltage range, the ability to withstand reverse input voltage, and high temperature rating, the LTC4359 satisfies the demanding requirements of both automotive and telecom applications. The LTC4359 also easily ORs power sources in systems with redundant supplies.

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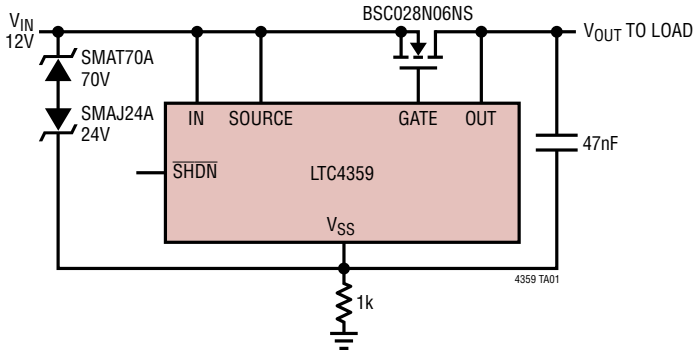
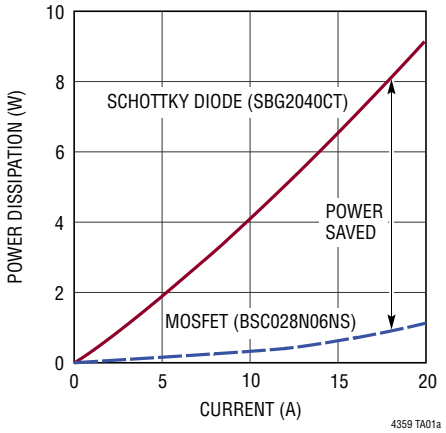
TYPICAL APPLICATION

12V, 20A Automotive Reverse-Battery Protection



Power Dissipation vs Load Current

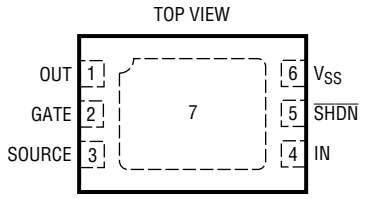


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

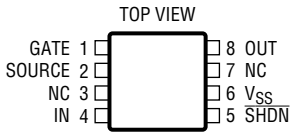
IN, SOURCE, $\overline{SHDN}$ ..... –40V to 100V
OUT (Note 3) ..... –2V to 100V
IN – OUT ..... –100V to 100V
IN – SOURCE ..... –1V to 80V
GATE – SOURCE (Note 4) ..... –0.3V to +10V

Operating Ambient Temperature Range
LTC4359C ..... 0°C to 70°C
LTC4359I ..... –40°C to 85°C
LTC4359H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS, SO Packages ..... 300°C

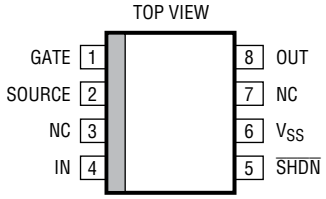
PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 64°C/W
EXPOSED PAD (PIN 7) PCB V_{SS} CONNECTION OPTIONAL



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER INFORMATION

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4359CDCB#TRMPBF	LTC4359CDCB#TRPBF	LFKF	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC4359IDCB#TRMPBF	LTC4359IDCB#TRPBF	LFKF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4359HDCB#TRMPBF	LTC4359HDCB#TRPBF	LFKF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
TUBE	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4359CMS8#PBF	LTC4359CMS8#TRPBF	LTFKD	8-Lead Plastic MSOP	0°C to 70°C
LTC4359IMS8#PBF	LTC4359IMS8#TRPBF	LTFKD	8-Lead Plastic MSOP	–40°C to 85°C
LTC4359HMS8#PBF	LTC4359HMS8#TRPBF	LTFKD	8-Lead Plastic MSOP	–40°C to 125°C
LTC4359CS8#PBF	LTC4359CS8#TRPBF	4359	8-Lead Plastic SO	0°C to 70°C
LTC4359IS8#PBF	LTC4359IS8#TRPBF	4359	8-Lead Plastic SO	–40°C to 85°C
LTC4359HS8#PBF	LTC4359HS8#TRPBF	4359	8-Lead Plastic SO	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC4359IMS8#WPBF	LTC4359IMS8#WTRPBF	LTFKD	8-Lead Plastic MSOP	–40°C to 85°C
LTC4359HMS8#WPBF	LTC4359HMS8#WTRPBF	LTFKD	8-Lead Plastic MSOP	–40°C to 125°C
LTC4359IDCB#WTRPBF	LTC4359IDCB#WTRPBF	LFKF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC4359HDCB#WTRPBF	LTC4359HDCB#WTRPBF	LFKF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, IN = 12V, SOURCE = IN, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Supply Range		●	4		80	V
I_{IN}	IN Current	IN = 12V IN = OUT = 12V, $\overline{SHDN}$ = 0V IN = OUT = 24V, $\overline{SHDN}$ = 0V IN = –40V	● ● ● ●	 0	150 9 15 –15	200 20 30 –40	µA µA µA µA
I_{OUT}	OUT Current	IN = 12V, In Regulation IN = 12V, ΔV_{SD} = –1V IN = OUT = 12V, $\overline{SHDN}$ = 0V IN = OUT = 24V, $\overline{SHDN}$ = 0V OUT = 12V, IN = $\overline{SHDN}$ = 0V	● ● ● ● ●	3 	5 120 0.8 0.8 6	7.5 220 3 3 12	µA µA µA µA µA
I_{SOURCE}	SOURCE Current	IN = 12V, ΔV_{SD} = –1V IN = SOURCE = 12V, $\overline{SHDN}$ = 0V SOURCE = –40V	● ● ●	 1 –0.4	150 4 –0.8	200 15 –1.5	µA µA mA
ΔV_{GATE}	Gate Drive (GATE–SOURCE)	IN = 4V, I_{GATE} = 0, –1µA IN = 8V to 80V; I_{GATE} = 0, –1µA	● ●	4.5 10	5.5 12	15 15	V V
ΔV_{SD}	Source-Drain Regulation Voltage (IN –OUT)	ΔV_{GATE} = 2.5V	●	20	30	45	mV
$I_{GATE(UP)}$	Gate Pull-Up Current	GATE = IN, ΔV_{SD} = 0.1V	●	–6	–10	–14	µA
$I_{GATE(DOWN)}$	Gate Pull-Down Current	Fault Condition, ΔV_{GATE} = 5V, ΔV_{SD} = –1V Shutdown Mode, ΔV_{GATE} = 5V, ΔV_{SD} = 0.7V	● ●	70 0.6	130	180	mA mA
t_{OFF}	Gate Turn-Off Delay Time	ΔV_{SD} = 0.1V to –1V, ΔV_{GATE} < 2V, C_{GATE} = 0pF	●		0.3	0.5	µs
t_{ON}	Gate Turn-On Delay Time	IN = 12V, SOURCE = OUT = 0V, $\overline{SHDN}$ = 0V to 2V ΔV_{GATE} > 4.5V, C_{GATE} = 0pF			200		µs
$V_{\overline{SHDN}(TH)}$	$\overline{SHDN}$ Pin Input Threshold	IN = 4V to 80V	●	0.6	1.2	2	V
$V_{\overline{SHDN}(FLT)}$	$\overline{SHDN}$ Pin Float Voltage	IN = 4V to 80V	●	0.6	1.75	2.5	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ = 0.5V, LTC4359I, LTC4359C $\overline{SHDN}$ = 0.5V, LTC4359H $\overline{SHDN}$ = –40V Maximum Allowable Leakage, V_{IN} = 4V	● ● ●	–1 –0.5 –0.4	–3 –3 –0.8 100	–5 –5 –1.5	µA µA mA nA
$V_{SOURCE(TH)}$	Reverse SOURCE Threshold for GATE Off	GATE = 0V, $I_{GATE(DOWN)}$ = 1mA	●	–0.9	–1.8	–2.7	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

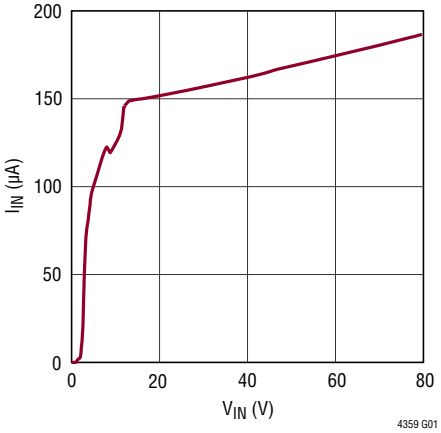
Note 2: All currents into pins are positive; all voltages are referenced to V_{SS} unless otherwise specified.

Note 3: An internal clamp limits the OUT pin to a minimum of 100V above V_{SS}. Driving this pin with more current than 1mA may damage the device.

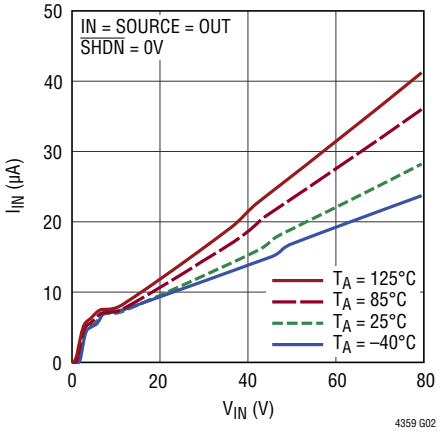
Note 4: An internal clamp limits the GATE pin to a minimum of 10V above IN or 100V above V_{SS}. Driving this pin to voltages beyond the clamp may damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

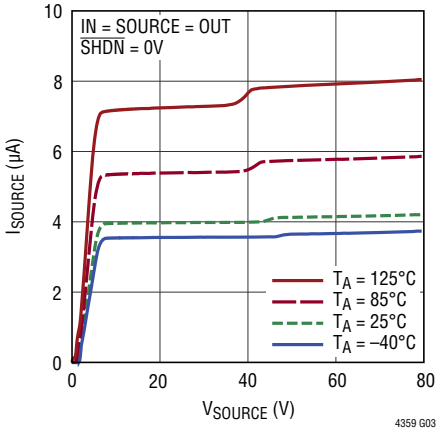
IN Current in Regulation



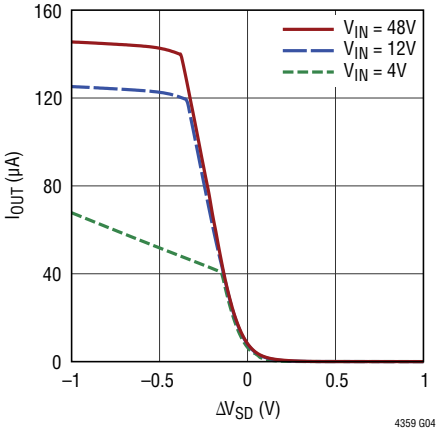
IN Current in Shutdown



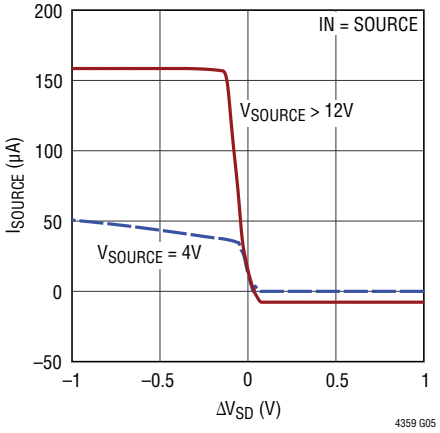
SOURCE Current in Shutdown



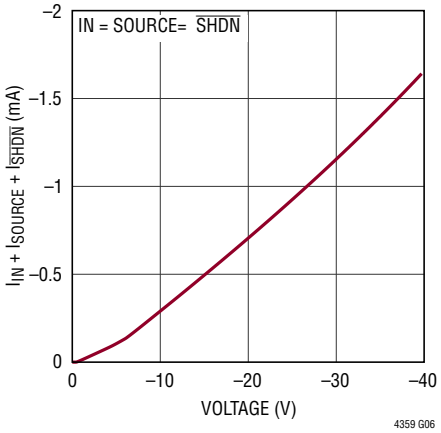
OUT Current vs Forward Voltage Drop



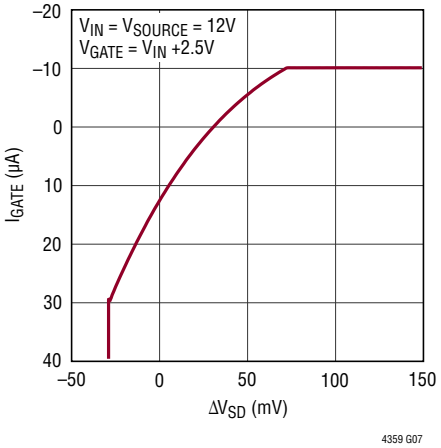
SOURCE Current vs Forward Voltage Drop



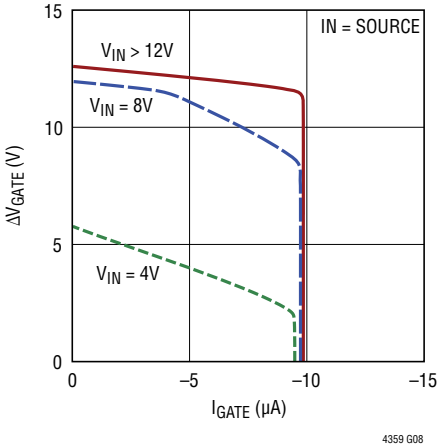
Total Negative Current vs Negative Input Voltage



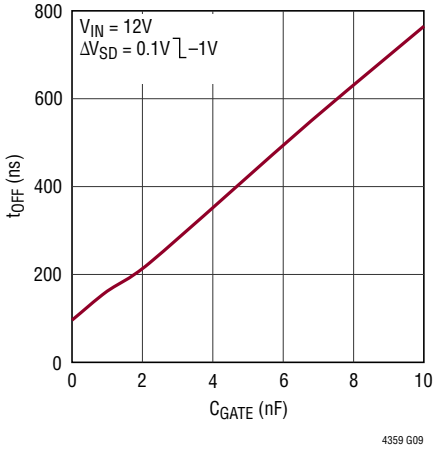
Gate Current vs Forward Voltage Drop



Gate Drive vs Gate Current



Gate Turn-Off Time vs GATE Capacitance



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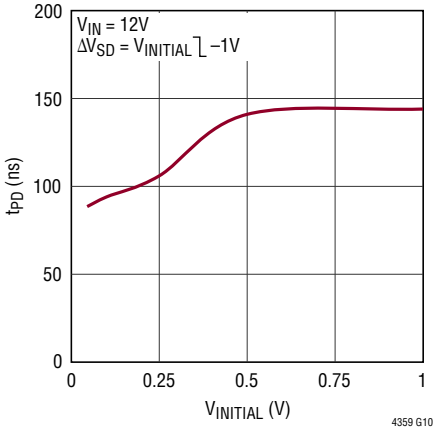
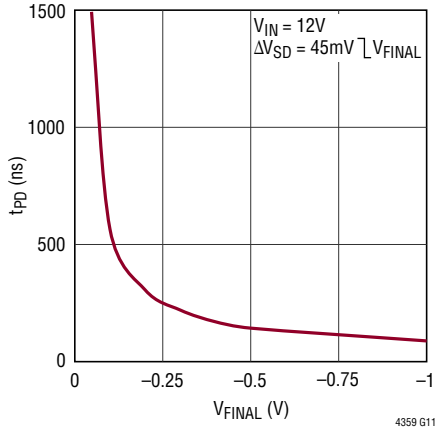
TYPICAL PERFORMANCE CHARACTERISTICS

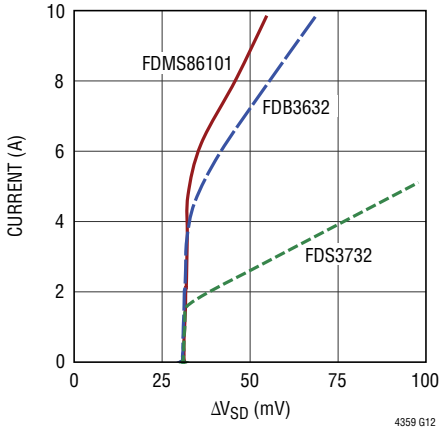
Gate Turn-Off Time vs Initial Overdrive



Gate Turn-Off Time vs Final Overdrive



Load Current vs Forward Voltage Drop



PIN FUNCTIONS

Exposed Pad (DCB Package Only): Exposed pad may be left open or connected to V_{SS}.

GATE: Gate Drive Output. The GATE pin pulls high, enhancing the N-channel MOSFET when the load current creates more than 30mV of voltage drop across the MOSFET. When the load current is small, the gate is actively driven to maintain 30mV across the MOSFET. If reverse current flows, a fast pull-down circuit connects the GATE to the SOURCE pin within 0.3µs, turning off the MOSFET.

IN: Voltage Sense and Supply Voltage. IN is the anode of the ideal diode. The voltage sensed at this pin is used to control the MOSFET gate.

NC (MS8 and S8 Packages): No Connection. Not internally connected.

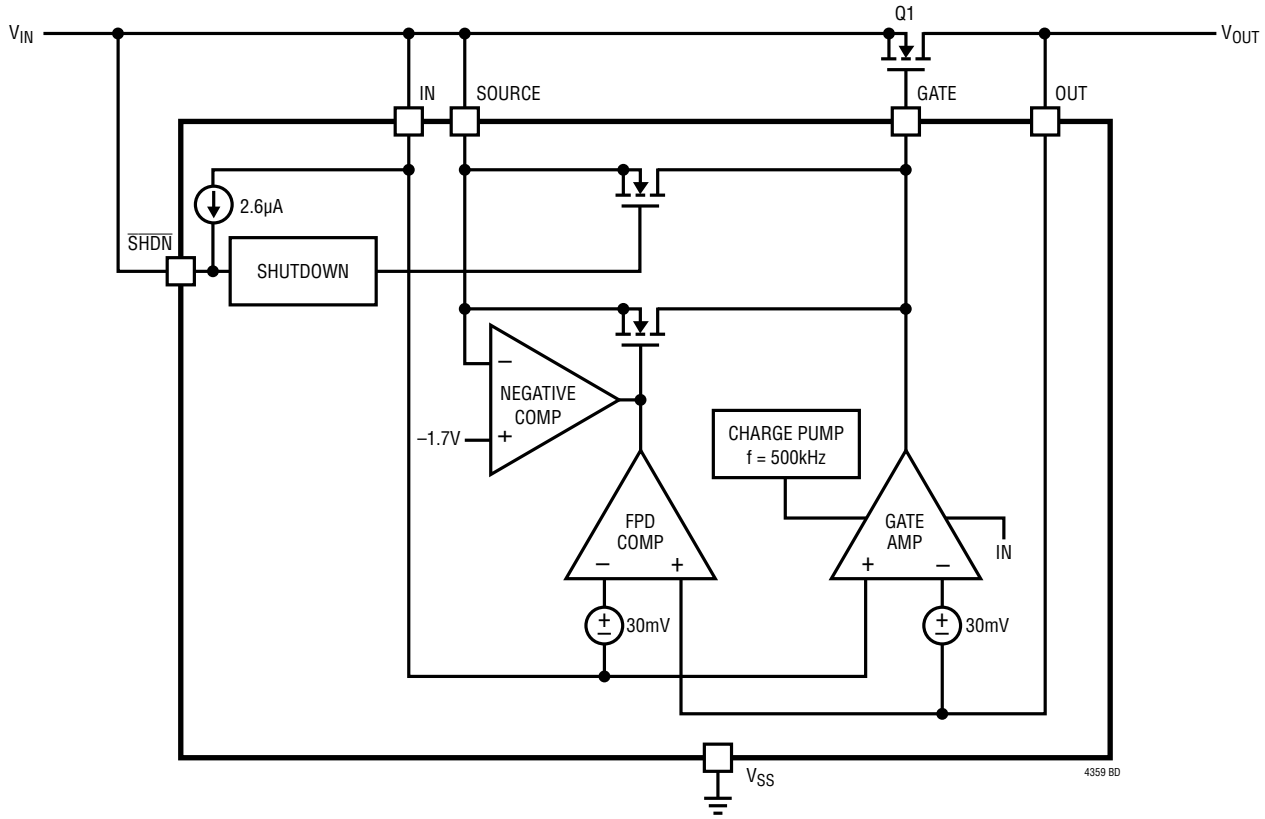
OUT: Drain Voltage Sense. OUT is the cathode of the ideal diode and the common output when multiple LTC4359s are configured as an ideal diode-OR. It connects either directly or through a 2k resistor to the drain of the N-channel MOSFET. The voltage sensed at this pin is used to control the MOSFET gate.

$\overline{\text{SHDN}}$: Shutdown Control Input. The LTC4359 can be shut down to a low current mode by pulling the $\overline{\text{SHDN}}$ pin below 0.6V. Pulling this pin above 2V or disconnecting it allows an internal 2.6µA current source to turn the part on. Maintain board leakage to less than 100nA for proper operation. The $\overline{\text{SHDN}}$ pin can be pulled up to 100V or down to –40V with respect to V_{SS} without damage. If the shutdown feature is not used, connect $\overline{\text{SHDN}}$ to IN.

SOURCE: Source Connection. SOURCE is the return path of the gate fast pull-down. Connect this pin as close as possible to the source of the external N-channel MOSFET.

V_{SS}: Supply Voltage Return and Device Ground.

BLOCK DIAGRAM



OPERATION

The LTC4359 controls an external N-channel MOSFET to form an ideal diode. The GATE amplifier (see Block Diagram) senses across IN and OUT and drives the gate of the MOSFET to regulate the forward voltage to 30mV. As the load current increases, GATE is driven higher until a point is reached where the MOSFET is fully on. Further increases in load current result in a forward drop of $R_{DS(ON)} \bullet I_{LOAD}$.

If the load current is reduced, the GATE amplifier drives the MOSFET gate lower to maintain a 30mV drop. If the input voltage is reduced to a point where a forward drop of 30mV cannot be supported, the GATE amplifier drives the MOSFET off.

In the event of a rapid drop in input voltage, such as an input short-circuit fault or negative-going voltage spike, reverse current temporarily flows through the MOSFET. This current is provided by any load capacitance and by other supplies or batteries that feed the output in diode-OR applications. The FPD COMP (Fast Pull-Down Comparator) quickly responds to this condition by turning the MOSFET off in 300ns, thus minimizing the disturbance to the output bus.

The IN, SOURCE, GATE and $\overline{SHDN}$ pins are protected against reverse inputs of up to –40V. The NEGATIVE COMP detects negative input potentials at the SOURCE pin and quickly pulls GATE to SOURCE, turning off the MOSFET and isolating the load from the negative input.

When pulled low the $\overline{SHDN}$ pin turns off most of the internal circuitry, reducing the quiescent current to 9µA and holding the MOSFET off. The $\overline{SHDN}$ pin may be either driven high or left open to enable the LTC4359. If left open, an internal 2.6µA current source pulls $\overline{SHDN}$ high. In applications where Q1 is replaced with back-to-back MOSFETs, the $\overline{SHDN}$ pin serves as an on/off control for the forward path, as well as enabling the diode function.

APPLICATIONS INFORMATION

Blocking diodes are commonly placed in series with supply inputs for the purpose of ORing redundant power sources and protecting against supply reversal. The LTC4359 replaces diodes in these applications with a MOSFET to reduce both the voltage drop and power loss associated with a passive solution. The curve shown on page 1 illustrates the dramatic improvement in power loss achieved in a practical application. This represents significant savings in board area by greatly reducing power dissipation in the pass device. At low input voltages, the improvement in forward voltage loss is readily appreciated where headroom is tight, as shown in Figure 2.

The LTC4359 operates from 4V to 80V and withstands an absolute maximum range of –40V to 100V without damage. In automotive applications the LTC4359 operates through load dump, cold crank and two-battery jumps, and it survives reverse battery connections while also protecting the load.

A 12V/20A ideal diode application is shown in Figure 1. Several external components are included in addition to the MOSFET, Q1. Ideal diodes, like their nonideal counterparts, exhibit a behavior known as reverse recovery. In combination with parasitic or intentionally introduced inductances, reverse recovery spikes may be generated by an ideal diode during commutation. D1, D2 and R1 protect against these spikes which might otherwise exceed the LTC4359's –40V to 100V survival rating. C_{OUT} also plays a role in absorbing reverse recovery energy. Spikes and protection schemes are discussed in detail in the Input Short-Circuit Faults section.

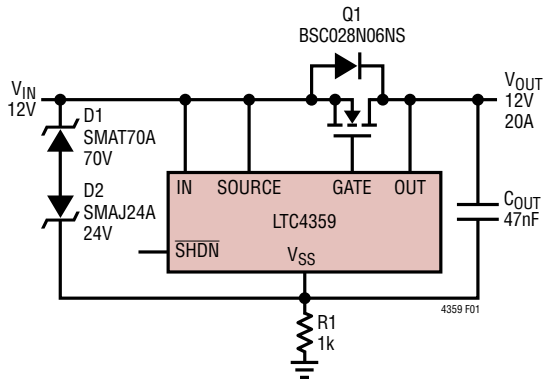


Figure 1. 12V/20A Ideal Diode with Reverse Input Protection

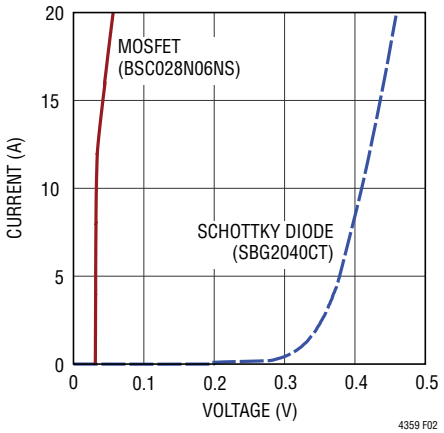


Figure 2. Forward Voltage Drop Comparison Between MOSFET and Schottky Diode

It is important to note that the $\overline{SHDN}$ pin, while disabling the LTC4359 and reducing its current consumption to 9µA, does not disconnect the load from the input since Q1's body diode is ever-present. A second MOSFET is required for load switching applications.

MOSFET Selection

All load current passes through an external MOSFET, Q1. The important characteristics of the MOSFET are on-resistance, $R_{DS(ON)}$, the maximum drain-source voltage, BV_{DSS}, and the gate threshold voltage $V_{GS(TH)}$.

Gate drive is compatible with 4.5V logic-level MOSFETs over the entire operating range of 4V to 80V. In applications above 8V, standard 10V threshold MOSFETs may be used. An internal clamp limits the gate drive to 15V maximum between the GATE and SOURCE pins. For 24V and higher applications, an external Zener clamp (D4) must be added between GATE and SOURCE to not exceed the MOSFET's $V_{GS(MAX)}$ during input shorts.

The maximum allowable drain-source voltage, BV_{DSS}, must be higher than the power supply voltage. If the input is grounded, the full supply voltage will appear across the MOSFET. If the input is reversed, and the output is held up by a charged capacitor, battery or power supply, the sum of the input and output voltages will appear across the MOSFET and $BV_{DSS} > OUT + |V_{IN}|$.

APPLICATIONS INFORMATION

The MOSFET's on-resistance, $R_{DS(ON)}$, directly affects the forward voltage drop and power dissipation. Desired forward voltage drop should be less than that of a diode for reduced power dissipation; 100mV is a good starting point. Choose a MOSFET which has:

$$R_{DS(ON)} < \frac{\text{Forward Voltage Drop}}{I_{LOAD}}$$

The resulting power dissipation is

$$P_d = (I_{LOAD})^2 \bullet R_{DS(ON)}$$

Shutdown Mode

In shutdown, the LTC4359 pulls GATE low to SOURCE, turning off the MOSFET and reducing its current consumption to 9µA. Shutdown does not interrupt forward current flow, a path is still present through Q1's body diode, as shown in Figure 1. A second MOSFET is needed to block the forward path; see the section Load Switching and Inrush Control. When enabled the LTC4359 operates as an ideal diode. If shutdown is not needed, connect $\overline{SHDN}$ to IN. $\overline{SHDN}$ may be driven with a 3.3V or 5V logic signal, or with an open drain or collector. To assert $\overline{SHDN}$ low, the pull down must sink at least 5µA at 500mV. To enable the part, $\overline{SHDN}$ must be pulled up to at least 2V. If $\overline{SHDN}$ is driven with an open drain, open collector or switch contact, an internal pull-up current of 2.6µA (1µA minimum) asserts $\overline{SHDN}$ high and enables the LTC4359. If leakage from $\overline{SHDN}$ to ground cannot be maintained at less than 100nA, add a pull-up resistor to >2V to assure turn on. The self-driven open circuit voltage is limited internally to 2.5V. When floating, the impedance is high and $\overline{SHDN}$ is subject to capacitive coupling from nearby clock lines or traces exhibiting high dV/dt. Bypass $\overline{SHDN}$ to V_{SS} with 10nF to eliminate injection. Figure 3a is the simplest way to control the shutdown pin. Since the control signal ground is different from the $\overline{SHDN}$ pin reference, V_{SS}, there could be momentary glitches on $\overline{SHDN}$ during transients. Figures 3b and 3c are alternative solutions that level-shift the control signal and eliminate glitches.

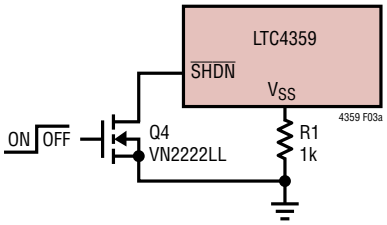


Figure 3a. $\overline{SHDN}$ Control

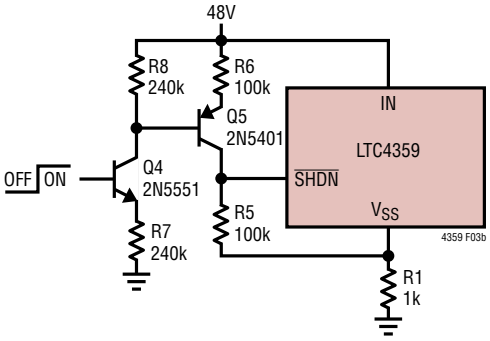


Figure 3b. Transistor $\overline{SHDN}$ Control

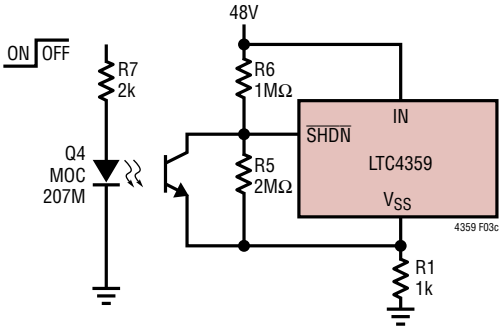


Figure 4c. Opto-Isolator $\overline{SHDN}$ Control

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery

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phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/µs or higher.

High slew rates coupled with parasitic inductances in series with the input and output paths may cause potentially destructive transients to appear at the IN, SOURCE and OUT pins of the LTC4359 during reverse recovery. A zero impedance short-circuit directly across the input and ground is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the MOSFET finally interrupts the reverse current, the LTC4359 IN and SOURCE pins experience a negative voltage spike, while the OUT pin spikes in the positive direction.

To prevent damage to the LTC4359 under conditions of input short-circuit, protect the IN, SOURCE and OUT pins as shown in Figure 4. The IN and SOURCE pins are protected by clamping to the V_{SS} pin with two TransZorbs or TVS. For input voltages 24V and greater, D4 is needed to protect the MOSFET's gate oxide during input short-circuit conditions. Negative spikes, seen after the MOSFET turns off during an input short, are clamped by D2, a 24V TVS. D2 allows reverse inputs to 24V while keeping the MOSFET off and is not required if reverse-input protection is not needed. D1, a 70V TVS, protects IN and SOURCE in the positive direction during load steps and overvoltage conditions. OUT can be protected by an output capacitor, C_{OUT} of at least 1.5µF, a TVS across the MOSFET or by the MOSFET's avalanche breakdown. Care must be taken if the MOSFET's avalanche breakdown is used to protect the OUT pin. The MOSFET's BV_{DSS} must be sufficiently lower than 100V, and the MOSFET's avalanche energy rating must be ample enough to absorb the inductive energy. If a TVS across the MOSFET or the MOSFET avalanche is used to protect the OUT pin, C_{OUT} can be reduced to 47nF. C_{OUT} and R1 preserve the fast turn off time when output parasitic inductance causes the IN and OUT voltages to drop quickly.

Reverse Input Protection

In the case of a reverse input where negative voltage is present on the input, the components D1, D2 and R1 protect the LTC4359. With reverse inputs more negative than D2's breakdown voltage (24V), current flows from system ground through R1. For applications that must withstand reverse inputs much greater than –24V such that R1's power dissipation is unacceptable, it may be replaced by a diode. If reverse input protection and fast turn off time are not required, R1 can be removed and V_{SS} connected to system ground.

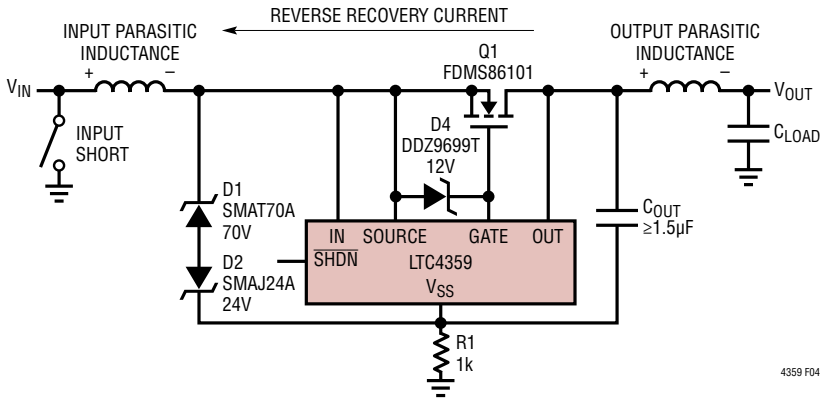


Figure 4. Reverse Recovery Produces Inductive Spikes at the IN, SOURCE and OUT Pins. The Polarity of Step Recovery Is Shown Across Parasitic Inductances

APPLICATIONS INFORMATION

Figure 10 shows a +48V application with reverse input protection where D5 is used instead of R1 to eliminate the power dissipation and system ground current when the input reverses to –48V. With –48V input and OUT powered by another supply or held up by output capacitance, D2 (5.1V) and D3 (75V) prevent the LTC4359's OUT–IN pins from exceeding the 100V absolute maximum rating. R2 limits the current into D1, D2 and D3 during a reverse input.

Paralleling Supplies

Multiple LTC4359s can be used to combine the outputs of two or more supplies for redundancy or for droop sharing, as shown in Figure 5. For redundant supplies, the supply with the highest output voltage sources most or all of the load current. If this supply's output is quickly shorted to ground while delivering load current, the flow of current temporarily reverses and flows backwards through the LTC4359's MOSFET. The LTC4359 senses this reverse current and activates a fast pull-down to quickly turn off the MOSFET.

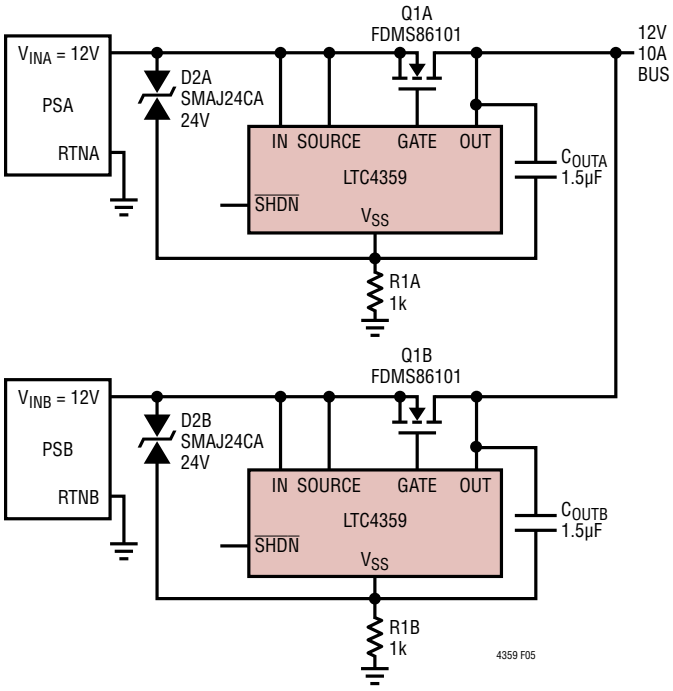


Figure 5. Redundant Power Supplies

If the other, initially lower, supply was not delivering any load current at the time of the fault, the output falls until the body diode of its ORing MOSFET conducts. Meanwhile, the LTC4359 charges the MOSFET gate with 10µA until the forward drop is reduced to 30mV. If this supply was sharing load current at the time of the fault, its associated ORing MOSFET was already driven partially on. In this case, the LTC4359 will simply drive the MOSFET gate harder in an effort to maintain a drop of 30mV.

Droop sharing can be accomplished if both power supply output voltages and output impedances are nearly equal. The 30mV regulation technique ensures smooth load sharing between outputs without oscillation. The degree of sharing is a function of MOSFET $R_{DS(ON)}$, the output impedance of the supplies and their initial output voltages.

Load Switching and Inrush Control

By adding a second MOSFET as shown in Figure 6, the LTC4359 can be used to control power flow in the forward direction while retaining ideal diode behavior in the reverse direction. The body diodes of Q1 and Q2 prohibit

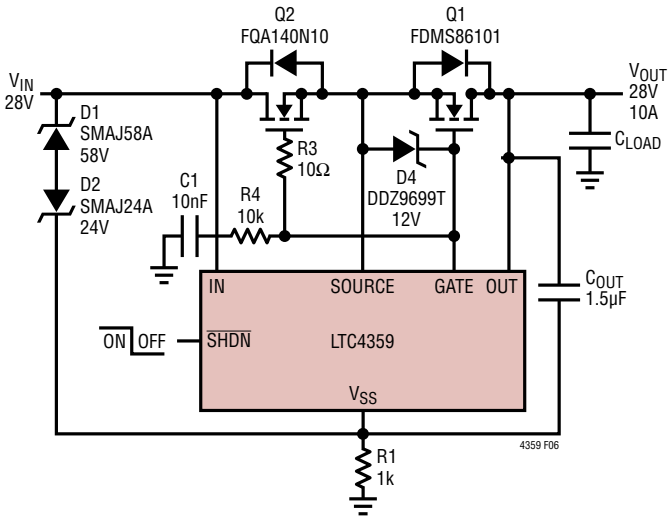


Figure 6. 28V Load Switch and Ideal Diode with Reverse Input Protection

APPLICATIONS INFORMATION

current flow when the MOSFETs are off. Q1 serves as the ideal diode, while Q2 acts as a switch to control forward power flow. On/off control is provided by the $\overline{SHDN}$ pin, and C1 and R4 may be added if inrush control is desired.

When $\overline{SHDN}$ is driven high and provided $V_{IN} > V_{OUT} + 30mV$, GATE sources 10µA and gradually charges C1, pulling up both MOSFET gates. Q2 operates as a source follower and

$$I_{INRUSH} = \frac{10\mu A \bullet C_{LOAD}}{C1}$$

If $V_{IN} < V_{OUT} + 30mV$, the LTC4359 will be activated but holds Q1 and Q2 off until the input exceeds the output by 30mV. In this way normal diode behavior of the circuit is preserved, but with soft starting when the diode turns on.

When $\overline{SHDN}$ is pulled low, GATE pulls the MOSFET gates down quickly to SOURCE turning off both forward and reverse paths, and the input current is reduced to 9µA.

While C1 and R4 may be omitted if soft starting is not needed, R3 is necessary to prevent MOSFET parasitic oscillations and must be placed close to Q2.

Layout Considerations

Connect the IN, SOURCE and OUT pins as close as possible to the MOSFET source and drain pins. Keep the traces to the MOSFET wide and short to minimize resistive losses as shown in Figure 7. Place surge suppressors and necessary transient protection components close to the LTC4359 using short lead lengths.

For the DFN package, pin spacing may be a concern at voltages greater than 30V. Check creepage and clearance guidelines to determine if this is an issue. To increase the effective pin spacing between high voltage and ground pins, leave the exposed pad connection open. Use no-clean flux to minimize PCB contamination.

Figures 8 through 18 show typical applications of the LTC4359.

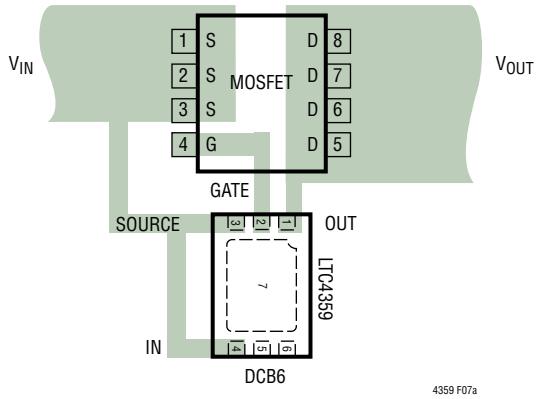


Figure 7a. Layout, DCB6 Package

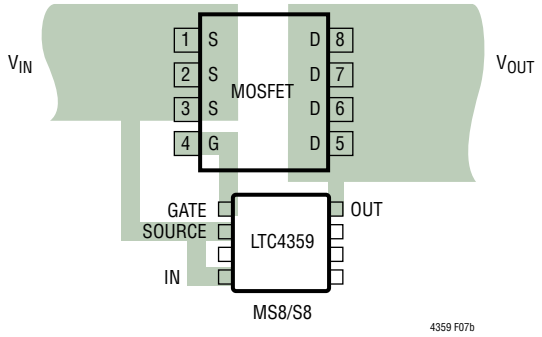


Figure 7b. Layout, MS8/S8 Package

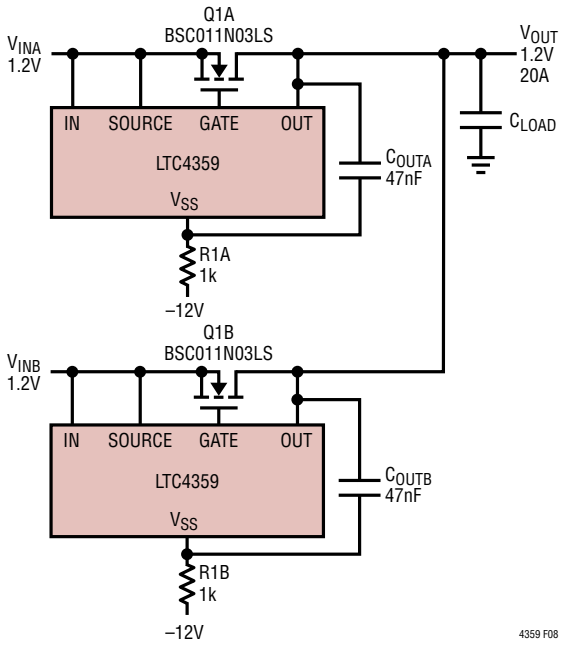


Figure 8. 1.2V Diode–OR

TYPICAL APPLICATIONS

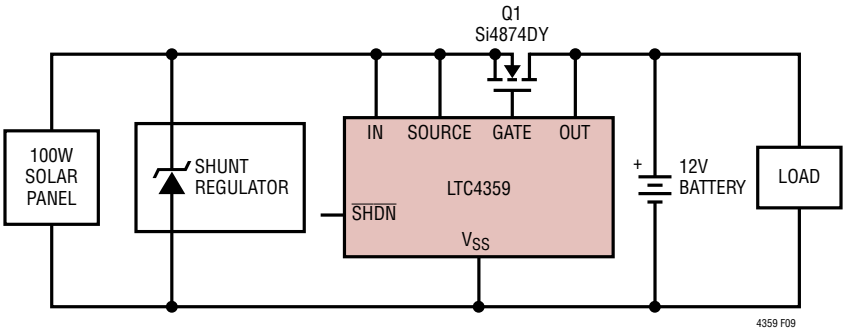


Figure 9. Lossless Solar Panel Isolation

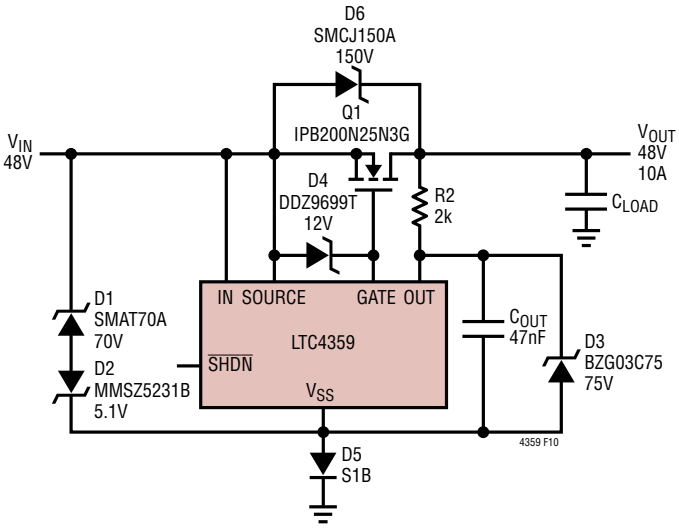


Figure 10. 48V Ideal Diode with Reverse Input Protection to –72V

TYPICAL APPLICATIONS

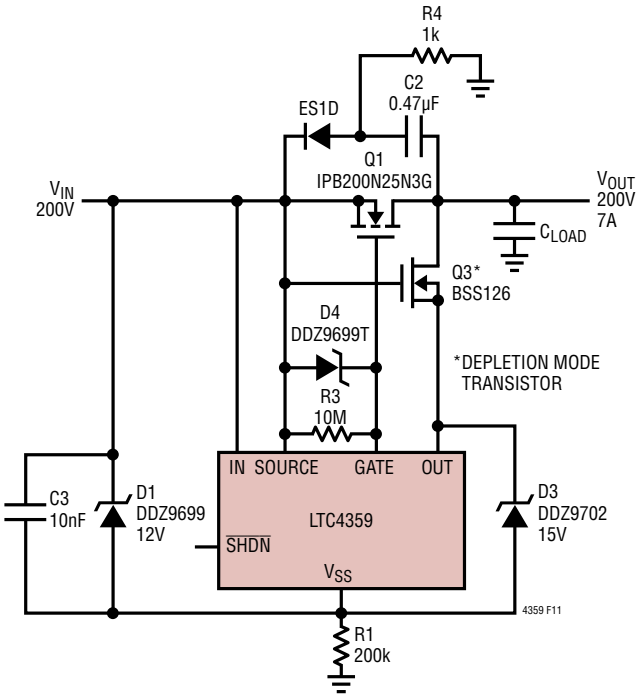


Figure 11. 200V Ideal Diode

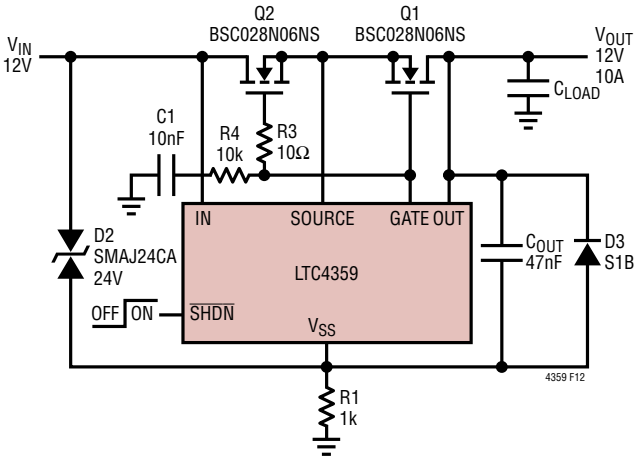


Figure 12. 12V Load Switch and Ideal Diode with Reverse Input Protection

TYPICAL APPLICATIONS

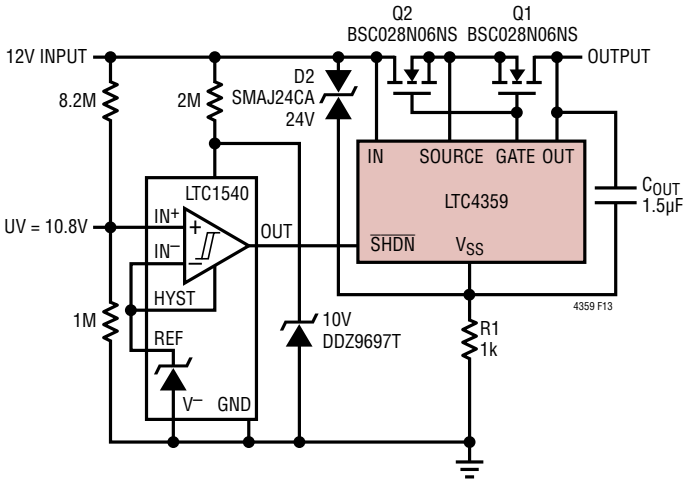


Figure 13. 12V Load Switch and Ideal Diode with Precise Undervoltage Lockout

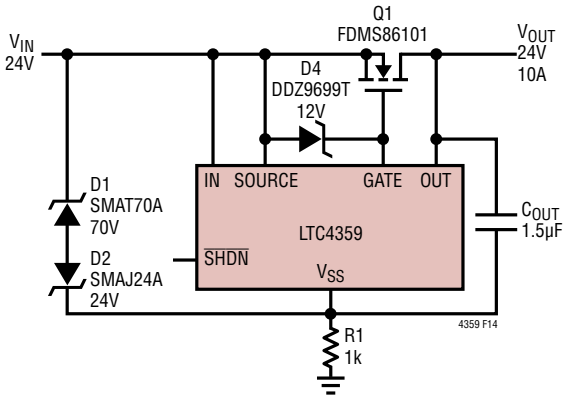


Figure 14. 24V Ideal Diode with Reverse Input Protection

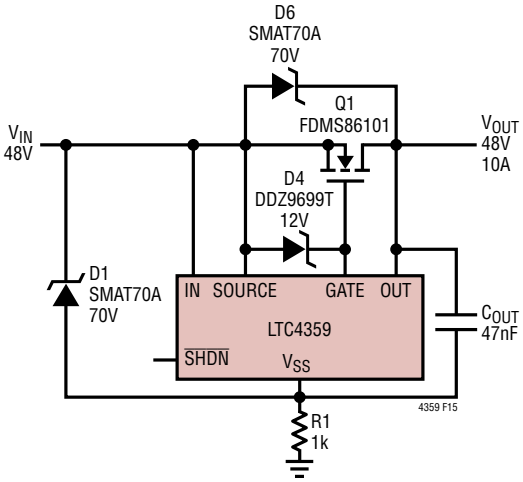


Figure 15. 48V Ideal Diode without Reverse Input Protection

TYPICAL APPLICATIONS

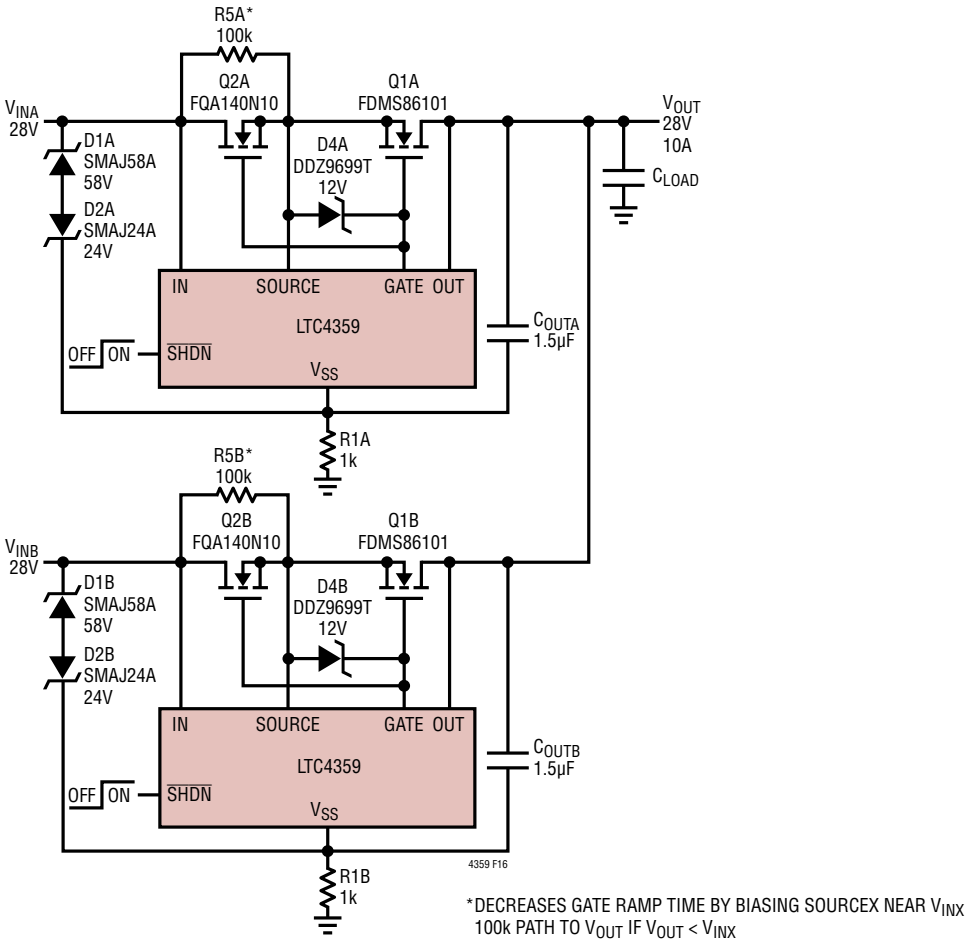


Figure 16. Diode-OR with Selectable Power Supply Feeds and Reverse Input Protection

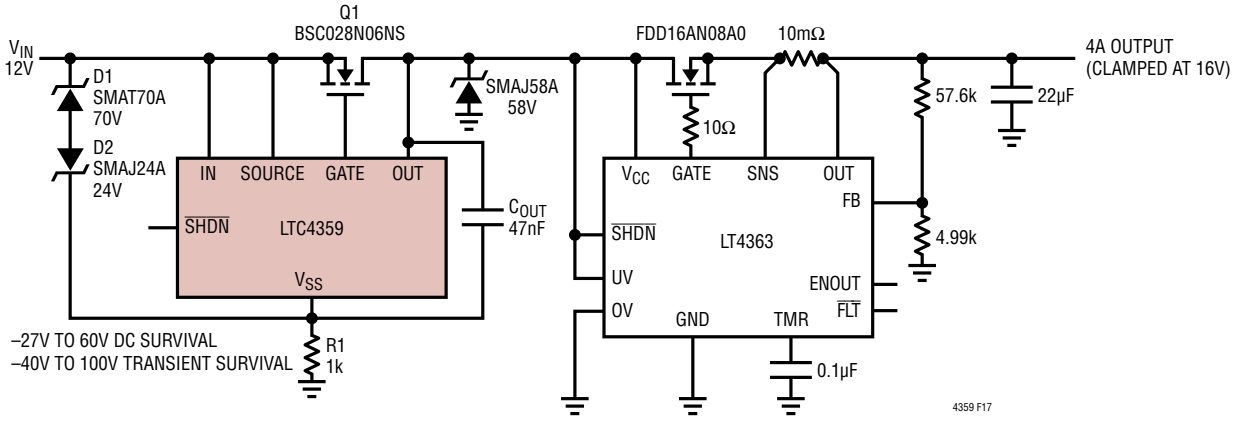
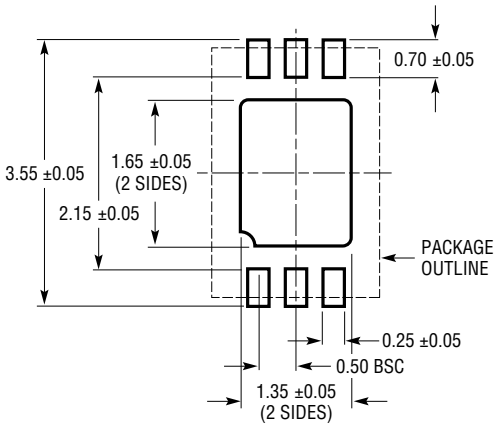


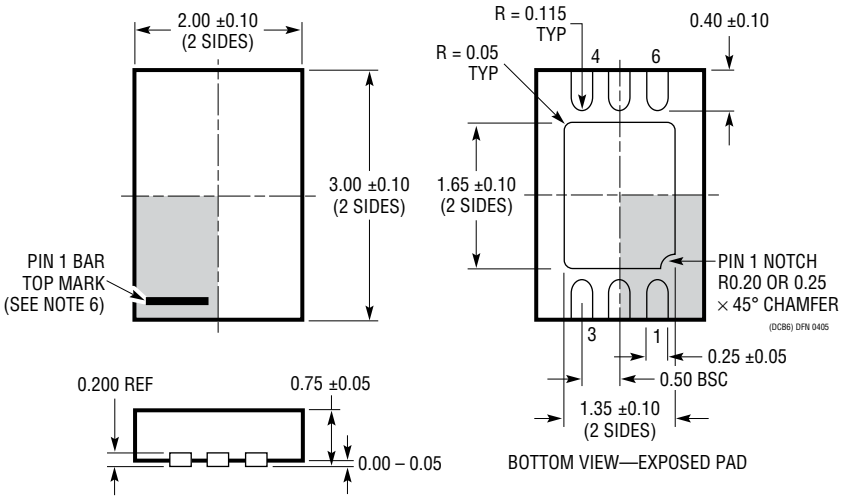
Figure 17. Overvoltage Protector and Ideal Diode Blocks Reverse Input Voltage

PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



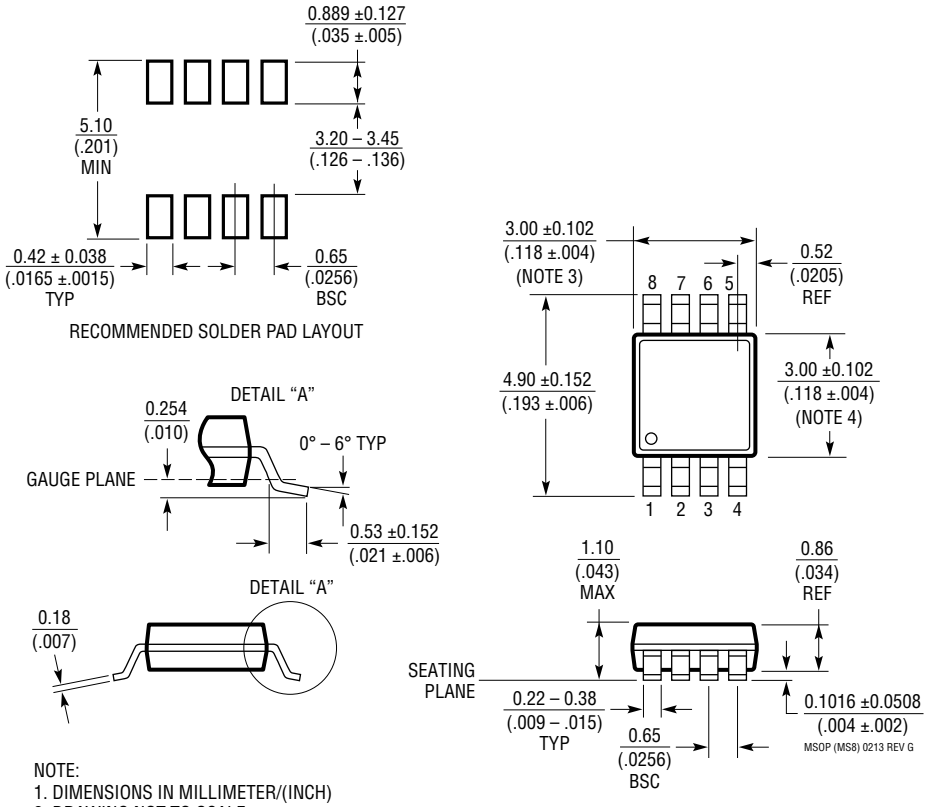
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

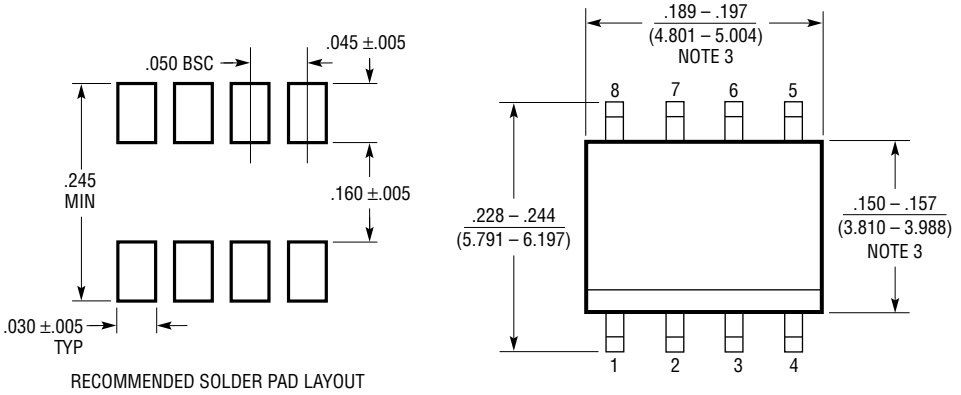
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

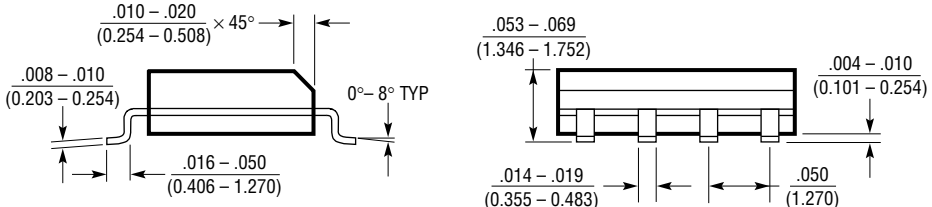


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)





NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

SO8 REV G 0212

Rev. F

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/13	Corrected $\overline{SHDN}$ pull-up current from 2μA to 2.6μA. Updated Figure 11.	5, 6, 7, 8 12
B	05/14	Pin Configuration, updated T_{JMAX} to 150°C from 125°C. Added specification, Gate Turn-On Delay Time (t_{ON}).Figure 16, added R5A and R5B resistors.	2 3 14
C	09/17	Updated specification limit for OUT current at IN = 12V, ΔV_{SD} = –1V. Added section titled Reverse Input Protection.	3 9, 10
D	03/18	Added 8-lead SO package.	1, 2, 18
E	06/19	Added AEC-Q100 qualification and “W” part numbers.	1, 2
F	12/21	Added DFN packaged AEC-Q100 qualification and “W” part numbers.	2

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TYPICAL APPLICATION

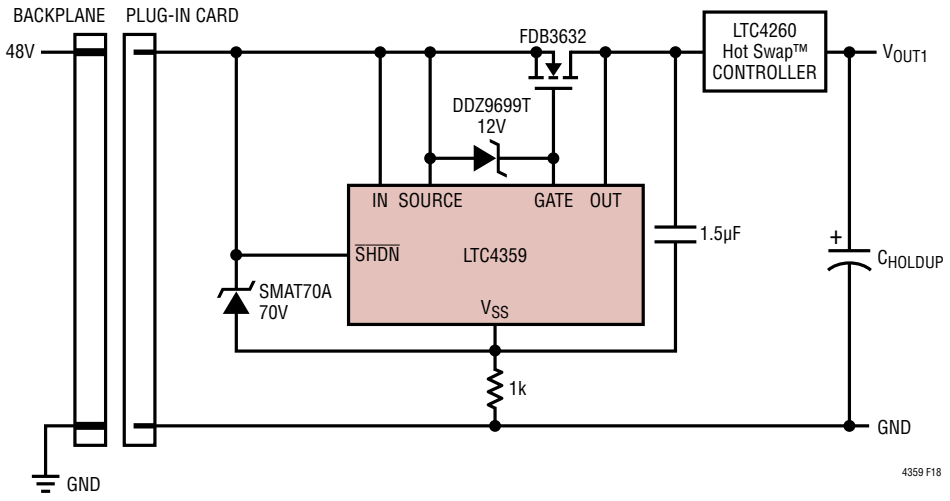

Figure 18. Input Diode for Supply Hold-Up on Plug-In Card

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4352	Ideal Diode Controller with Monitor	Controls N-Channel MOSFET, 0V to 18V Operation
LTC4371	Negative Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, –4.5V to >–100V Operation
LTC4355	Positive Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 0.4µs Turn-Off, 80V Operation
LTC4357	Positive High Voltage Ideal Diode Controller	Controls Single N-Channel MOSFET, 0.5µs Turn-Off, 80V Operation
LTC4358	5A Ideal Diode	Internal N Channel MOSFET, 9V to 26.5V Operation
LT4363-1/LT4363-2	High Voltage Surge Stopper	Stops High Voltage Surges, 4V to 80V, –60V Reverse Input Protection
LTC4380	Low Quiescent Current Surge Stopper	8µA I_Q, 4V to 72V Operation, –60V Reverse Input Protection
LT4256-1/LT4256-2	Positive High Voltage Hot Swap Controllers	Active Current Limiting, Supplies from 10.8V to 80V Latch-Off and Automatic Retry Option
LTC4260	Positive High Voltage Hot Swap Controller	With I^2C and ADC, Supplies from 8.5V to 80V
LTC4364	Surge Stopper with Ideal Diode	4V to 80V Operation, –40V Reverse Input, –20V Reverse Output

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