

ASSP

Spread Spectrum Clock Generator

MB88R157

■ DESCRIPTION

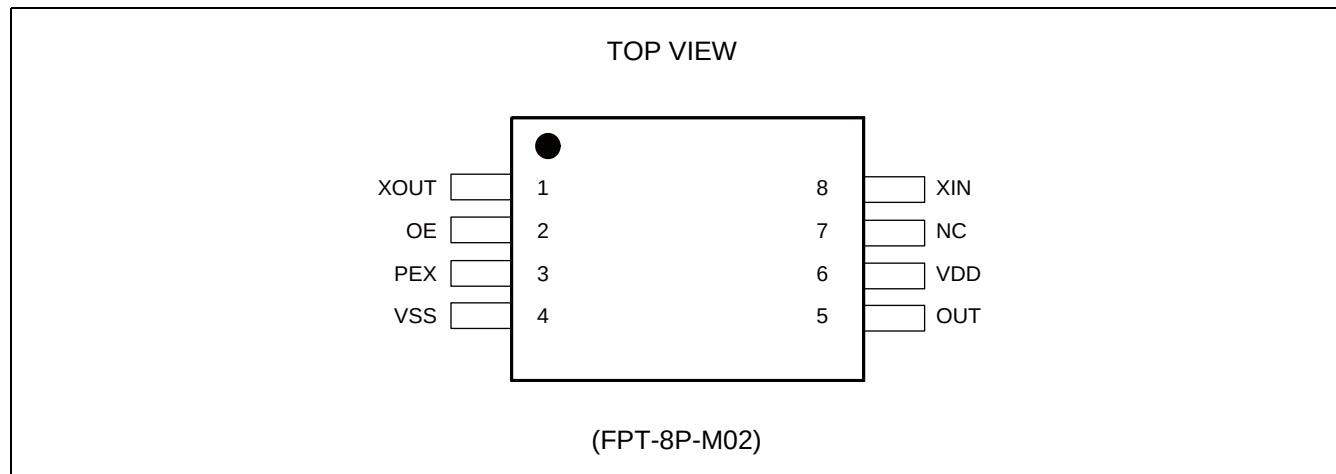
MB88R157 is a clock generator for EMI (Electro Magnetic Interference) reduction. The peak of unnecessary radiation noise (EMI) can be attenuated by making the oscillation frequency slightly modulate periodically with the internal modulator.

This product has a built-in non-volatile memory, so its frequency setting can memorize each system or application. Also the product has a built-in oscillation stabilization circuit, so it is not necessary to use the external oscillation stabilization capacitance.

■ FEATURES

- Input frequency : 10 MHz to 40 MHz
- Output frequency : 1 MHz to 134 MHz
 Programmable of the parameter of N divider, M divider, K divider
 (N divider : 11-bit, M divider : 12-bit, K divider : 7-bit)
- Modulation rate : no modulation, $\pm 0.25\%$, $\pm 0.5\%$, $\pm 0.75\%$, $\pm 1.0\%$, $\pm 1.25\%$, $\pm 1.5\%$, $\pm 1.75\%$
- Equipped with a crystal oscillation circuit
- Built-in oscillation stabilization capacitance : 5 pF to 10 pF (0.039 pF step range)
- Clock output Duty : 45% to 55%
- Clock Cycle-Cycle Jitter : Less than 100 ps (Output frequency is over 2 MHz)
- Low power consumption by CMOS process 5.5 mA (24 MHz, Typ-sample, no load)
 (Input frequency : 24 MHz, N divider parameter : 1000, M divider parameter : 1000, K divider parameter : 1)
- Power supply voltage : 3.3 V $\pm$ 0.3 V
- Operating temperature -20°C to $+85^{\circ}\text{C}$
- Package : 8-pin plastic SOP

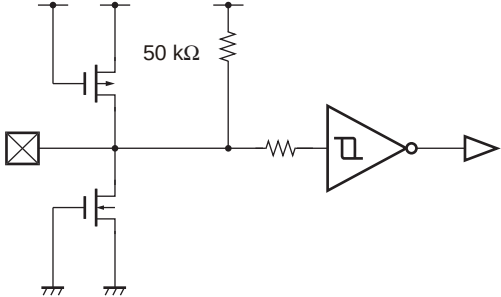
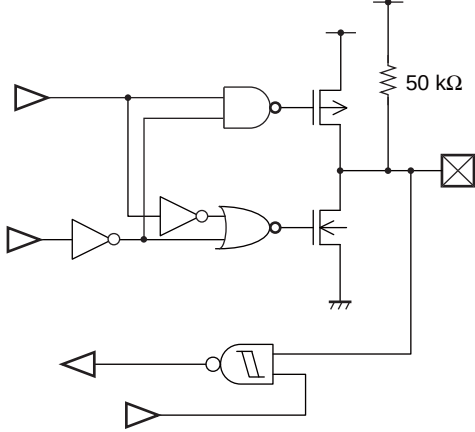
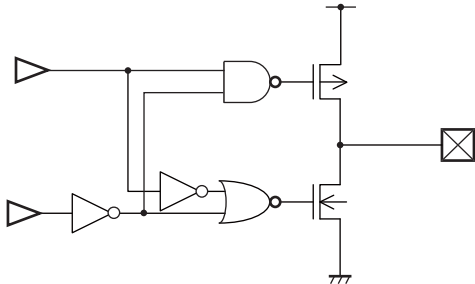
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin name	Pin no.	I/O	Description
XOUT	1	O	Resonator connection pin
OE	2	I/O	Clock output enable pin L : output disable, H : output enable Serial input/output pin (only program mode)
PEX	3	I	Programmable enable setting pin L : program mode, H : normal operation
VSS	4	—	GND pin
OUT	5	O	Modulation clock output pin
VDD	6	—	Power supply voltage pin
NC	7	—	Non-connection pin (do not connect anything)
XIN	8	I	Resonator connection pin/clock input pin

■ I/O CIRCUIT TYPE

Pin name	Circuit type	Remarks
PEX		• CMOS hysteresis input • With pull-up resistor (50 kΩ)
OE		With pull-up resistor (50 kΩ) • CMOS hysteresis input (Input) In serial output mode • CMOS output • $I_{OL} = 3 \text{ mA}$
OUT		• CMOS output • $I_{OL} = 3 \text{ mA}/7 \text{ mA}$ selectable (Selectable by Output driver setting bit) • Hi-Z or "L" output at OE = "L" (Selectable by OUT pin setting bit)

Note : About XIN and XOUT pins, please refer to the chapter of "■ CRYSTAL OSCILLATION CIRCUIT".

■ HANDLING DEVICES

• Preventing Latch-up

A latch-up can occur if, on this device, (a) a voltage higher than power supply voltage or a voltage lower than GND is applied to an input or output pin or (b) a voltage higher than the rating is applied between power supply and GND. The latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use this device, be very careful not to exceed the maximum rating.

• Handling unused pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, using a pull-up or pull-down resistor.

• To use external clock input

To use an external clock signal, input the clock signal to the XIN pin with the XOUT pin connected to nothing.

• Power supply pins

Please design connecting the power supply pin of this device by as low impedance as possible from the current supply source.

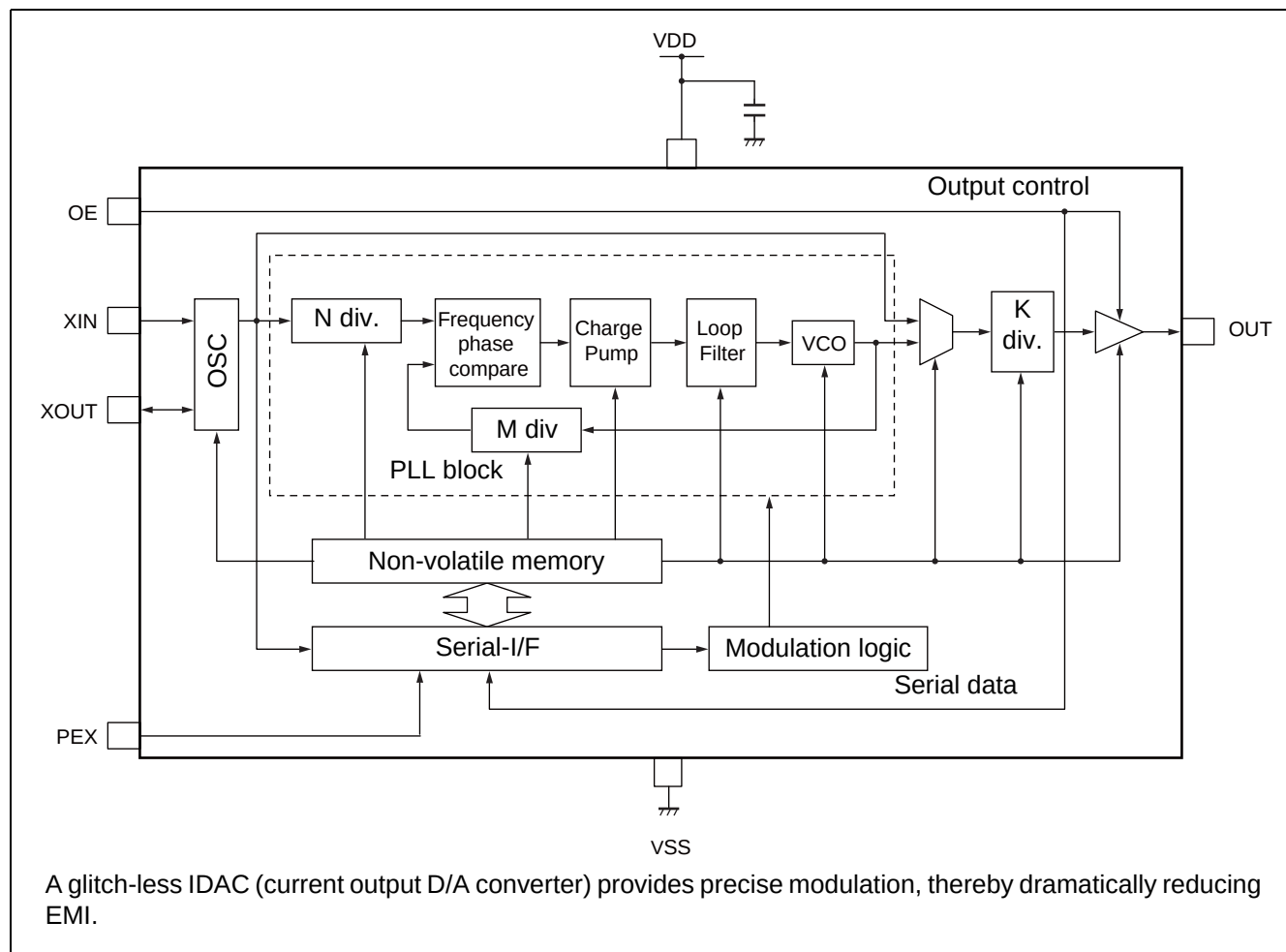
We recommend connecting electrolytic capacitor (about 10 μ F) and the ceramic capacitor (about 0.01 μ F) in parallel between power supply and GND near the device, as a bypass capacitor.

• Oscillation circuit

Noise near the XIN pin and XOUT pin may cause the device to malfunction. Design printed circuit boards so that electric wiring of XIN pin or XOUT pin and the resonator do not intersect other wiring.

Design the printed circuit board that surrounds the XIN pin and XOUT pin with ground in order to stabilize operation.

■ BLOCK DIAGRAM



■ MEMORY MAP

Address	Function	Remarks
bit0-bit11	M divider setting (12-bit)	Selectable in the range of 1 to 4096
bit12-bit22	N divider setting (11-bit)	Selectable in the range of 1 to 2048
bit23-bit29	K divider setting (7-bit)	Selectable in the range of 1 to 128
bit30-bit32	L divider setting (3-bit)	Modulation frequency setting (the value is due to the input frequency)
bit33-bit36	Charge Pump setting (4-bit)	Charge pump current setting due to VCO oscillation frequency
bit37-bit41	VCO Gain setting (5-bit)	VCO gain setting due to VCO oscillation frequency
bit42-bit44	Modulation rate setting (3-bit)	No modulation, $\pm 0.25\%$, $\pm 0.50\%$, $\pm 0.75\%$, $\pm 1.00\%$, $\pm 1.25\%$, $\pm 1.50\%$, $\pm 1.75\%$ are selectable
bit45	OUT pin setting (1bit)	Selectable OUT pin situation at OE pin = L 0 : L output 1 : Hi-Z output
bit46	Output drive setting (1bit)	OUT pin driving ability setting 0 : Ability small 1 : Ability large
bit47	Source clock dividing mode (1bit)	Source clock selectable to K divider 0 : VCO output 1 : Source clock
bit48	PLL mode setting (1bit)	0 : Normal mode 1 : PLL mode
bit49-bit55	XIN oscillation stabilization capacitance setting (7-bit)	Capacitance is selectable from 5 pF to 10 pF by 0.039 pF Step
bit56-bit62	XOUT oscillation stabilization capacitance setting (7-bit)	Capacitance is selectable from 5 pF to 10 pF by 0.039 pF Step
bit63	Reserve	—

■ OPERATION SETTING

• Frequency setting

Output frequency can be set by writing the internal memory to each divider parameter in the PLL block.
Internal oscillation frequency and output frequency can be calculated following expressions :

$$\text{Internal oscillation frequency (fvco*)} = \text{Input frequency (fin)} \times (M+1) / (N+1)$$

* : Please set the fvco range from 20 MHz to 134 MHz.

$$\text{Output frequency (fout*)} = \text{Input frequency (fin)} \times (M+1) / ((N+1) \times K)$$

* : Please set the fout range from 1 MHz to 134 MHz.

(Setting example)

$$\text{fin} = 27 \text{ MHz}, \text{fout} = 60 \text{ MHz}$$

M divider parameter : 1999 (= 7CF_H) , N divider parameter : 899 (= 383_H) , K divider parameter : 1 (= 01_H)

$$27 \times (1999+1) / ((899+1) \times 1) = 60 [\text{MHz}] \quad (\text{fvco} = 27 \times (1999+1) / (899+1) = 60 [\text{MHz}])$$

Note: Recommended value of each divider parameter is different at PLL mode and normal mode. Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

• Modulation frequency setting

Modulation frequency can be set by writing the internal memory to L divider parameter.
The average of modulation frequency can be calculated following expressions :

$$\frac{\text{Input frequency}}{266 \times (L+1)} \quad (L = 1, 2, 3, 4, 5, 6, 7)$$

Note: Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

• Modulation rate setting

Modulation rate can be selectable from no modulation, ±0.25%, ±0.50%, ±0.75%, ±1.00%, ±1.25%, ±1.50%, ±1.75%.

bit44	bit43	bit42	Modulation rate setting
0	0	0	No modulation
0	0	1	±0.25%
0	1	0	±0.50%
0	1	1	±0.75%
1	0	0	±1.00%
1	0	1	±1.25%
1	1	0	±1.50%
1	1	1	±1.75%

- **Charge Pump setting, VCO gain setting**

Note: Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

- **OUT pin setting**

OUT pin situation can be selected at OE pin “L” input.

bit45	OUT pin situation
0	“L” output
1	“Hi-Z” output

Note : Internal oscillation circuit has been operating when OE pin is input “L”.

- **Output drive ability setting**

Output drive ability of OUT pin can be selected.

bit46	OUT pin drive ability
0	Small ($I_{OL} = 3 \text{ mA}$)
1	Large ($I_{OL} = 7 \text{ mA}$)

- **Source clock dividing setting**

Source clock to K divider can be selected.

When “input frequency” is selected, source clock or its divided clock can be output. But modulation setting is not enable.

bit47	Source clock to K divider
0	VCO output clock
1	Input clock (Source clock)

Note: When “input frequency ” is selected, internal oscillation circuit has been operating. About M and N divider parameter setting, please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

- **PLL mode setting**

It can be selected normal mode and PLL mode by bit48 setting in the memory map. PLL mode is good jitter specification at non modulation. When the mode is selected, it becomes non modulation setting, the resistance and capacitance value of the loop filter is changed, so oscillation specification is change.

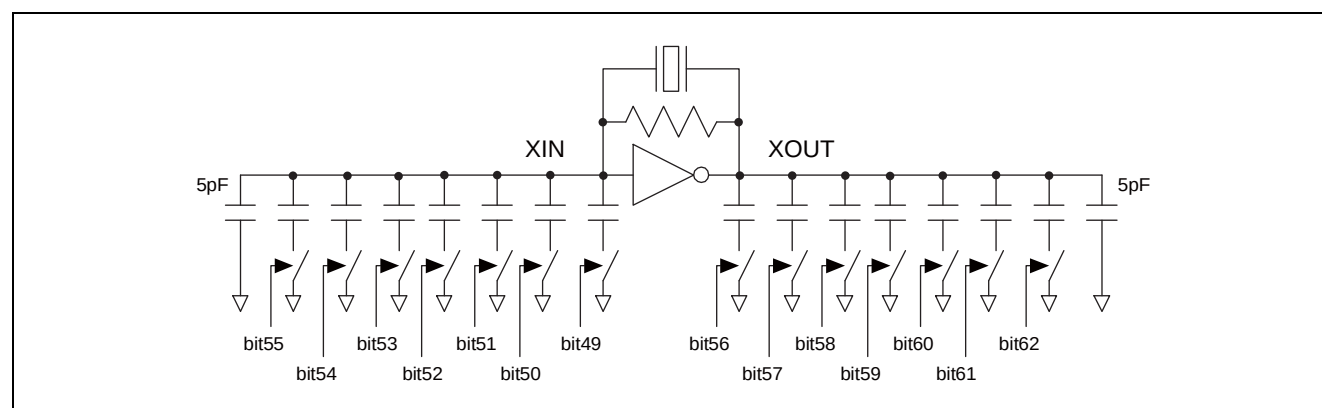
bit48	Operation mode
0	SSCG mode
1	PLL mode

Note: When PLL mode is selected, recommended value of M, N, K divider is changed. Please refer and confirm the recommended value by our support tool. Contact the sales representatives for details on the support tools.

• Oscillation stabilization capacitance setting

The capacitance connected XIN and XOUT pin can change each from 5 pF to 10 pF by writing to bit49 to bit55 and bit56 to bit62 in the memory map.

XIN	XOUT	Capacitance [pF]
bit49	bit56	0.039
bit50	bit57	0.079
bit51	bit58	0.157
bit52	bit59	0.315
bit53	bit60	0.630
bit54	bit61	1.260
bit55	bit62	2.520



(Setting example)

bit49 to bit55 : "0000000" bit56 to bit62 : "0100001"

XIN pin Oscillation stabilization capacitance : 5.000 pF

XOUT pin Oscillation stabilization capacitance : 7.599 pF

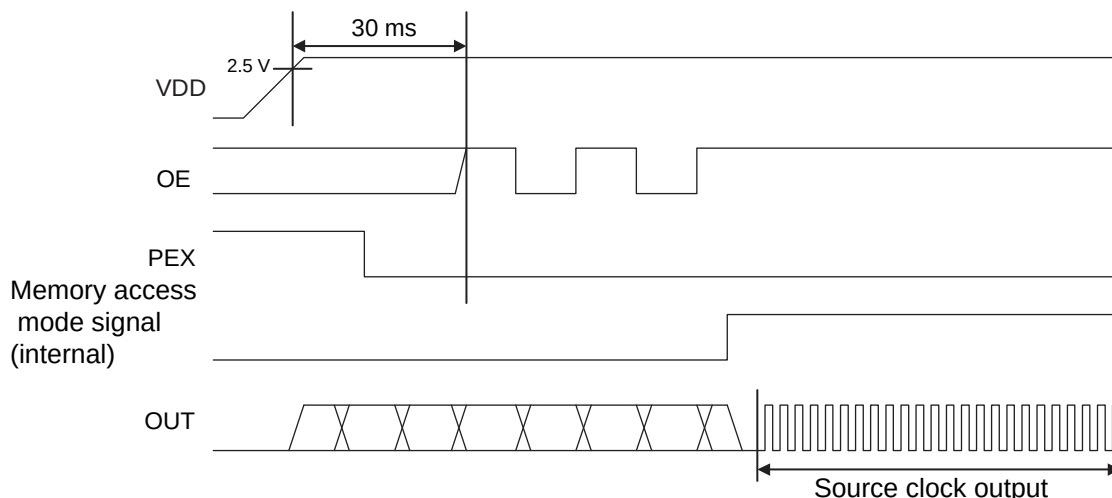
■ MEMORY ACCESS

Read/write to the built-in non-volatile memory is enabled through the serial communication with the OE pin functioned as the I/O pin.

Set for the communication protocol. Also, set the transfer speed as 1/512 of the source clock.

- Asynchronous transfer mode of UART
- LSB fast
- NRZ format
- Bit length: 8 bits
- No parity
- Stop bit: 1 bit

• Transfer sequence



1. Set the PEX pin to "L" more than 30 ms after this device is turned on, input a command from the OE pin set MB88R157 into memory access mode. (When a command is input by serial communication, data of "FD_H" is sent.)

Note: When memory access is available, source clock can be output from the OUT pin.
Fix the PEX pin to "H", or fix the OE pin to "H" or "L" until command input.

2. At writing, "00_H" is sent serially, and at reading, "40_H" is sent.

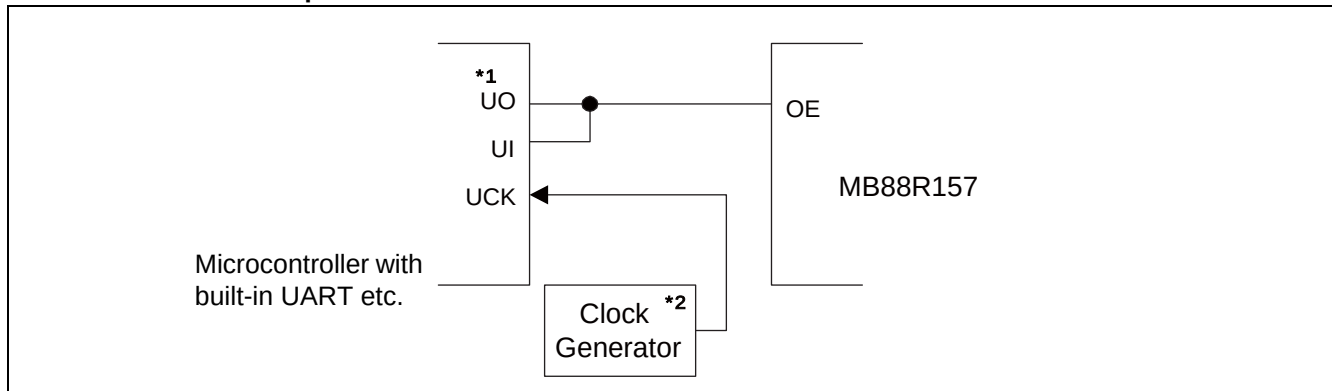
Note: This device needs to stop outputting to the OE pin of the transferred device within 15 μs after transferring "40_H" serially at the reading state and place it to a receivable state.

3. At writing : Send 8-byte data blocks from the lower address of the memory map in turn with more than 100 μs between each data block.
At read : This device outputs 8-byte data blocks from the lower address of the memory map in turn.
4. Repeat the operations of 2. and 3. for re-writing and re-reading.

To operate the device using the written data, turn on the power again.

However, the oscillation stabilization capacitance is set simultaneously with writing to memory. When the oscillation stabilization capacitance and the crystal oscillation frequency are adjusted, change the oscillation stabilization capacitance value so that the clock output from the OUT pin is set to the desired frequency.

• Interconnection example



* 1 : Set the UO pin to Hi-z to read from memory, as the UO pin serves for serial I/O.

UO : UART serial data output pin

UI : UART serial data input pin

UCK : UART serial synchronous clock I/O pin

*2 : Because the transfer rate is set to 1/512 of source oscillation in MB88R157, the clock generator is used as shown in above figure, so that the transfer speed is set to 1/512 of source clock in MB88R157. However, the clock generator is not needed if the transfer speed can be maintained from an internal clock of the baud rate generator of the UART.

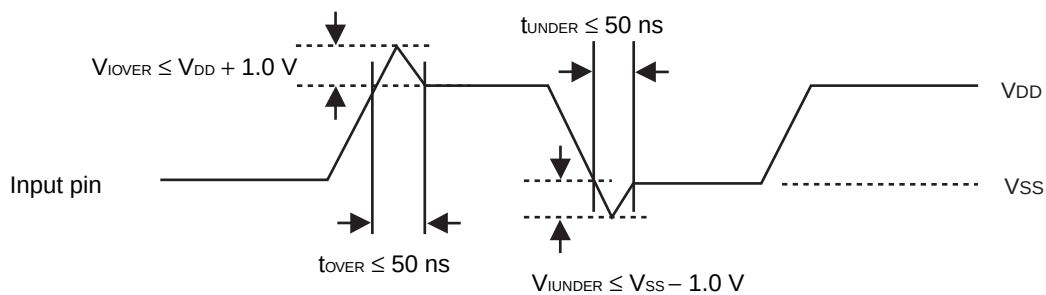
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	- 0.5	+ 4.0	V
Input voltage*	V_I	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Output voltage*	V_O	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
Storage temperature	T_{ST}	- 55	+ 125	°C
Operation junction temperature	T_J	- 40	+ 125	°C
Output current	I_O	- 14	+ 14	mA
Overshoot	V_{IOVER}	—	$V_{DD} + 1.0$ ($t_{OVER} \leq 50$ ns)	V
Undershoot	V_{IUNDER}	$V_{SS} - 1.0$ ($t_{UNDER} \leq 50$ ns)	—	V

* : This parameter is based on $V_{SS} = 0.0$ V

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ RECOMMENDED OPERATING CONDITONS

(V_{SS} = 0.0 V)

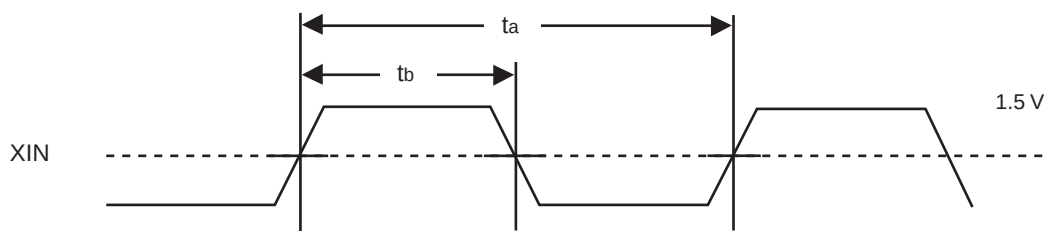
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V _{DD}	VDD	—	3.0	3.3	3.6	V
"H" level input voltage	V _{IH}	OE, PEX, XIN	Input slew rate for XIN pin only 3 V/ns	V _{DD} × 0.80	—	V _{DD} + 0.3	V
"L" level input voltage	V _{IL}			V _{SS}	—	V _{DD} × 0.20	V
Input clock duty cycle	t _{DCI}	XIN	10 MHz to 50 MHz	40	50	60	%
Operating temperature	T _a	—	Write to the internal non-volatile memory	+ 20	—	+ 50	°C
			Operating test after the re-flow				
			Other than those above	−20	—	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Input clock duty cycle ($t_{DCI} = t_b / t_a$)



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

($T_a = -20\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	I_{CC}	VDD	24 MHz input (Crystal) , 24 MHz internal oscillation, 24 MHz output no load capacitance	—	5.5	7.0	mA
	I_{CC2}		50 MHz input clock, 134 MHz internal oscillation, 134 MHz output 15 pF load capacitance	—	—	26	mA
Output voltage	V_{OH}	OUT	“H” level output Driving voltage (low) $I_{OH} = -3\text{ mA}$, Driving voltage (high) $I_{OH} = -7\text{ mA}$	$V_{DD} - 0.5$	—	V_{DD}	V
	V_{OL}		“L” level output Driving voltage (low) $I_{OL} = 3\text{ mA}$, Driving voltage (high) $I_{OL} = 7\text{ mA}$	V_{SS}	—	0.4	V
Pull-up resistance	R_{PU}	OE, PEX	—	25	50	200	k Ω
Load capacitance	C_{IN}	XIN, OE, PEX	$T_a = +25\text{ }^{\circ}\text{C}$, $V_{DD} = V_I = 0.0\text{ V}$, $f = 1\text{ MHz}$	—	—	16	pF

• AC characteristics (1)

($T_a = -20\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

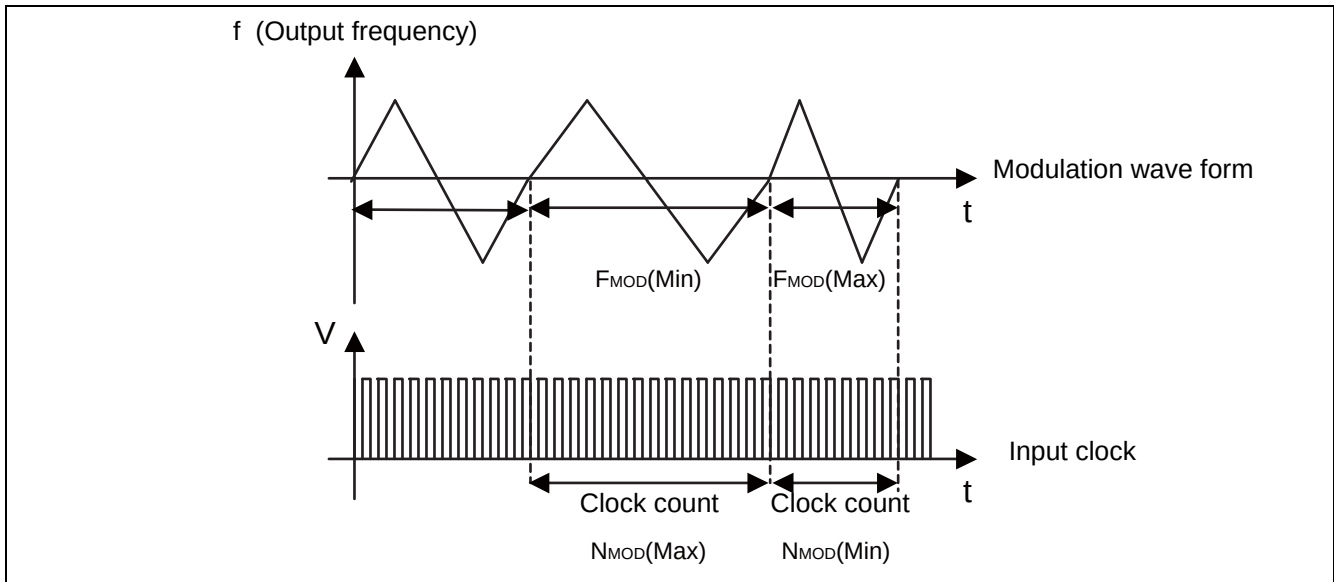
Parameter	Sym- bol	Pin name	Conditions		Value			Unit
					Min	Typ	Max	
Crystal oscillation frequency	f _x	XIN, XOUT	Fundamental oscillation		10	—	40	MHz
Input frequency	f _{in}	XIN	—		10	—	40	MHz
Internal oscillation frequency	f _{VCO}	—	—		20	—	134	MHz
Output frequency	f _{OUT}	OUT	Operation in PLL mode and at non modulation		1	—	134	MHz
			Operation at modulation		16	—	134	
Output slewing rate	SR		0.4 V to 2.4 V load capacitance 15 pF Driving ability small: at 1 MHz to 60 MHz out- put Driving ability large: at 60 MHz to 134 MHz output		0.3	—	—	V/ns
Output impedance	Z _O		Driving ability small		—	75	—	Ω
			Driving ability large		—	38	—	
Output clock duty cycle	t _{DCC}		VCO clock output		45	—	55	%
	t _{DCR}		At reference clock output		t _{DCI} −10*	—	t _{DCI} +10*	
Modulation frequency (number of clocks par one modulation)	f _{MOD} (n _{MOD})		—		f _{in} / (224 × (L+1)) (224 × (L+1))	f _{in} / (266 × (L+1)) (266 × (L+1))	f _{in} / (308 × (L+1)) (308 × (L+1))	kHz (clks)
Power supply time	t _R	VDD	0.2 V to 3.0 V		0.05	—	20	ms
Lock-up time	t _{LK}	OUT	—		—	270/f _{in} +5	270/f _{in} +10	ms
Cycle-cycle jitter	t _{JC}		No load capacitance, T _a = + 25 °C V _{DD} = 3.3 V	f _{OUT} ≥ 2 MHz	—	—	100	ps- rms
				f _{OUT} < 2 MHz	—	—	150	
Output stop time from OE exit.	t _{OD}		t _a = 1 / f _{OUT}		—	—	2 × t _a	ns
Output start time after OE entry	t _{OE}		t _a = 1 / f _{OUT}		—	—	2 × t _a	ns

* : The duty cycle value (t_{DCR}) of the source clock output depends on the duty cycle of input clock t_{DCI} . Either case of A or B will be guaranteed.

A. Resonator : Oscillating with the resonator connected with XIN, XOUT

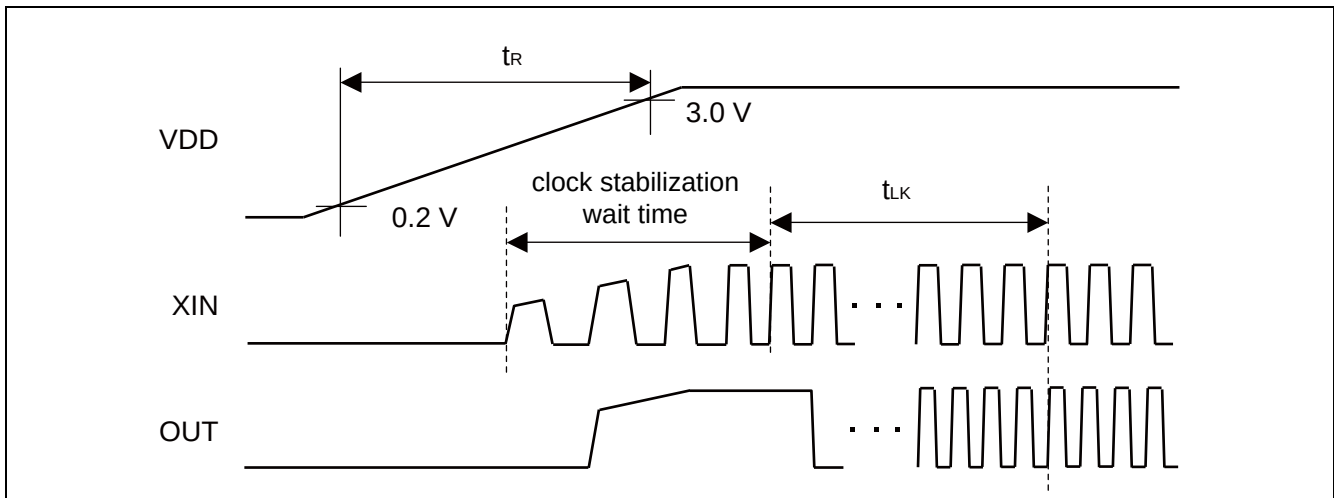
B. External clock input : The input level is Full - swing ($V_{SS} - V_{DD}$).

■ DEFINITION of MODULATION FREQUENCY and NUMBER of INPUT CLOCKS PER MODULATION

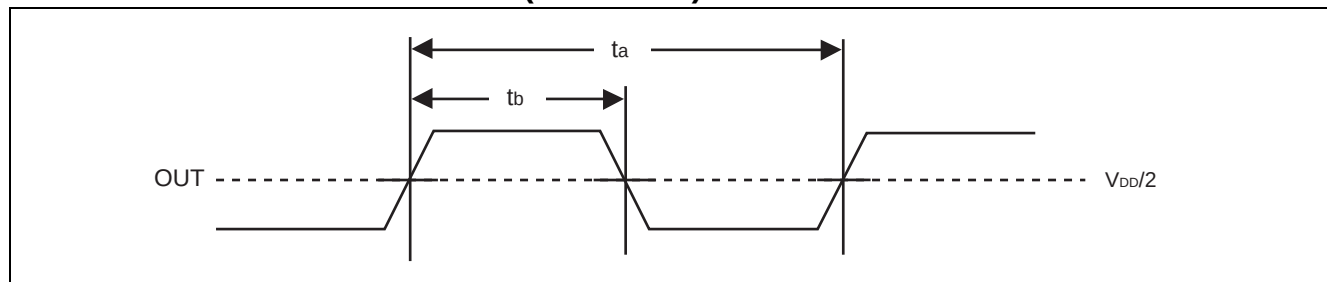


This product contains the modulation period to realize the efficient EMI reduction. The modulation period F_{MOD} depends on the input frequency and changes between $F_{MOD}(Min)$ and $F_{MOD}(Max)$. Furthermore, the typical value of the electrical characteristics is equivalent to the average value of the modulation period F_{MOD} .

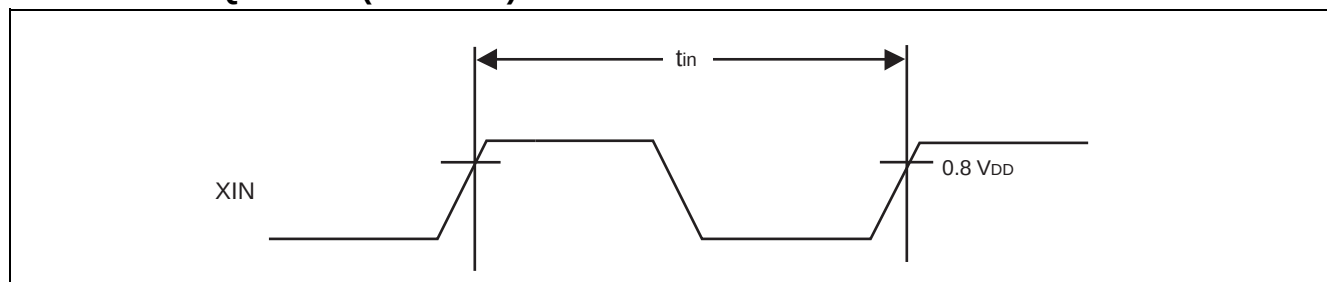
■ TURNING ON POWER SUPPLY AND LOCK-UP TIME



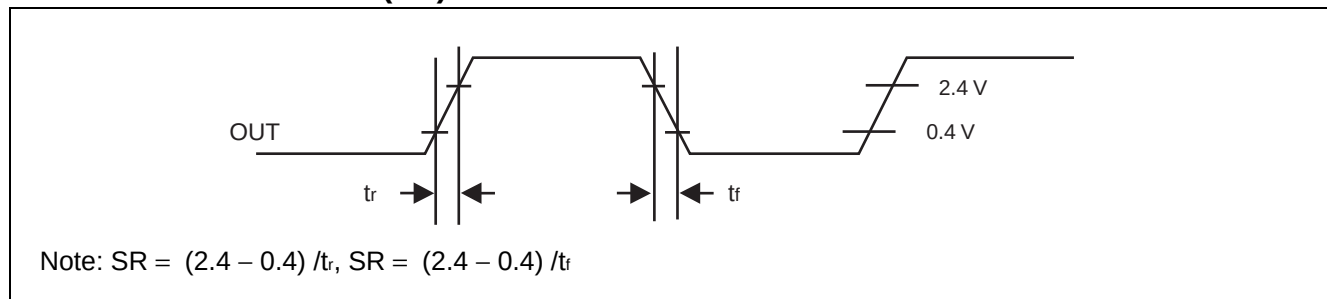
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b / t_a$)



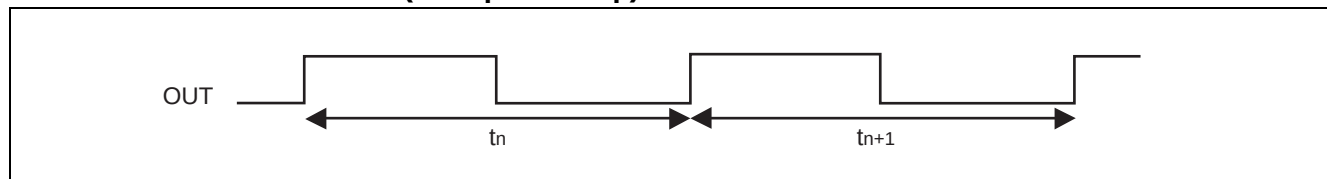
■ INPUT FREQUENCY ($f_{in} = 1 / t_{in}$)



■ OUTPUT SLEW RATE (SR)

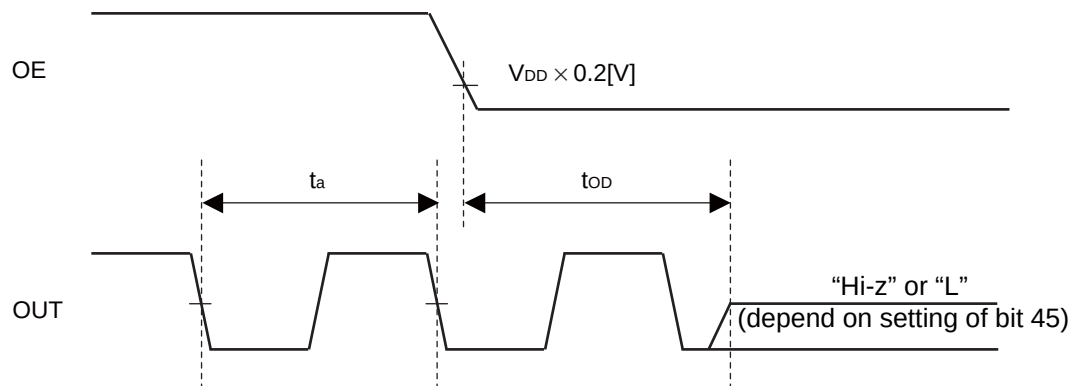


■ CYCLE-CYCLE JITTER ($t_{JC} = |t_n - t_{n+1}|$)

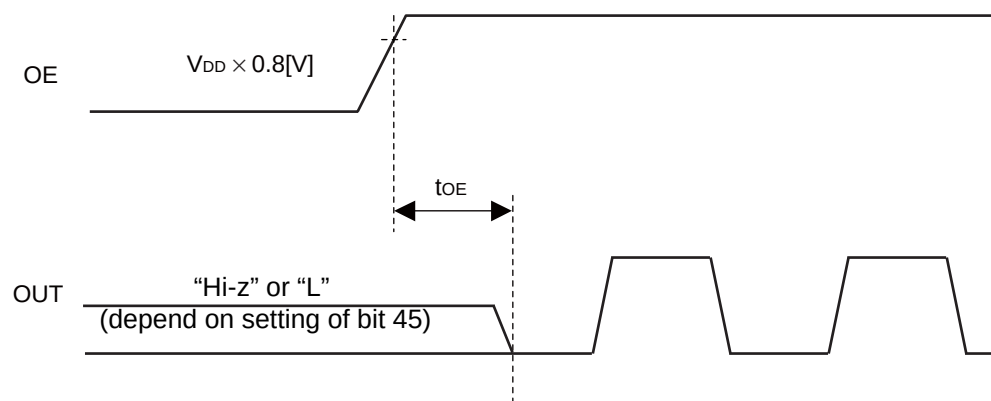


■ OUTPUT TIMING AT OE CHANGE

- Output stop time from OE exit



- Output start time after OE entry

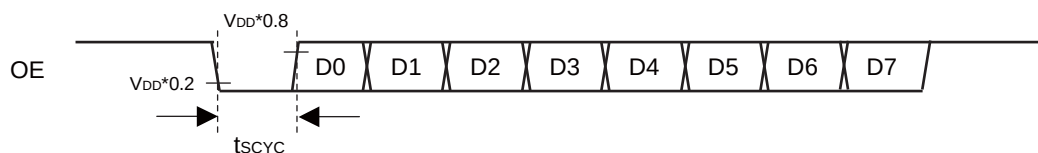


• AC characteristics (2) (Serial interface timing)

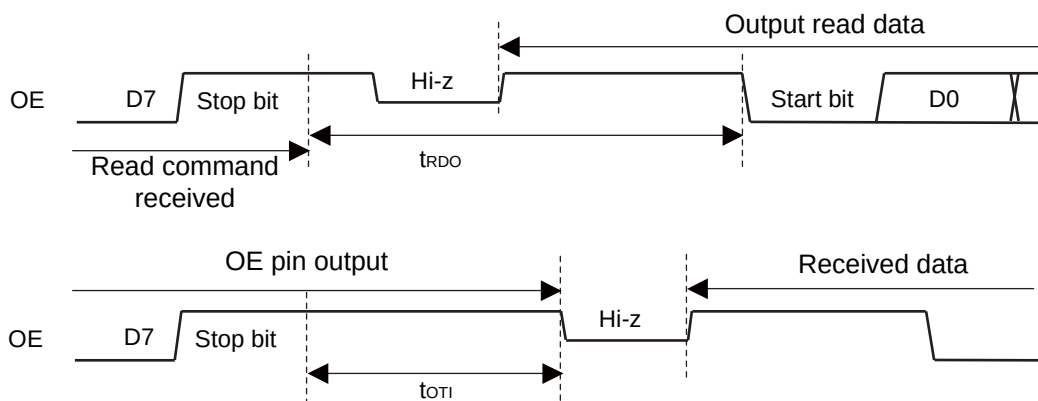
($T_a = -20\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Cycle time of transfer and receiver	t_{SCYC}	OE	—	$(t_{in} \times 512) \times 0.93$	$t_{in} \times 512$	$(t_{in} \times 512) \times 1.025$	μs
Read operation Read command receive → OE in read data output	t_{RDO}		—	15	—	—	μs
Read operation Final read data output → OE pin input mode exchanged	t_{OTI}		—	—	—	65	μs

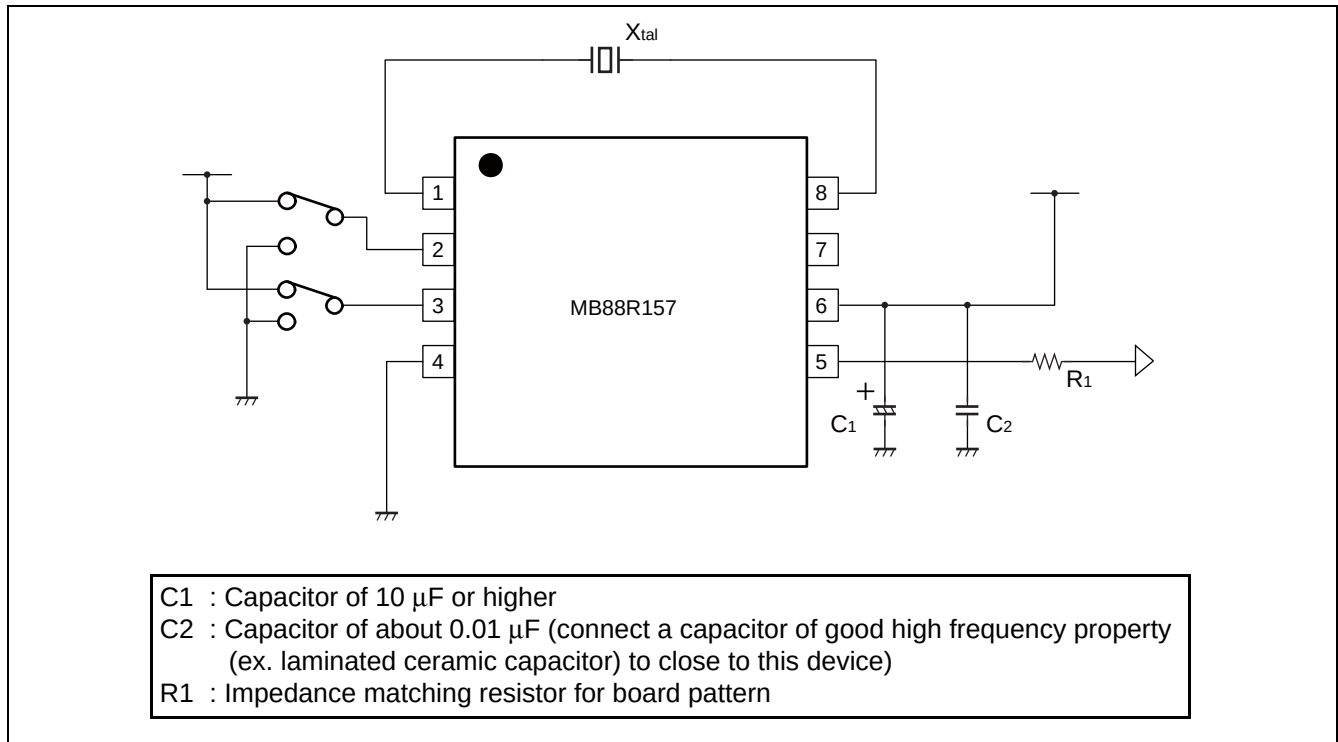
• Command / write data transfer



• Read operation



■ INTERCONNECTION CIRCUIT EXAMPLE

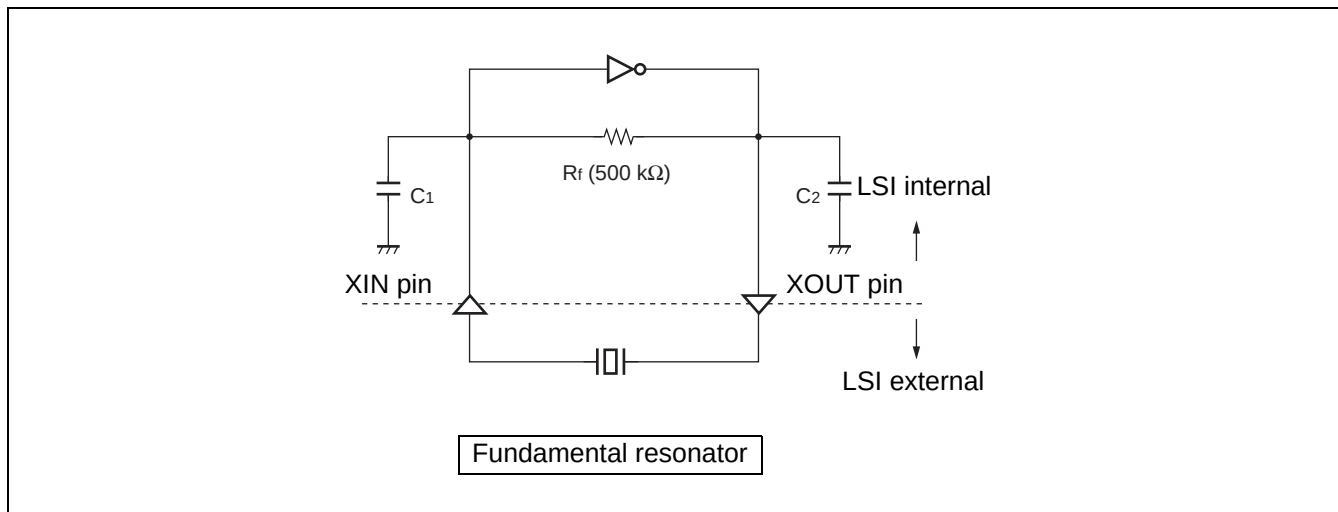


■ CRYSTAL OSCILLATION CIRCUIT

The figure below shows the connection example about general resonator. The oscillation circuit has the built-in feedback resistor (500 k Ω) and oscillation stabilization capacitance (C1 and C2).

C1 and C2 value can be changeable by setting bit49 to bit55 and bit56 to bit62 in memory. It is necessary to set suitable parameter for each resonator.

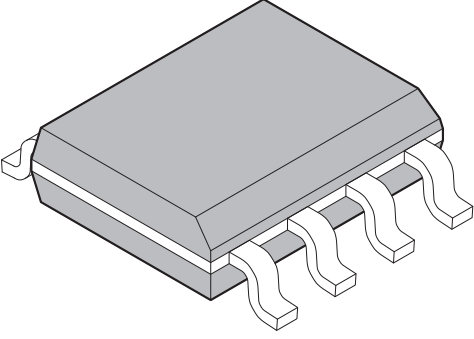
To use an external clock signal (without using the resonator), input the clock signal to the XIN pin with the XOUT pin connected to nothing.

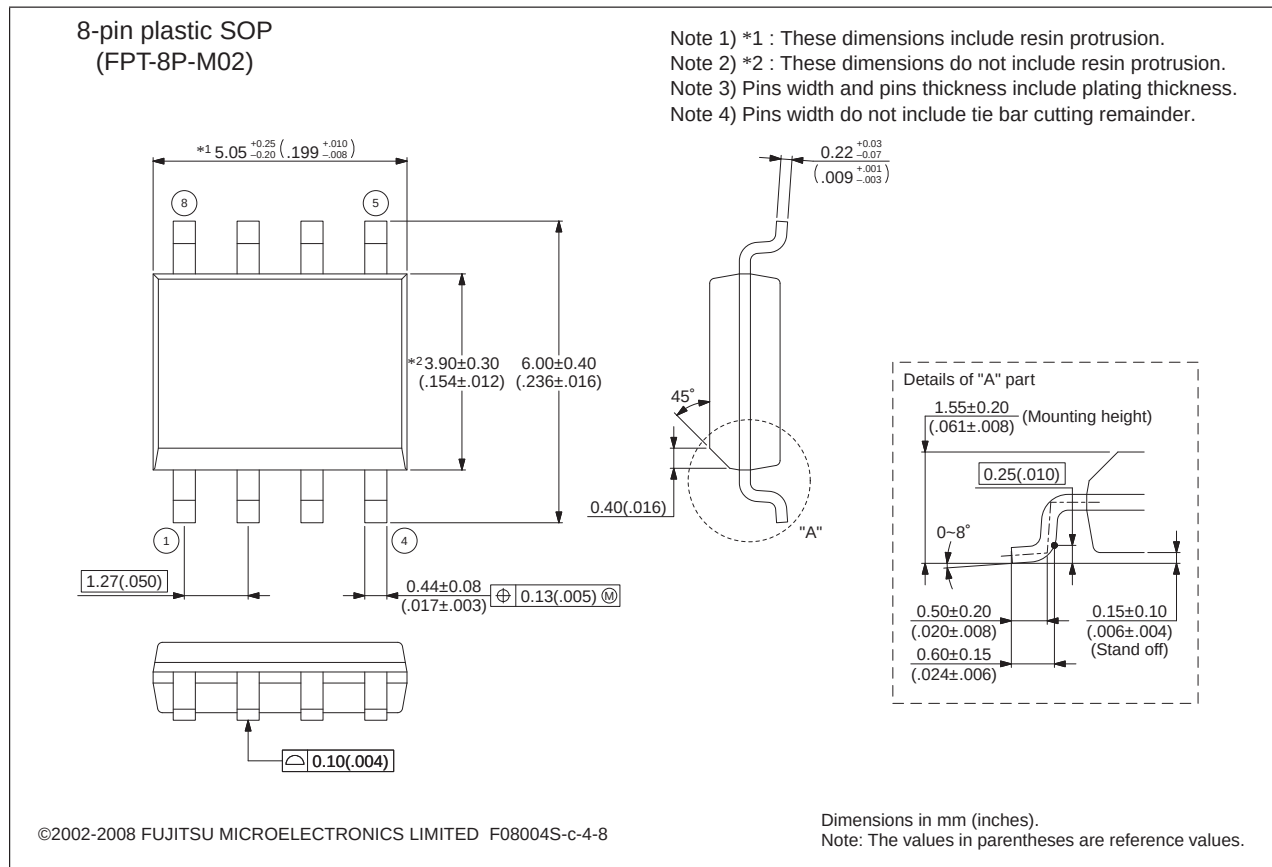


■ ORDERING INFORMATION

Part number	Package
MB88R157PNF-G-JNE1 MB88R157PNF-G-JN-ERE1 MB88R157PNF-G-JN-EFE1	8-pin plastic SOP (FPT-8P-M02)

■ PACKAGE DIMENSION

 8-pin plastic SOP (FPT-8P-M02)	Lead pitch	1.27 mm
	Package width × package length	3.9 × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g



Please confirm the latest Package dimension by following URL.
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