

AGR19030EF 30 W, 1930 MHz—1990 MHz, PCS LDMOS RF Power Transistor

Introduction

The AGR19030EF is a 30 W, 28 V N-channel laterally diffused metal oxide semiconductor (LDMOS) RF power field effect transistor (FET) suitable for personal communication service (PCS) (1930 MHz—1990 MHz), global system for mobile communication (GSM/EDGE), time division multiple access (TDMA), and single-carrier or multicarrier class AB power amplifier applications.

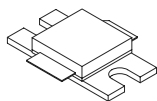


Figure 1. AGR19030EF (flanged) Package

N-CDMA Features

Typical 2 carrier N-CDMA performance: $V_{DD} = 28$ V, $I_{DQ} = 350$ mA, $f_1 = 1958.75$ MHz, $f_2 = 1961.25$ MHz, IS-95 CDMA (pilot, sync, paging, traffic codes 8—13). Peak/average (P/A) = 9.72 dB at 0.01% probability on CCDF. 1.2288 MHz transmission bandwidth (BW). Adjacent channel power ratio (ACPR) measured over 30 kHz BW at $f_1 - 885$ kHz and $f_2 + 885$ kHz. Third-order intermodulation distortion (IM3) measured over a 1.2288 MHz BW at $f_1 - 2.5$ MHz and $f_2 + 2.5$ MHz.

- Output power (P_{OUT}): 6 W.
- Power gain: 16 dB.
- Efficiency: 24.8%.
- IM3: -34.5 dBc.
- ACPR: -49 dBc.

EDGE Features

Typical EDGE performance, 1960 MHz, 26 V, $I_{DQ} = 250$ mA:

- Output power (P_{OUT}): 12 W typical.
- Power gain: 15.5 dB.
- Efficiency: 38% typical.
- Modulation spectrum:
 - @ ± 400 kHz = -61 dBc.
 - @ ± 600 kHz = -74 dBc.
- Error vector magnitude (EVM) = 2.2%

GSM Features

Typical performance over entire GSM band:

- P1dB: 30 W typical.
- Continuous wave (CW) power gain: @ P1dB = 15 dB.
- CW efficiency @ P1dB = 55% typical.
- Return loss: -12 dB.

Device Performance Features

High-reliability, gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 1930 MHz, 30 W CW output power.

Large signal impedance parameters available.

ESD Rating*

AGR19030EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Table 1. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	$^{\circ}\text{C/W}$

Table 2. Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at $T_C = 25^{\circ}\text{C}$	P_D	87.5	W
Derate Above 25°C	—	0.5	$\text{W}/^{\circ}\text{C}$
Operating Junction Temperature	T_J	200	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	–65, 150	$^{\circ}\text{C}$

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Recommended operating conditions apply unless otherwise specified: $T_C = 30^{\circ}\text{C}$.

Table 3. dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 150\text{ }\mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current ($V_{GS} = 5\text{ V}$, $V_{DS} = 0\text{ V}$)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$)	I_{DSS}	—	—	50	μAdc
On Characteristics					
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 0.4\text{ A}$)	G_{FS}	—	2.4	—	S
Gate Threshold Voltage ($V_{DS} = 10\text{ V}$, $I_D = 100\text{ }\mu\text{A}$)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ V}$, $I_D = 300\text{ mA}$)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage ($V_{GS} = 10\text{ V}$, $I_D = 0.4\text{ A}$)	$V_{DS(ON)}$	—	0.3	—	Vdc

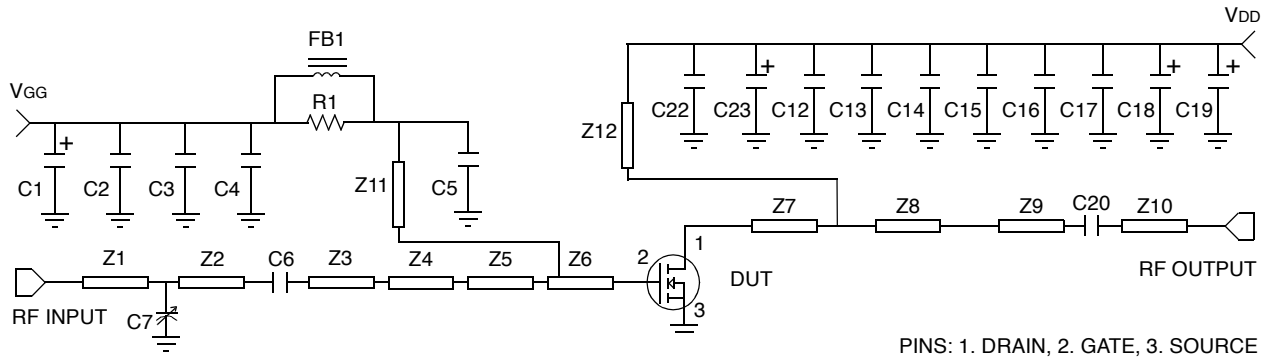
Electrical Characteristics (continued)

Recommended operating conditions apply unless otherwise specified: $T_c = 30\text{ }^{\circ}\text{C}$.

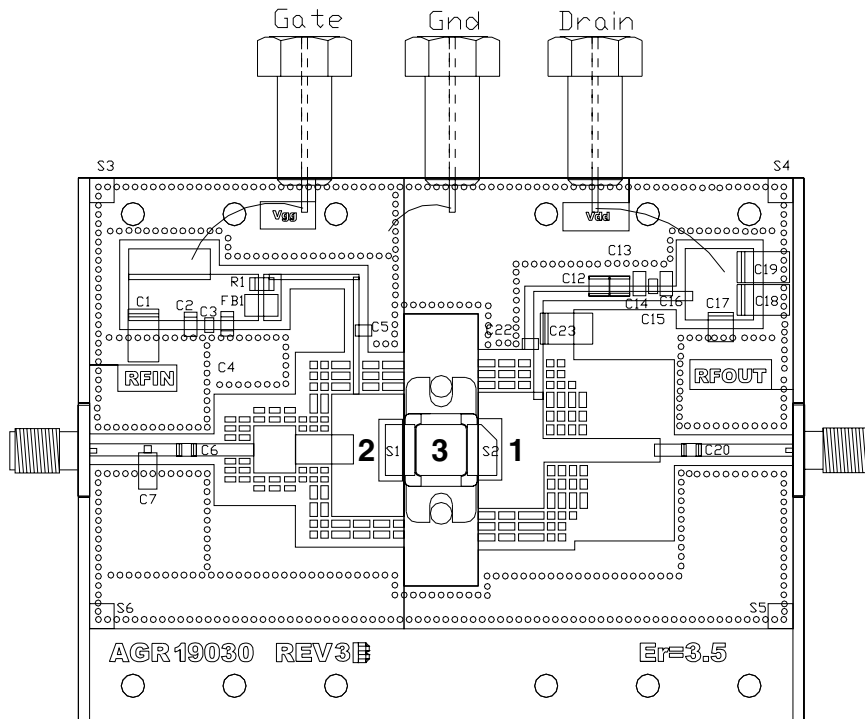
Table 4. RF Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance ($V_{DS} = 28\text{ V}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$) (This part is internally matched on both the input and output.)	CRSS	—	0.8	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{OUT} = 6\text{ W Avg.}$, 2-carrier N-CDMA, $I_{DQ} = 350\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1932.5\text{ MHz}$, and $f_1 = 1987.5\text{ MHz}$, $f_2 = 1990\text{ MHz}$)	GPS	15.5	16	—	dB
Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{OUT} = 6\text{ W Avg.}$, 2-carrier N-CDMA, $I_{DQ} = 350\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1932.5\text{ MHz}$, and $f_1 = 1987.5\text{ MHz}$, $f_2 = 1990\text{ MHz}$)	η	—	24.8	—	%
Third-order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{OUT} = 6\text{ W Avg.}$, 2-carrier N-CDMA, $I_{DQ} = 350\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1932.5\text{ MHz}$, and $f_1 = 1987.5\text{ MHz}$, $f_2 = 1990\text{ MHz}$; IM3 measured in a 1.2288 integration BW centered at $f_1 - 2.5\text{ MHz}$ and $f_2 + 2.5\text{ MHz}$, referenced to the carrier channel power)	IM3	—	−34.5	—	dBc
Adjacent Channel Power Ratio ($V_{DD} = 28\text{ Vdc}$, $P_{OUT} = 6\text{ W Avg.}$, 2-carrier N-CDMA, $I_{DQ} = 350\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1932.5\text{ MHz}$, and $f_1 = 1987.5\text{ MHz}$, $f_2 = 1990\text{ MHz}$; IM3 measured in a 1.2288 integration BW centered at $f_1 - 2.5\text{ MHz}$ and $f_2 + 2.5\text{ MHz}$, referenced to the carrier channel power)	ACPR	—	−49.0	—	dBc
Output Power at 1 dB Gain Compression ($V_{DD} = 28\text{ V}$, $P_{OUT} = 30\text{ W CW}$, $f = 1990\text{ MHz}$, $I_{DQ} = 350\text{ mA}$)	P1dB	30	35	—	W
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{OUT} = 6\text{ W Avg.}$, 2-carrier N-CDMA, $I_{DQ} = 350\text{ mA}$, $f_1 = 1930\text{ MHz}$, $f_2 = 1932.5\text{ MHz}$, and $f_1 = 1987.5\text{ MHz}$, $f_2 = 1990\text{ MHz}$)	IRL	—	−12	—	dB
Ruggedness ($V_{DD} = 28\text{ V}$, $P_{OUT} = 30\text{ W CW}$, $I_{DQ} = 350\text{ mA}$, $f = 1930\text{ MHz}$, $V_{SWR} = 10:1$ [all phase angles])	Ψ	No degradation in output power.			

Test Circuit Illustrations for AGR19030EF



A. Schematic



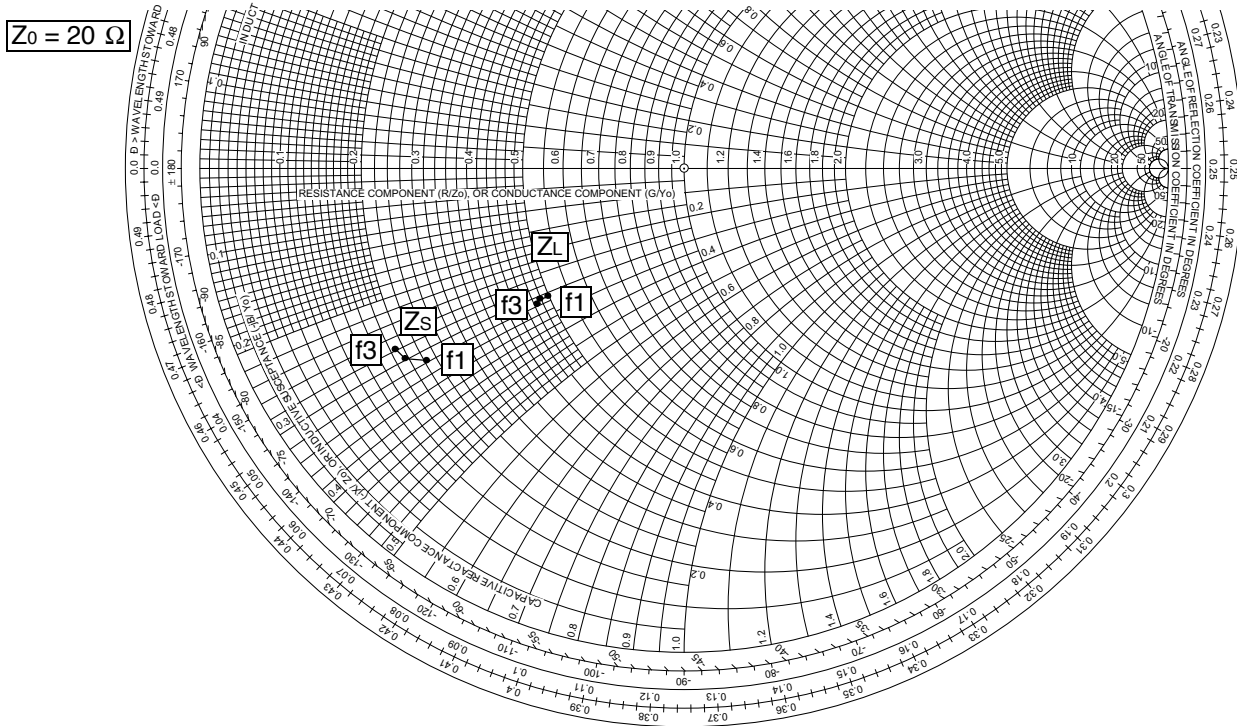
B. Component Layout

Parts List:

- Microstrip line: Z1, 0.315 in. x 0.067 in.; Z2, 0.195 in. x 0.067 in.; Z3, 0.345 in. x 0.067 in.; Z4, 0.230 in. x 0.260 in.; Z5, 0.200 in. x 0.160 in.; Z6, 0.395 in. x 0.675 in.; Z7, 0.355 in. x 0.640 in.; Z8, 0.645 in. x 0.130 in.; Z9, 0.145 in. x 0.067 in.; Z10, 0.535 in. x 0.067 in.; Z11, 0.345 in. x 0.030 in.; Z12, 0.275 in. x 0.050 in.
- ATC® B case chip capacitors: C5, C22: 8.2 pF 100B8R2JCA500X; C6, C20: 10 pF 100B100JCA500X; C12: 100 pF 102B100JCA500X; C13: 1000 pF 103B100JCA500X.
- Kemet® B case chip capacitors: C2, C16: 0.10 μ F CDR33VX104AKWS; tantalum capacitor: C17: 1 μ F 50 V T491C.
- Vitramon® 1206: C4, C14: 22000 μ F.
- Sprague® tantalum SMT (35 V): C1, C19, C23: 22 μ F; C18: 10 μ F.
- Murata® 0805: C3, C15: 0.01 μ F, GRM40X7R103K100AL.
- Johanson Giga-Trin® variable capacitors: C7, 0.4 pF—2.5 pF.
- Fair-Rite® ferrite bead: FB1: 2743019447.
- Fixed film chip resistor: R1: 12 Ω , 0.25 W, 0.08 x 0.13.
- PCB etched circuit boards
- Taconic® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, $\epsilon_r = 3.5$.

Figure 2. AGR19030EF Test Circuit

Typical Performance Characteristics



MHz (f)	$Z_s \, \Omega$ (Complex Source Impedance)	$Z_L \, \Omega$ (Complex Optimum Load Impedance)
1930 (f1)	$4.49 - j6.43$	$10.00 - j6.30$
1960 (f2)	$4.06 - j5.98$	$9.65 - j6.25$
1990 (f3)	$3.78 - j5.61$	$9.44 - j6.33$

Note: Z_L was chosen based on trade-offs between gain, output power, drain efficiency, and intermodulation distortion.

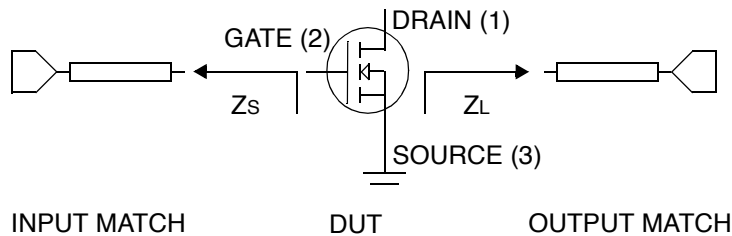
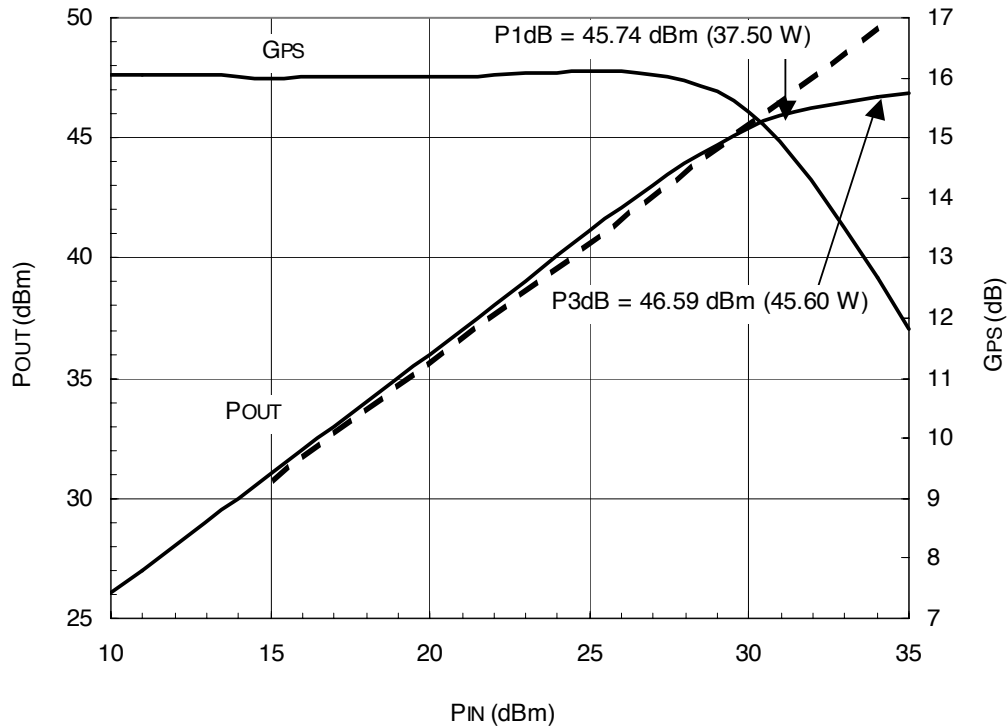


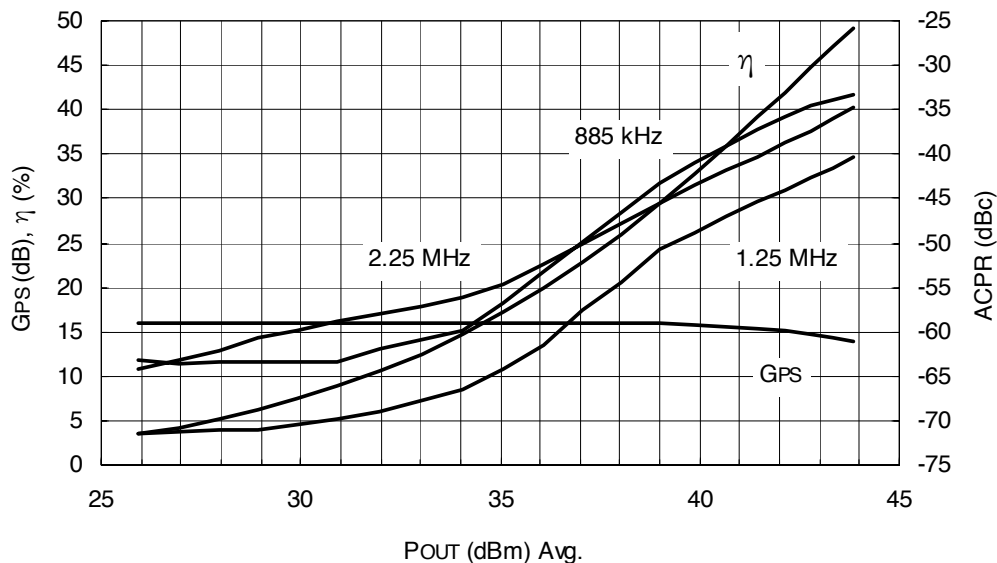
Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)



Test Conditions:
 $V_{DD} = 28$ Vdc, $I_{DQ} = 350$ mA, pulsed CW, 4 μ s (on), 40 μ s (off), center frequency = 1960 MHz.

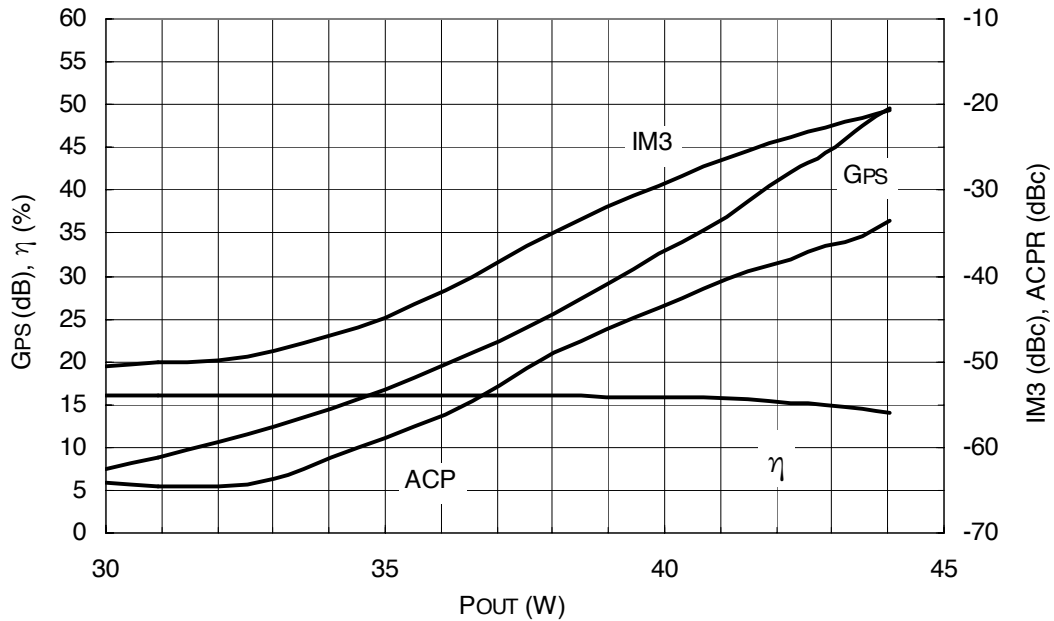
Figure 4. CW POUT vs. PIN



Test Conditions:
 $V_{DD} = 28$ Vdc, $I_{DQ} = 350$ mA, $f = 1960$ MHz, N-CDMA, 2.5 MHz @ 1.2288 MHz BW, P/A = 9.72 dB @ 0.01% probability (CCDF), channel spacing (BW) 885 kHz (30 kHz), 1.25 MHz (12.5 kHz), 2.25 MHz (1 MHz).

Figure 5. N-CDMA ACPR, Power Gain, and Drain Efficiency vs. POUT

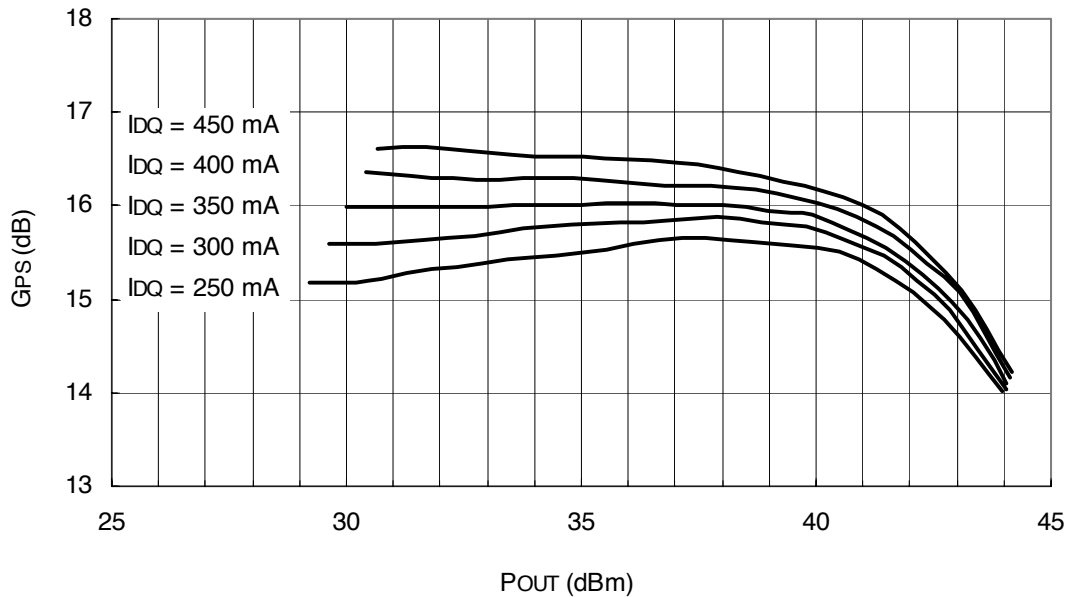
Typical Performance Characteristics (continued)



Test Conditions:

$V_{DD} = 28$ Vdc, $I_{DQ} = 350$ mA, $f_1 = 1958.75$ MHz, $f_2 = 1961.25$ MHz, 2 x N-CDMA, 2.5 MHz @ 1.2288 MHz BW, P/A = 9.72 dB @ 0.01% probability (CCDF), channel spacing (BW) ACPR: 885 kHz (30 kHz), IM3: 2.5 MHz (1.2288 MHz).

Figure 6. 2-Carrier N-CDMA ACPR, IM3 Power Gain, and Drain Efficiency vs. P_{OUT}

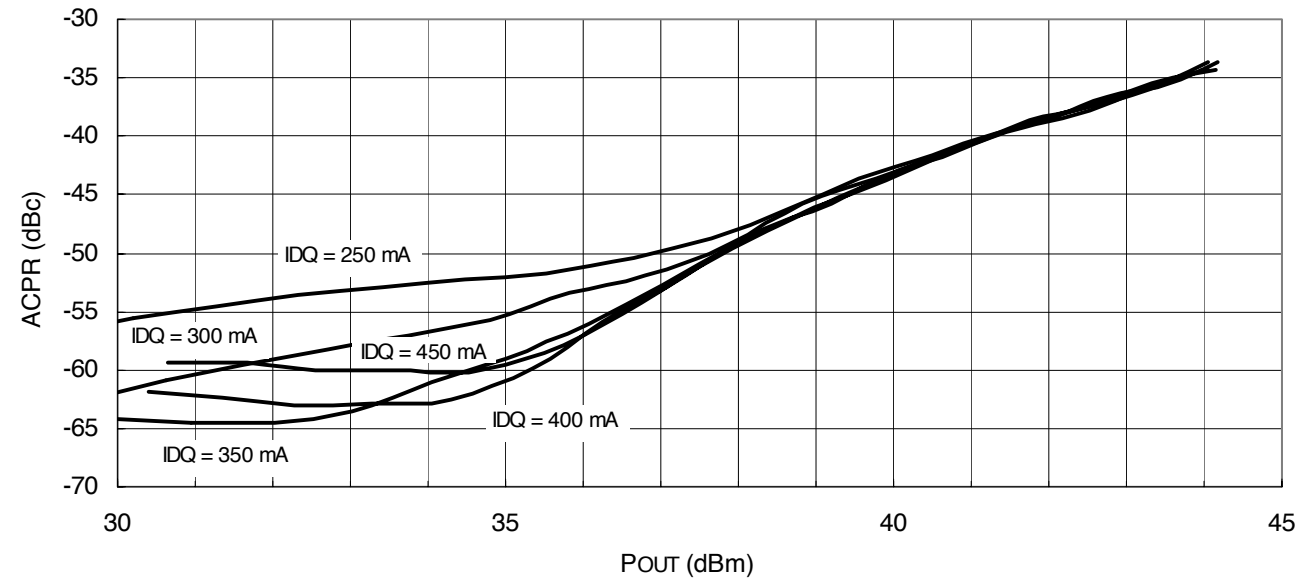


Test Conditions:

$V_{DD} = 28$ Vdc, $f_1 = 1958.75$ MHz, $f_2 = 1961.25$ MHz, 2 carrier N-CDMA measurement.

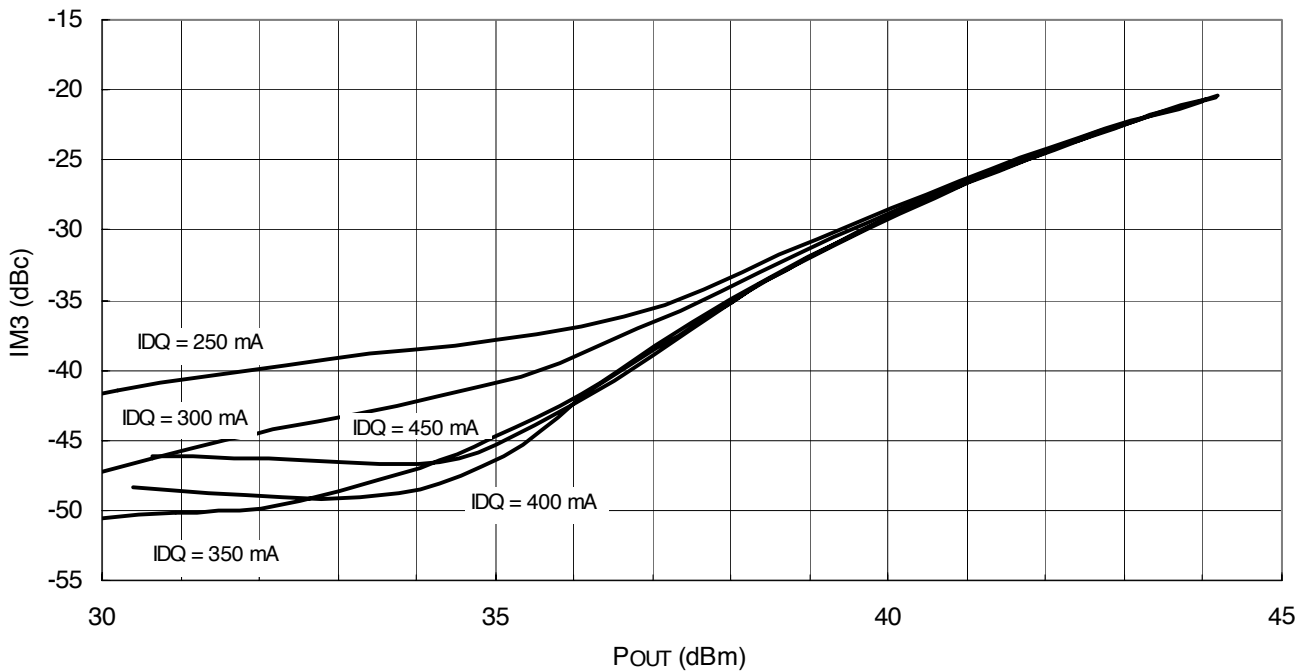
Figure 7. 2-Carrier N-CDMA Power Gain vs. P_{OUT}

Typical Performance Characteristics (continued)



Test Conditions:
 VDD = 28 Vdc, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2 carrier N-CDMA measurement.

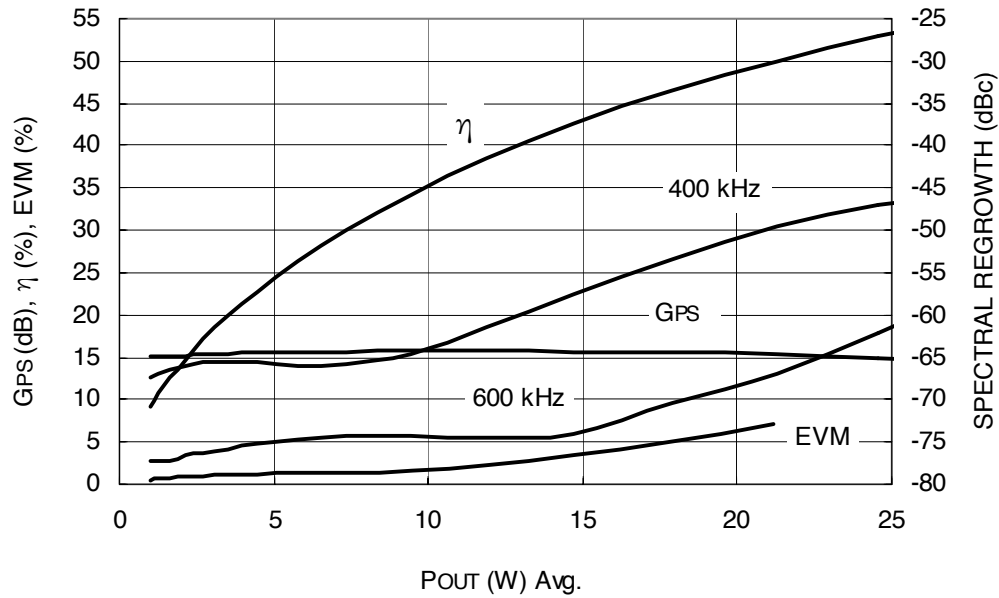
Figure 8. ACPR vs. Pout



Test Conditions:
 VDD = 28 Vdc, f1 = 1958.75 MHz, f2 = 1961.25 MHz, 2 carrier N-CDMA measurement.

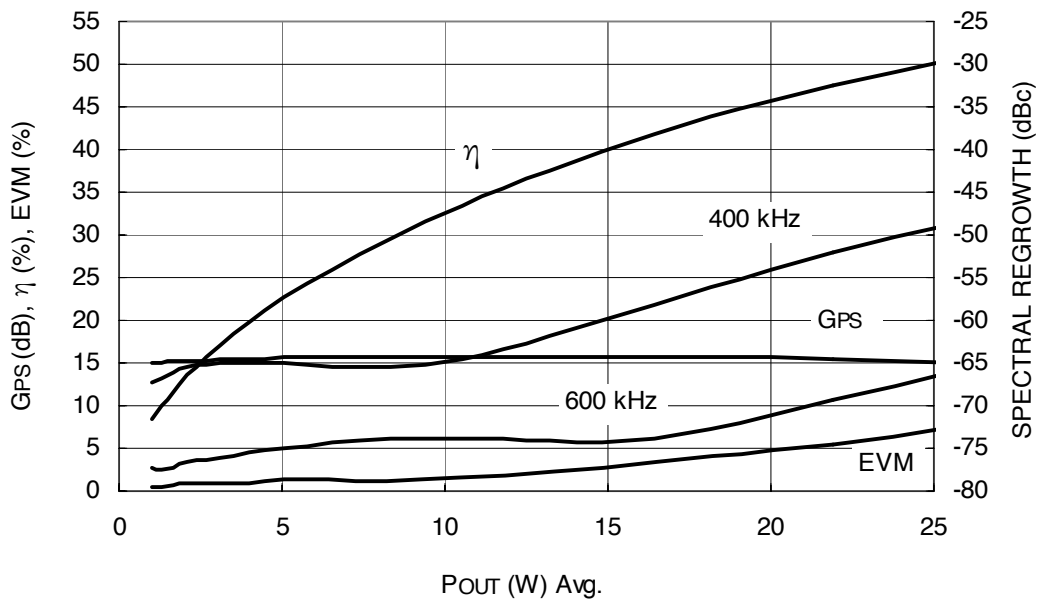
Figure 9. IM3 vs. Pout

Typical Performance Characteristics (continued)



Test Conditions:
 $V_{DD} = 26 \text{ Vdc}$, $I_{DQ} = 250 \text{ mA}$, $f = 1960 \text{ MHz}$, modulation = GSM/EDGE.

Figure 10. GSM/EDGE Power Gain, Drain Efficiency, Spectral Regrowth, and EVM vs. P_{out}



Test Conditions:
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 250 \text{ mA}$, $f = 1960 \text{ MHz}$, modulation = GSM/EDGE.

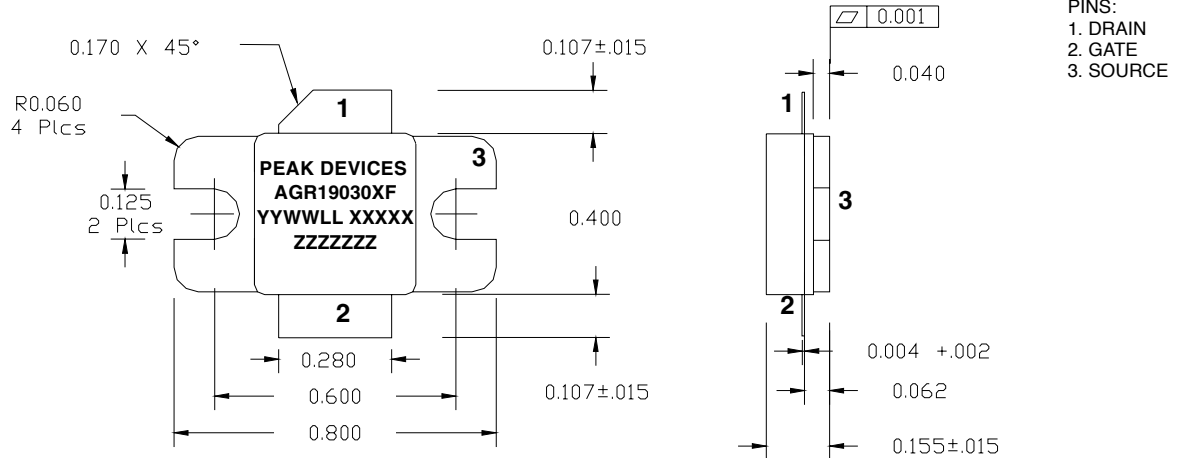
Figure 11. GSM/EDGE Power Gain, Drain Efficiency, Spectral Regrowth, and EVM vs. P_{out}

AGR19030EF
30 W, 1930 MHz—1990 MHz, PCS LDMOS RF Power Transistor

Package Dimensions

All dimensions are in inches. Tolerances are ± 0.005 in. unless specified.

AGR19030EF



Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; T = Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.