P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-92	TO-243AA*	Die
-500V	30Ω	-0.2A	VP2450N3	VP2450N8	VP2450ND

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

Features

- ❑ Free from secondary breakdown
- ❑ Low power drive requirement
- ❑ Ease of paralleling
- ❑ Low C_{ISS} and fast switching speeds
- ❑ Excellent thermal stability
- ❑ Integral Source-Drain diode
- ❑ High input impedance and high gain
- ❑ Complementary N- and P-channel devices

Product marking for TO-243AA:

VP4E✳

Where ✳ = 2-week alpha date code

Applications

- ❑ Motor controls
- ❑ Converters
- ❑ Amplifiers
- ❑ Switches
- ❑ Power supply circuits
- ❑ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

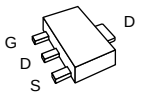
* Distance of 1.6 mm from case for 10 seconds.

Package Options



S G D

TO-92



TO-243AA
(SOT-89)

Note: See Package Outline section for dimensions.

Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: http://www.supertex.com. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.1A	-0.3A	1W	125	170	-0.1A	-0.3A
TO-243AA	-0.16A	-0.80A	1.6W†	15	78	-0.16A	-0.80A

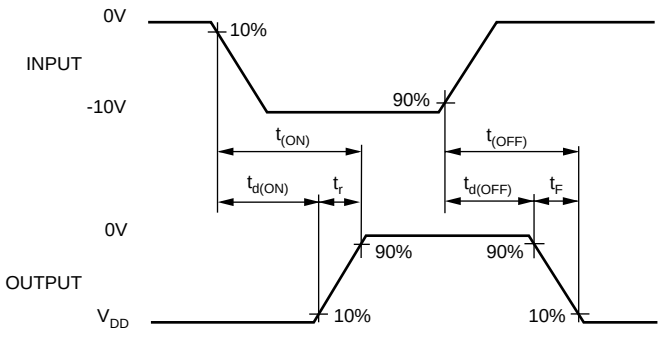
* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 Board. 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

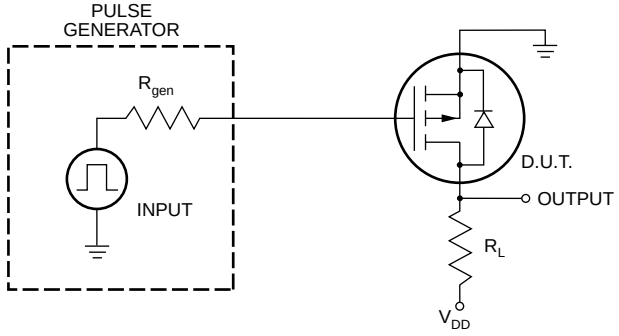
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-500			V	V_{GS} = 0V, I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	-1.5		-3.5	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage			-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			-10	μA	V_{GS} = 0V, V_{DS} = Max Rating
				-1	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	-75			mA	V_{GS} = -4.5V, V_{DS} = -15V
		-200				V_{GS} = -10V, V_{DS} = -15V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			35	Ω	V_{GS} = -4.5V, I_D = -50mA
				30		V_{GS} = -10V, I_D = -100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	%/°C	V_{GS} = -10V, I_D = -100mA
G_{FS}	Forward Transconductance	150	320		m℧	V_{DS} = -15V, I_D = -100mA
C_{ISS}	Input Capacitance			190	pF	V_{GS} = 0V, V_{DS} =- 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			75		
C_{RSS}	Reverse Transfer Capacitance			20		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	V_{DD} = -25V, I_D = -200mA, R_{GEN} = 25Ω
t_r	Rise Time			25		
$t_{d(OFF)}$	Turn-OFF Delay Time			45		
t_f	Fall Time			25		
V_{SD}	Diode Forward Voltage Drop			-1.8	V	V_{GS} = 0V, I_{SD} = -100mA
t_{rr}	Reverse Recovery Time		300		ns	V_{GS} = 0V, I_{SD} = -100mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

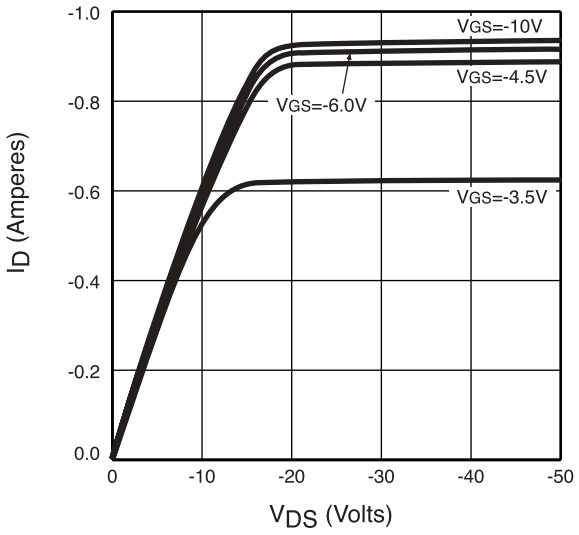
Switching Waveforms and Test Circuit



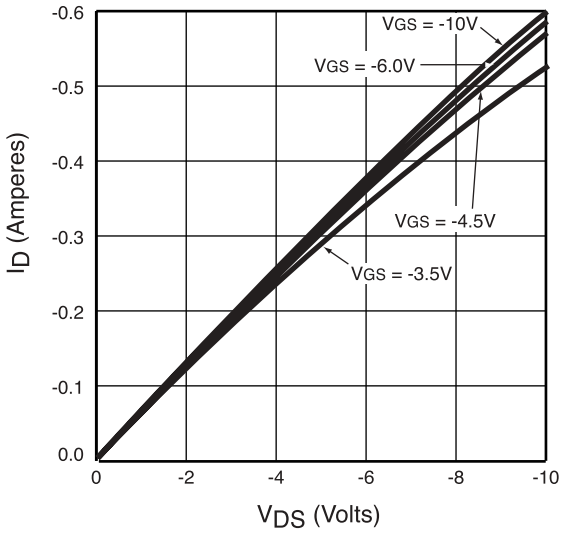


Typical Performance Curves

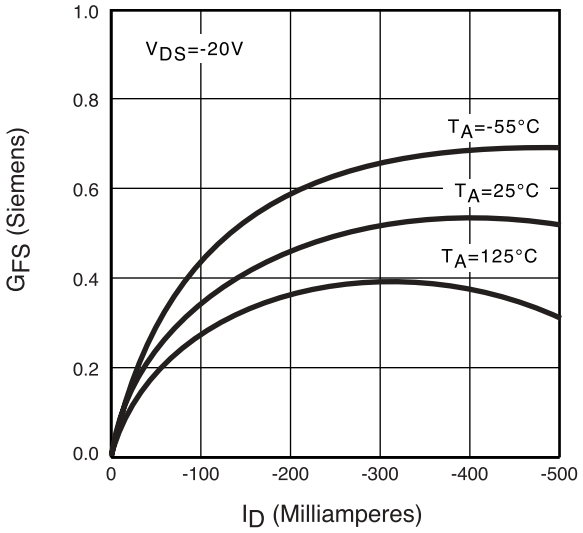
Output Characteristics



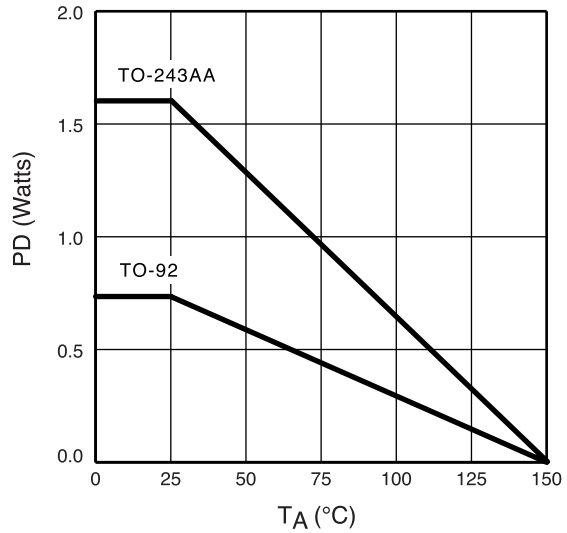
Saturation Characteristics



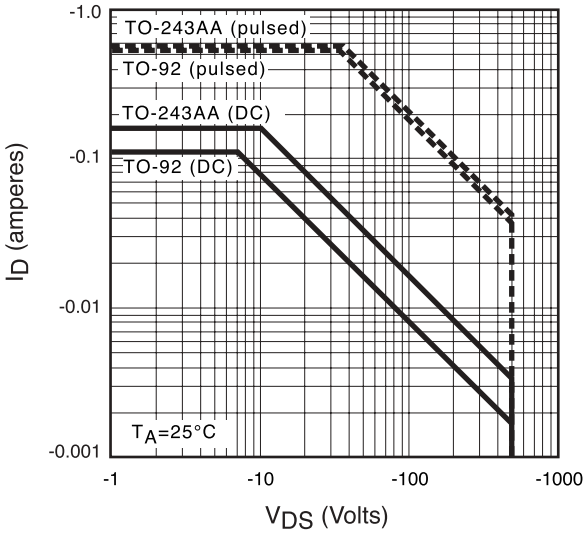
Transconductance vs. Drain Current



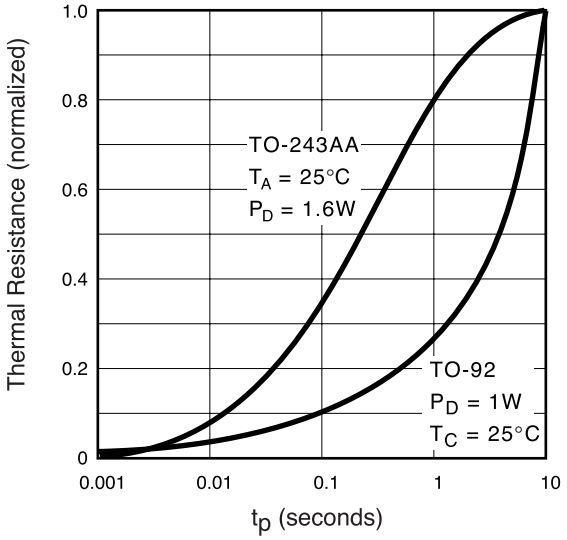
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

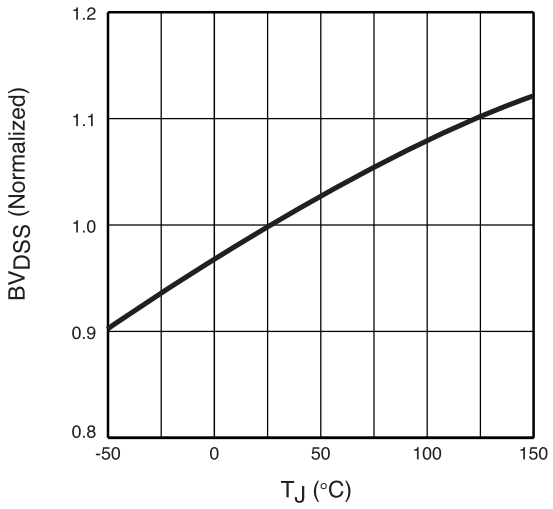


Thermal Response Characteristics

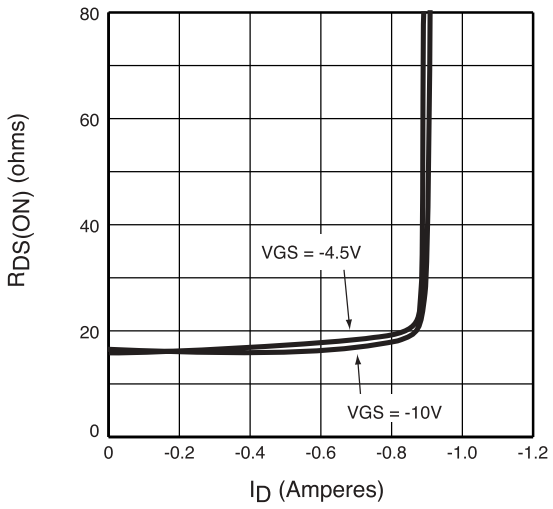


Typical Performance Curves

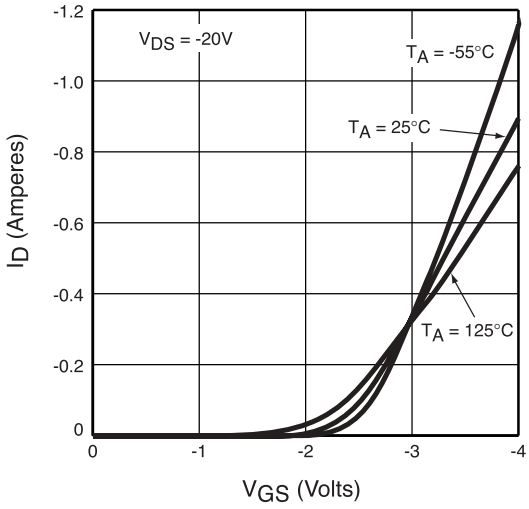
BV_{DSS} Variation with Temperature



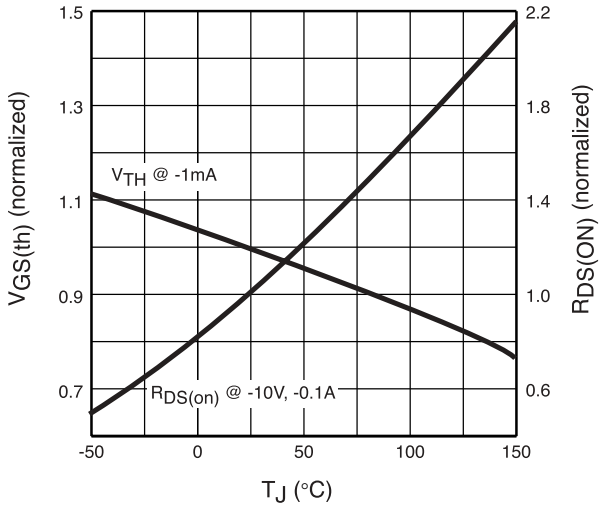
On Resistance vs. Drain Current



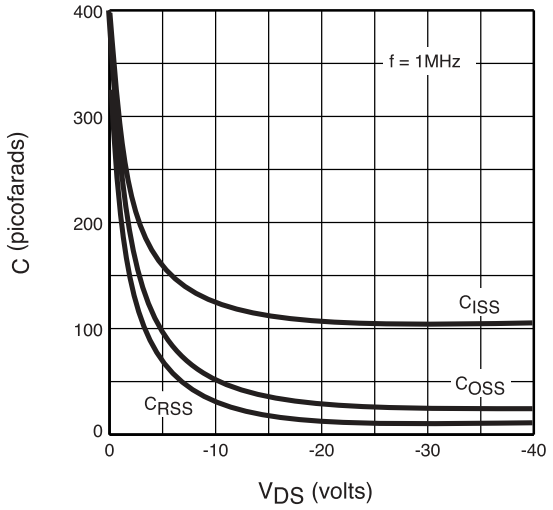
Transfer Characteristics



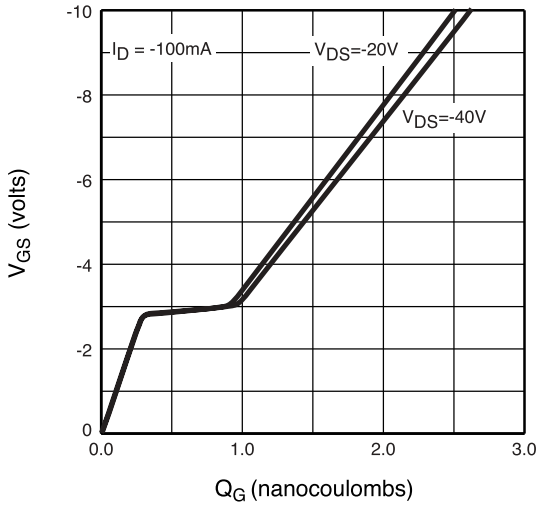
$VGS_{(th)}$ and $R_{DS(on)}$ Variation w/ Temperature



Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics



Supertex inc.

©2002 Supertex Inc. All rights reserved. Unauthorized use or reproduction prohibited.

1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 744-0100 • FAX: (408) 222-4895
www.supertex.com