TEXAS INSTRUMENTS
TPS62097
ZHCSMN1A – DECEMBER 2015 – REVISED JANUARY 2021

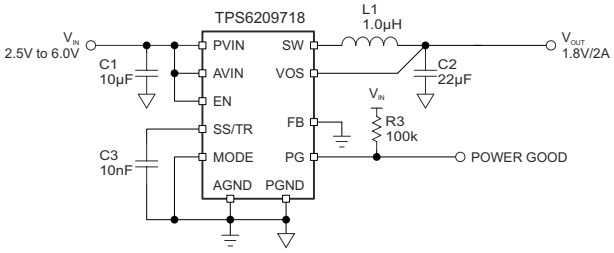
具有 iDCS-Control、强制 PWM 模式和可选开关频率的 TPS62097 2A 高效降压转换器

1 特性

- 推出的新产品：采用 SOT583 封装的 TPS62851x 6V、0.5A/1A/2A 降压转换器
- iDCS-Control 拓扑
- 强制 PWM 或省电模式
- 效率高达 97%
- 2.5V 至 6.0V 输入电压
- 可调输出电压：0.8V 至 V_{IN}
- 1.8V 和 3.3V 固定输出电压
- ±1% 的输出电压精度
- 断续短路保护
- 可编程软启动
- 输出电压跟踪
- 可选开关频率
- 100% 占空比，可实现超低压降
- 输出放电
- 电源正常状态输出
- 热关断保护
- -40°C 至 125°C 的工作结温范围
- 采用 2mm × 2mm VQFN 封装

2 应用

- 电机驱动器
- 可编程逻辑控制器 (PLC)
- 固态硬盘 (SSD)
- 负载点 (POL) 稳压器



1.8V 输出，PWM/PSM 模式应用

3 说明

TPS62097 器件是一款同步降压转换器，针对高效率和噪声关键型应用进行了优化。此器件主要用于宽输出电流范围内的高效转换。在中等负载至重负载状态下，此转换器在 PWM 模式下运行，且会在轻负载下自动进入节能运行模式。可使用外部电阻器在 1.5MHz 至 2.5MHz 之间选择开关频率。iDCS-Control 可在强制 PWM 模式下以恒定开关频率实现低噪声运行。

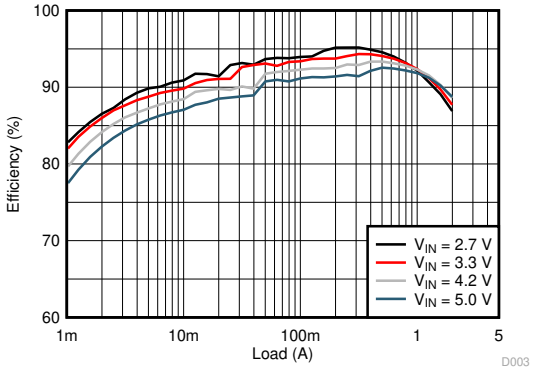
为了解决系统电源轨的需求，内部补偿电路支持使用电容值高于 150µF 的各种外部输出电容器。为在启动过程中控制浪涌电流，此器件通过连接至 SS/TR 引脚的外部电容器提供了可编程的软启动。SS/TR 引脚还可用于电压跟踪配置中。此器件还集成了短路保护、电源正常和热关断特性。此器件采用 2mm x 2mm VQFN 封装。

新产品 TPS62851x 提供更低的 BOM 成本、更小的解决方案总尺寸以及其他特性。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS62097	VQFN (11)	2.0mm x 2.0mm
TPS6209718		
TPS6209733		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



1.8V 输出，PWM/PSM 模式效率

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2015) to Revision A (January 2021)	Page
• 添加了指向新器件 (TPS62851x) 的链接	1
• 添加了指向 TI 网站上相关应用页面的链接	1
• 更新了整个文档的表、图和交叉参考的编号格式。	1

5 Device Options

PART NUMBER(1)	OUTPUT VOLTAGE	PACKAGE MARKING
TPS62097	Adjustable	ZFZ5
TPS6209718	1.8V	ZGB5
TPS6209733	3.3V	ZGC5

(1) For detailed ordering information, please check the Mechanical, Packaging, and Orderable Information section at the end of this datasheet.

6 Pin Configuration and Functions

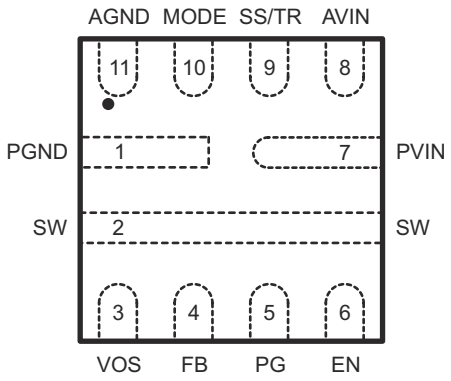


图 6-1. 11-Pin VQFN RWK Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND	1		Power ground pin
SW	2	PWR	Switch pin. It is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
VOS	3	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
FB	4	I	Feedback pin. For the fixed output voltage versions, this pin is recommended to be connected to AGND for improved thermal performance. The pin also can be left floating as an internal 400-kΩ resistor is connected between this pin and AGND for fixed output voltage versions. For the adjustable output voltage version, a resistor divider sets the output voltage.
PG	5	O	Power-good open-drain output pin. The pullup resistor should not be connected to any voltage higher than 6 V. If it is not used, leave the pin floating.
EN	6	I	Enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. This pin has an internal pulldown resistor of typically 375 kΩ when the device is disabled.
PVIN	7	PWR	Power input supply pin
AVIN	8	I	Analog input supply pin. Connect it to the PVIN pin together.
SS/TR	9	I	Soft start-up and voltage tracking pin. A capacitor is connected to this pin to set the soft start-up time. Leaving this pin floating sets the minimum start-up time.
MODE	10	I	Mode selection pin. Connect this pin to AGND to enable Power Save Mode with automatic transition between PWM and Power Save Mode. Connect this pin to an external resistor or leave floating to enable forced PWM mode only. See 表 8-1.
AGND	11		Analog ground pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage at Pins(2)	AVIN, PVIN, EN, VOS, PG	– 0.3	6.0	V
	MODE, SS/TR, SW	– 0.3	V_{IN}+0.3V	
	FB	– 0.3	3.0	
Sink current	PG	0	1.0	mA
Temperature	Operating Junction, T_J	-40	150	°C
	Storage, T_{stg}	– 65	150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human Body Model (HBM) ESD stress voltage(1)	±2000	V
		Charged Device Model (CDM) ESD stress voltage(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.5	6.0	V
V_{PG}	Pull-up resistor voltage	0	6.0	V
V_{OUT}	Output voltage range	0.8	V_{IN}	V
I_{OUT}	Output current range	0	2.0	A
T_J	Operating junction temperature	-40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS62097xx RWK (11 TERMINALS)	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953

7.5 Electrical Characteristics

T_J = -40°C to 125°C, and V_{IN} = 2.5V to 6.0V. Typical values are at T_J = 25°C and V_{IN} = 3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into AVIN, PVIN	EN = High, Device not switching, T_J = –40°C to 85°C		40	57	µA
		EN = High, Device not switching		40	65	
I_{SD}	Shutdown current into AVIN, PVIN	EN = Low, T_J = –40°C to 85°C		0.7	3	µA
		EN = Low		0.7	10	
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.2	2.3	2.4	V
		V_{IN} rising	2.3	2.4	2.5	
T_{JSD}	Thermal shutdown threshold	T_J rising		160		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE (EN, MODE)						
V_{H_EN}	High-level input voltage, EN pin		2.0	1.6		V
V_{L_EN}	Low-level input voltage, EN pin			1.3	1.0	V
$I_{EN,LKG}$	Input leakage current into EN pin	EN = High		0.01	0.9	µA
R_{PD}	Pull-down resistance at EN pin	EN = Low		375		kΩ
V_{H_MO}	High-level input voltage, MODE pin		1.2			V
V_{L_MO}	Low-level input voltage, MODE pin				0.4	V
$I_{MO,LKG}$	Input leakage current into MODE pin	MODE = High		0.01	0.16	µA
SOFT STARTUP, POWER GOOD (SS/TR, PG)						
I_{SS}	Soft startup current		5.5	7.5	9.5	µA
	Voltage tracking gain factor	V_{FB} / $V_{SS/TR}$		1		
V_{PG}	Power good threshold	V_{OUT} rising, referenced to V_{OUT} nominal	92	95	98	%
		V_{OUT} falling, referenced to V_{OUT} nominal	87	90	92	
$V_{PG,OL}$	Low-level output voltage, PG pin	I_{sink} = 1mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0V		0.01	1.6	µA
OUTPUT						
V_{OUT}	Output voltage accuracy TPS6209718, TPS6209733	PWM mode, No load	–1.0		1.0	%
		PSM mode(1)	–1.0		2.1	
V_{FB}	Feedback reference voltage	PWM mode	792	800	808	mV
		PSM mode(1)	792	800	817	
$I_{FB,LKG}$	Input leakage current into FB pin	V_{FB} = 0.8V		0.01	0.1	µA
R_{DIS}	Output discharge resistor	EN = Low, V_{OUT} = 1.8V		165		Ω
	Line regulation	I_{OUT} = 0.5A, V_{OUT} = 1.8V(1)		0.02		%/V
	Load regulation	PWM mode, V_{OUT} = 1.8V (1)		0.2		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance	I_{SW} = 500mA, V_{IN} = 5.0V		40	73	mΩ
		I_{SW} = 500mA, V_{IN} = 3.6V		50	96	
	Low-side FET on-resistance	I_{SW} = 500mA, V_{IN} = 5.0V		40	68	mΩ
		I_{SW} = 500mA, V_{IN} = 3.6V		50	85	
I_{LIMF}	High-side FET forward current limit		3.1	3.6	4.2	A
		V_{IN} = 5.0V	3.3	3.6	3.9	
I_{LIMN}	Low-side FET negative current limit	Forced PWM mode	–1.25	–1.1	-0.7	A

(1) Conditions: L = 1 µH, C_{OUT} = 22 µF, Switching Frequency = 2.0 MHz

7.6 Typical Characteristics

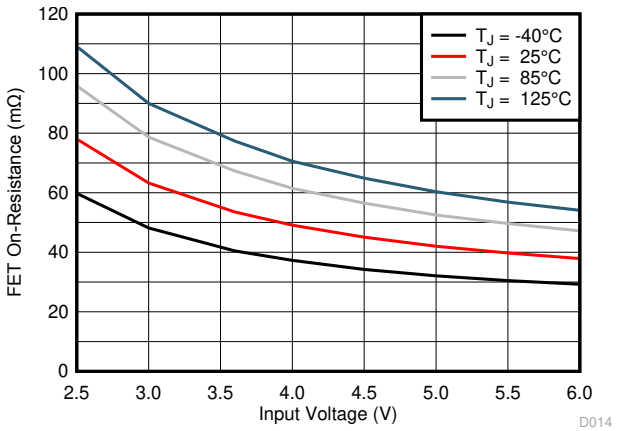


图 7-1. High-Side FET On-Resistance

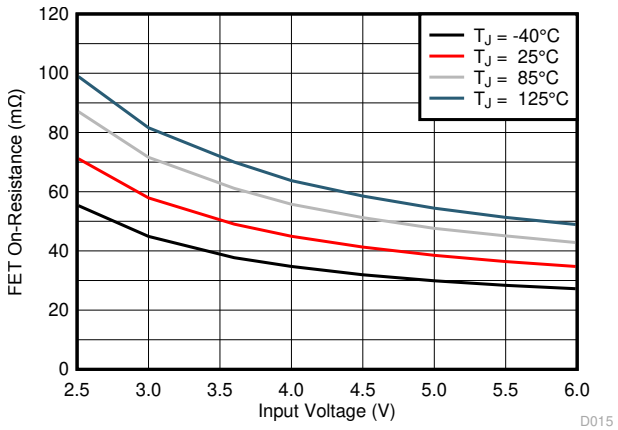


图 7-2. Low-Side FET On-Resistance

8 Detailed Description

8.1 Overview

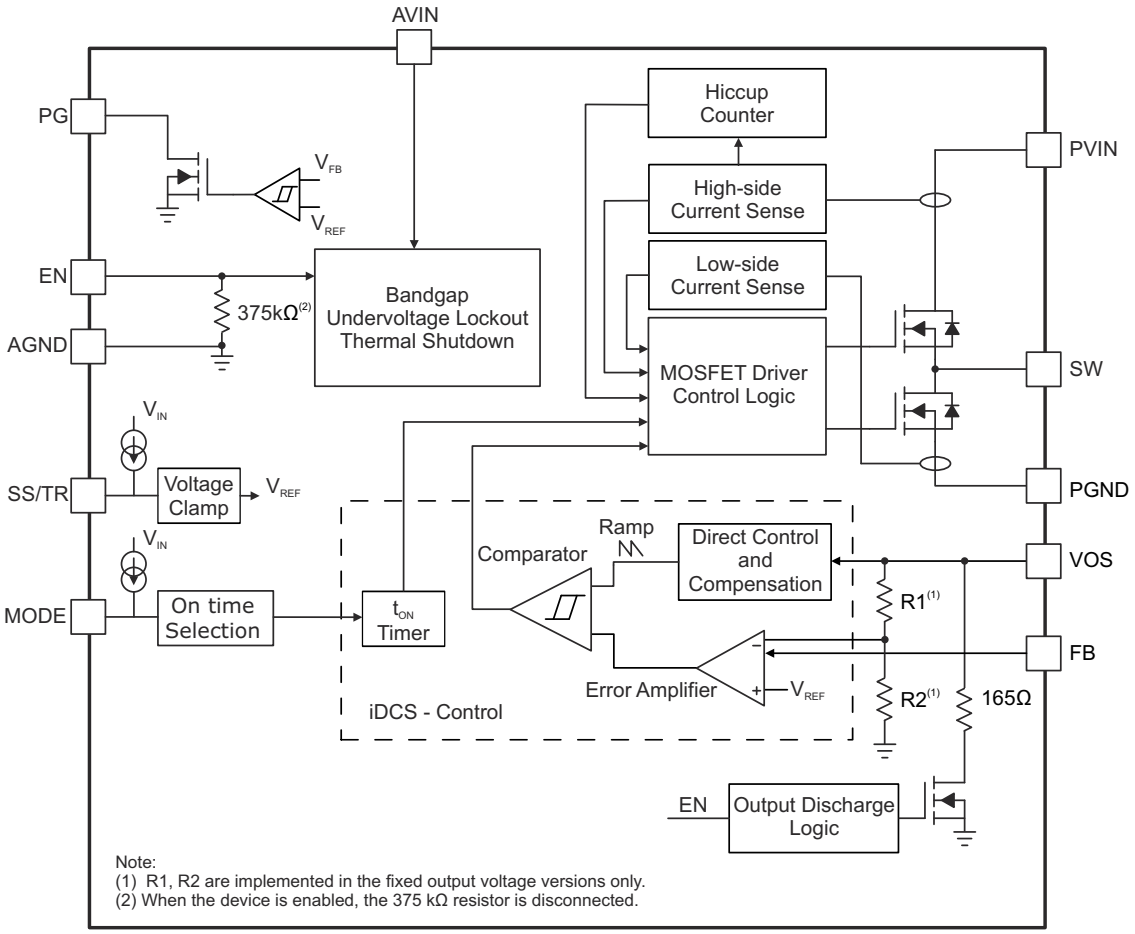
The TPS62097 synchronous step-down converter is based on the iDCS-Control (Industrial Direct Control with Seamless transition into Power Save Mode) topology. The control topology not only keeps the advantages of DCS-Control, but also provides other features:

- Forced PWM mode over the whole load range
- Selectable PWM switching frequency
- 1% output voltage accuracy
- Output voltage sequencing and tracking

The iDCS-Control topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode (PSM) at light load conditions. Or it forces the device in fixed frequency PWM mode only operation for the whole load range.

In PWM mode, the device operates with a predictive on-time switching pulse. A quasi-fixed switching frequency over the input and output voltage range is achieved by using an input and output voltage feedforward to set the on-time, as shown in 表 8-1. The converter enters Power Save Mode, reducing the switching frequency and minimizing current consumption, to achieve high efficiency over the entire load current range. Since iDCS-Control supports both operation modes within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 100% Duty Cycle Mode

The device offers a low input to output voltage dropout by entering 100% duty cycle mode when the input voltage reaches the level of the output voltage. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (1)$$

where

- $V_{IN(min)}$ = Minimum input voltage to maintain a minimum output voltage
- I_{OUT} = Output current
- $R_{DS(on)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

When the device operates close to 100% duty cycle mode, the TPS62097 cannot enter Power Save Mode regardless of the load current if the input voltage decreases to typically 15% above the output voltage. The device maintains output regulation in PWM mode.

8.3.2 Switch Current Limit and Hiccup Short Circuit Protection

The switch current limit prevents the devices from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition. If the inductor current reaches the threshold I_{LIMF}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Once this switch current limit is triggered 32 times, the devices stop switching and enable the output discharge. The devices then automatically start a new start-up after a typical delay time of 100 µs has passed. This is HICCUP short circuit protection and is implemented to reduce the current drawn during a short circuit condition. The devices repeat this mode until the high load condition disappears.

When the device is in forced PWM mode, the negative current limit of the low-side MOSFET is active. The negative current limit prevents excessive current from flowing back through the inductor to the input.

8.3.3 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is implemented, which shuts down the devices at voltages lower than V_{UVLO} with a hysteresis of 100 mV.

8.3.4 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds T_{JSD}. Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

8.4 Device Function Modes

8.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 0.7 µA.

In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 165 Ω discharges the output through the VOS pin smoothly. The output discharge function also works when thermal shutdown, undervoltage lockout, or HICCUP short circuit protection are triggered.

An internal pulldown resistor of 375 kΩ is connected to the EN pin when the EN pin is low. The pulldown resistor is disconnected when the EN pin is high.

8.4.2 Power Save Mode and Forced PWM Mode (MODE)

The MODE pin is a multi-functional pin that allows the device operation in forced PWM mode or PWM/PSM mode, and to select the PWM switching frequency.

Once the EN pin is pulled high, the IC enables internal circuit blocks and prepares to ramp the output up. The period between the rising edge of the EN pin and the beginning of the power stage switching is called the MODE detection time, typically 50 µs. During the MODE detection time period, shown in 图 8-1, the PWM switching frequency and operating mode are set by the MODE pin status, as shown in 表 8-1.

The PWM switching frequency cannot be changed after the detection time period. Only when the device is set in PWM/PSM mode during the MODE detection time period (MODE = AGND), it is possible to switch between PWM/PSM and forced PWM operation modes by toggling the MODE pin with a GPIO pin of a microcontroller, for example. The other four MODE pin selections force the device in PWM mode only.

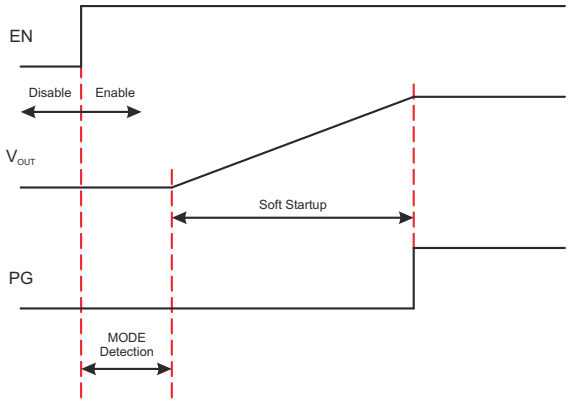


图 8-1. Power-up Sequence

表 8-1. Switching Frequency and Mode Selection

TYPICAL PWM SWITCHING FREQUENCY (MHZ)	RESISTANCE AT MODE PIN (E24 EIA VALUE)	TOGGLE MODE PIN AFTER MODE DETECTION	ON-TIME EQUATION	OPERATING MODE
1.50	8.2 kΩ ±5%	No	t_{ON} = 667 ns x V_{OUT} / V_{IN}	Forced PWM
1.75	18 kΩ ±5%	No	t_{ON} = 571 ns x V_{OUT} / V_{IN}	Forced PWM
2.00	AGND	Yes	t_{ON} = 500 ns x V_{OUT} / V_{IN}	PWM/PSM and Forced PWM
2.25	39 kΩ ±5%	No	t_{ON} = 444 ns x V_{OUT} / V_{IN}	Forced PWM
2.50	75 kΩ ±5% or Open	No	t_{ON} = 400 ns x V_{OUT} / V_{IN}	Forced PWM

Connecting the MODE pin to AGND with a resistor or leaving the MODE pin open forces the device into PWM mode for the whole load range. The device operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In forced PWM mode, the efficiency is lower than that of PSM at light load.

Connecting the MODE pin to the AGND pin enables Power Save Mode with an automatic transition between PWM and Power Save Mode. As the load current decreases and the inductor current becomes discontinuous, the device enters Power Save Mode operation automatically. In Power Save Mode, the switching frequency is reduced and estimated by 方程式 2. In Power Save Mode, the output voltage rises slightly above the nominal output voltage, as shown in Load Regulation, PWM/PSM Mode (2.0 MHz). This effect is minimized by increasing the output capacitor.

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (2)$$

When the device operates close to 100% duty cycle mode, the TPS62097 cannot enter Power Save Mode regardless of the load current if the input voltage decreases to typically 15% above the output voltage. The device maintains output regulation in PWM mode.

8.4.3 Soft Start-up (SS/TR)

The TPS62097 programs its output voltage ramp rate with the SS/TR pin. Connecting an external capacitor to SS/TR enables output soft start-up to reduce inrush current from the input supply. The device charges the capacitor voltage to the input supply voltage with a constant current of typically 7.5 μA. The FB pin voltage follows the SS/TR pin voltage until the internal reference voltage of 0.8 V is reached. The soft start-up time is calculated using 方程式 3. Keep the SS/TR pin floating to set the minimum start-up time.

$$t_{SS} = C_{SS/TR} \times \frac{0.8V}{7.5\mu A} \quad (3)$$

An active pulldown circuit is connected to the SS/TR pin. It discharges the external soft start-up capacitor in case of disable, UVLO, thermal shutdown, and HICCUP short circuit protection.

8.4.4 Voltage Tracking (SS/TR)

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 图 8-2. From 0 V to 0.8 V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.8 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.8 V. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in 图 8-3.

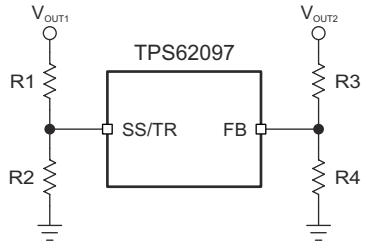


图 8-2. Output Voltage Tracking

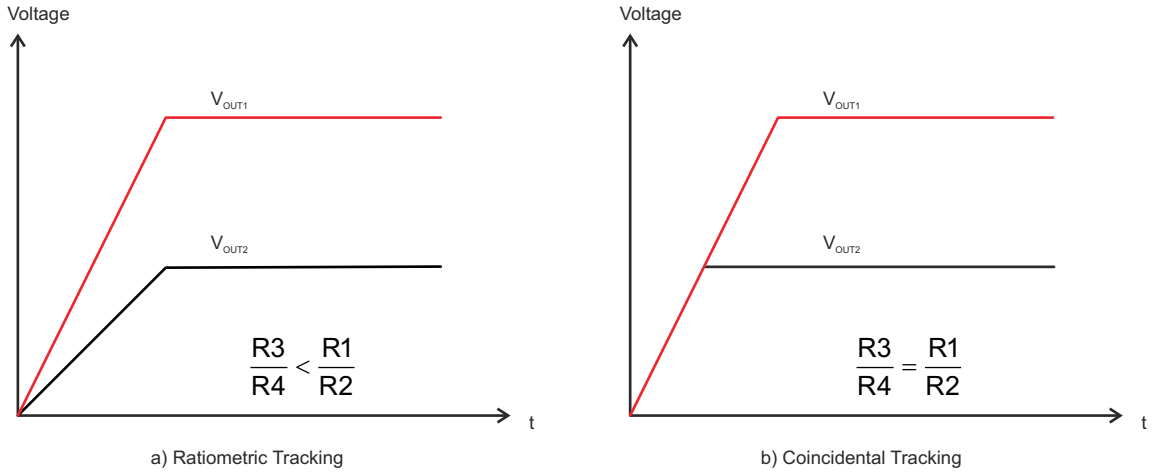


图 8-3. Voltage Tracking Options

The R2 value should be set properly to achieve accurate voltage tracking by taking 7.5 μA soft start-up current into account. 1 kΩ or smaller is a sufficient value for R2.

For decreasing SS/TR pin voltage, the device does not sink current from the output when the device is in PSM, so the resulting decreases of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN} + 0.3 V.

8.4.5 Power Good (PG)

The TPS62097 has a power-good output. The PG pin goes high impedance once the output voltage is above 95% of the nominal voltage and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connected to any voltage rail less than 6 V. The PG pin goes low when the device is disabled or in thermal shutdown. When the devices are in UVLO, the PG pin is high impedance.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when not used.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design of the TPS62097.

9.2 1.2-V Output Application

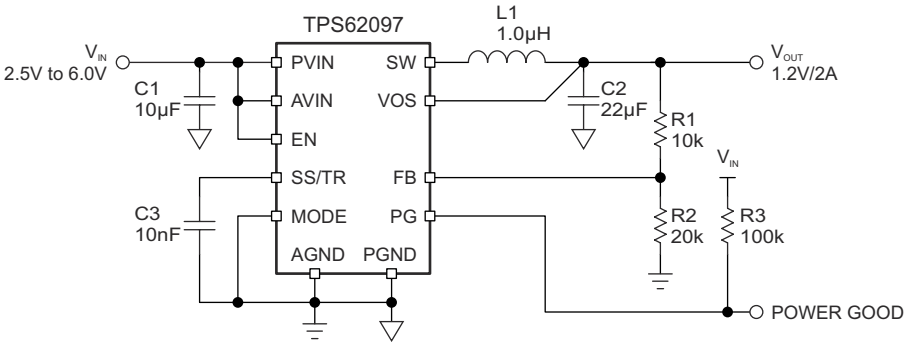


图 9-1. 1.2-V Output Application Schematic

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 6 V
Output voltage	1.2 V
Output current	2.0 A
Output voltage ripple	< 30 mV

表 9-2 lists the components used for the example.

表 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 µF, Ceramic Capacitor, 6.3 V, X7R, size 0805, C2012X7R0J106M125AB	TDK
C2	22 µF, Ceramic Capacitor, 6.3 V, X7S, size 0805, C2012X7S1A226M125AC	TDK
C3	10 nF, Ceramic Capacitor, 6.3 V, X7R, size 0603, GRM188R70J103KA01	Murata
L1	1 µH, Shielded, 5.4 A, XFL4020-102MEB	Coilcraft
R1	Depending on the output voltage, 1% accuracy	Std
R2	20 kΩ, 1% accuracy	Std
R3	100 Ωk, 1% accuracy	Std

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to 方程式 4:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (4)$$

R2 should not be higher than 20 kΩ to reduce noise coupling into the FB pin and improve the output voltage regulation. 图 9-1 shows the external resistor divider value for 1.2-V output. Choose additional resistor values for other outputs. A feedforward capacitor is not required.

The fixed output voltage versions, TPS6209718 and TPS6209733, do not need the external resistor divider. TI recommends to connect the FB pin to AGND for improved thermal performance.

9.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify the selection process, 表 9-3 outlines possible inductor and capacitor value combinations for most applications.

表 9-3. Output Capacitor / Inductor Combinations

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)				
	10	22	47	100	150
0.47					
1		+(1)	+	+	+
2.2					

(1) Typical application configuration. Other '+' mark indicates recommended filter combinations. Other values may be acceptable in applications but should be fully tested by the user. Refer to the application note SLVA710.
(2) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%. The required effective inductance is 500-nH minimum.
(3) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and -50%.

9.2.2.3 Inductor Selection

The main parameters for the inductor selection are the inductor value and the saturation current. To calculate the maximum inductor current under static load conditions, 方程式 5 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (5)$$

Where:

$I_{OUT,MAX}$ = Maximum output current
ΔI_L = Inductor current ripple
f_{SW} = Switching frequency
L = Inductor value

TI recommends to choose the saturation current for the inductor 20% to 30% higher than the $I_{L,MAX}$, out of 方程式 5. A higher inductor value is also useful to lower ripple current but increases the transient response time as well. The following inductors are recommended to be used in designs.

表 9-4. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS L x W x H [mm³]	DC RESISTANCE [mΩ TYP]	PART NUMBER(1)
1	5.4	4.0x4.0x2.0	11	COILCRAFT XFL4020-102ME
1	5.3	2.5x2.0x1.2	33	TOKO DFE252012F-1R0M
1	3.4	2.0x1.2x1.0	62	TOKO DFE201210S-1R0M
1	5.1	3.0x3.0x1.2	43	TAIYO YUDEN MDMK3030T1R0MM
1	4.2	2.5x2.0x1.2	43	CYNTEC SDEM25201B-1R0MS-79
1	2.6	2.5x2.0x1.2	48	Murata LQH2HPN1R0NJR
1	6.6	3.0x3.0x1.2	42	Wurth Electronics 74438334010

(1) See *Third-Party Products Disclaimer*

9.2.2.4 Capacitor Selection

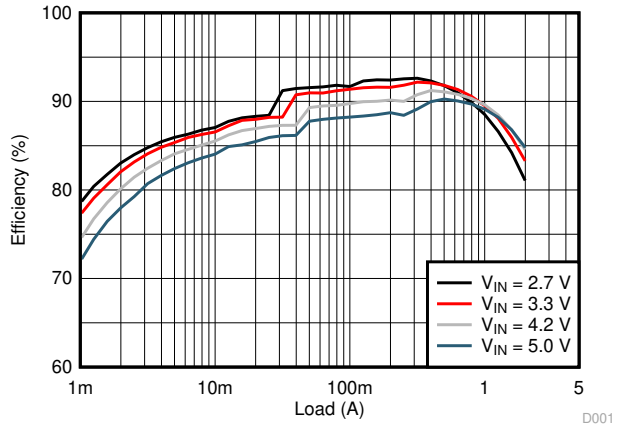
The input capacitor is the low impedance energy source for the converters which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is required for best filtering and should be placed between PVIN and PGND as close as possible to those pins. For most applications, a 10-µF capacitor is sufficient, though a larger value reduces input current ripple.

The architecture of the TPS62097 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectrics. The recommended typical output capacitor value is 22 µF and can vary over a wide range as outlined in 表 9-4.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. Ensure that the input effective capacitance is at least 5 µF and the output effective capacitance is at least 10 µF.

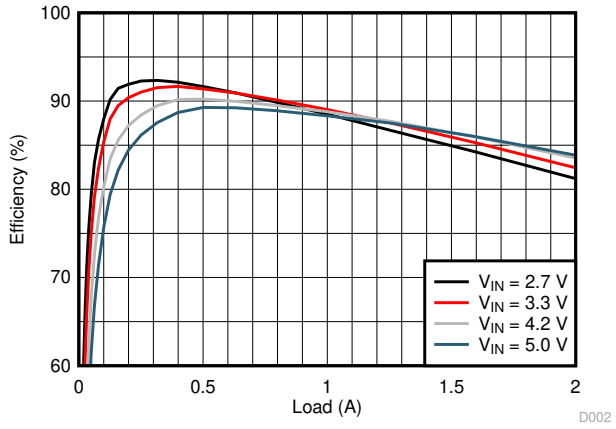
9.2.3 Application Performance Curves

T_A = 25°C, V_{IN} = 3.6 V, unless otherwise noted.



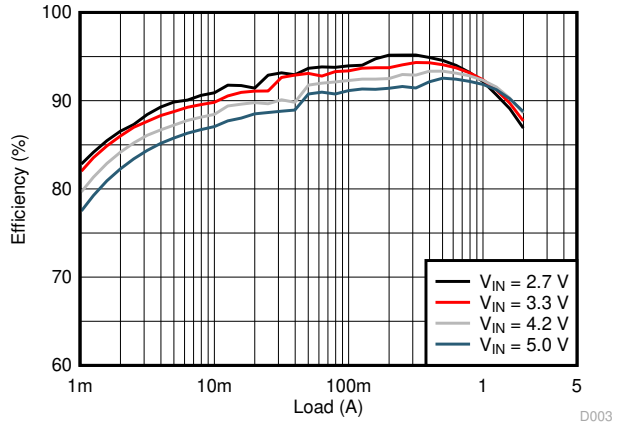
V_{OUT} = 1.2 V

图 9-2. Efficiency, PWM/PSM Mode (2.0 MHz)



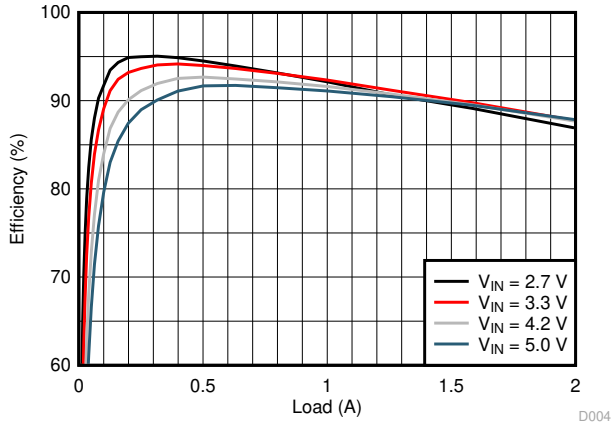
V_{OUT} = 1.2 V

图 9-3. Efficiency, Forced PWM Mode (2.0 MHz)



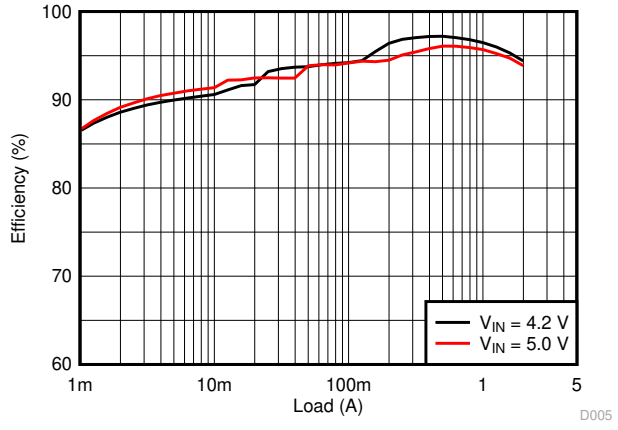
V_{OUT} = 1.8 V

图 9-4. Efficiency, PWM/PSM Mode (2.0 MHz)



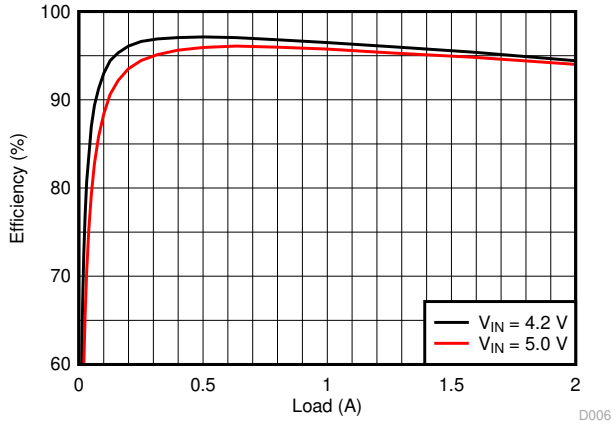
V_{OUT} = 1.8 V

图 9-5. Efficiency, Forced PWM Mode (2.0 MHz)



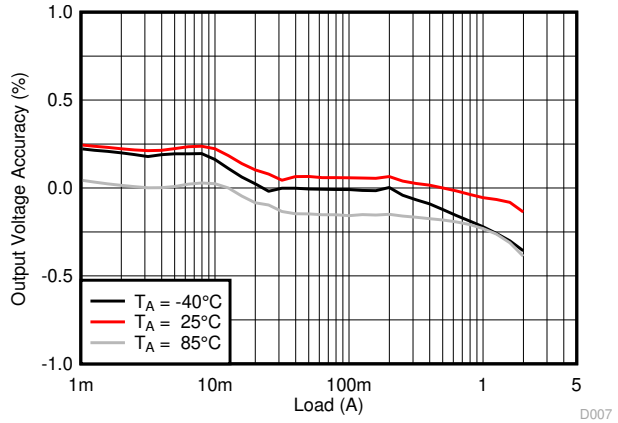
V_{OUT} = 3.3 V

图 9-6. Efficiency, PWM/PSM Mode (2.0 MHz)



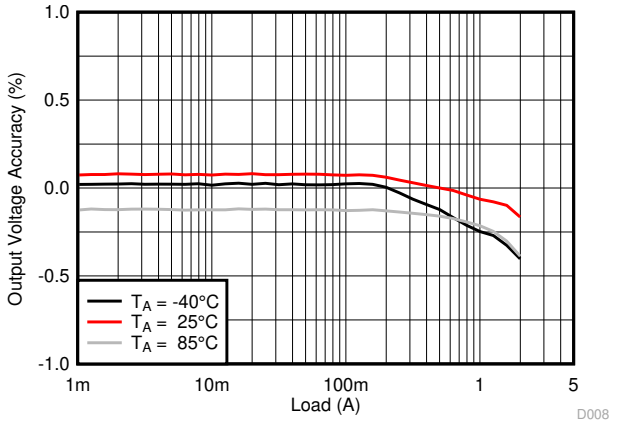
V_{OUT} = 3.3 V

图 9-7. Efficiency, Forced PWM Mode (2.0 MHz)



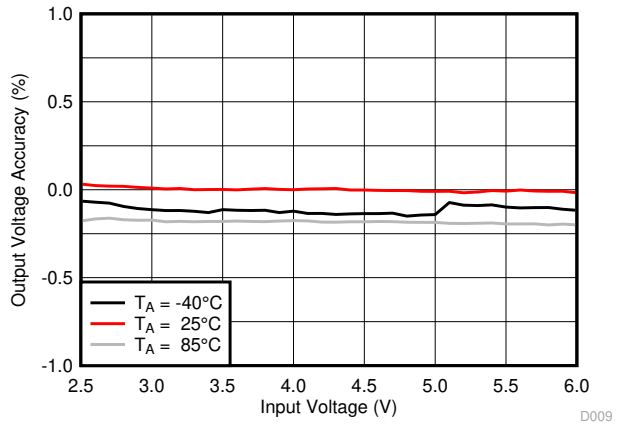
V_{OUT} = 1.2 V

图 9-8. Load Regulation, PWM/PSM Mode (2.0 MHz)



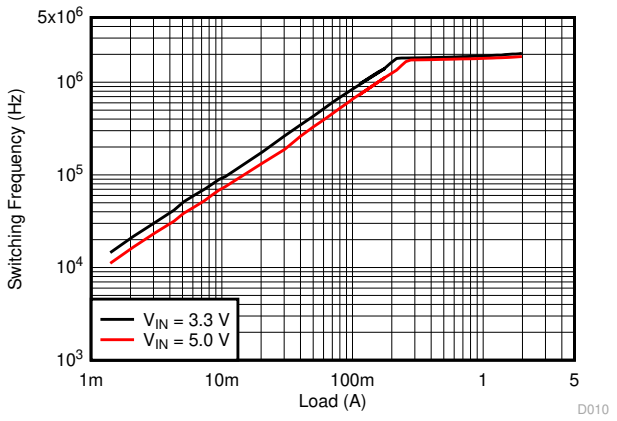
V_{OUT} = 1.2 V

图 9-9. Load Regulation, Forced PWM Mode (2.0 MHz)



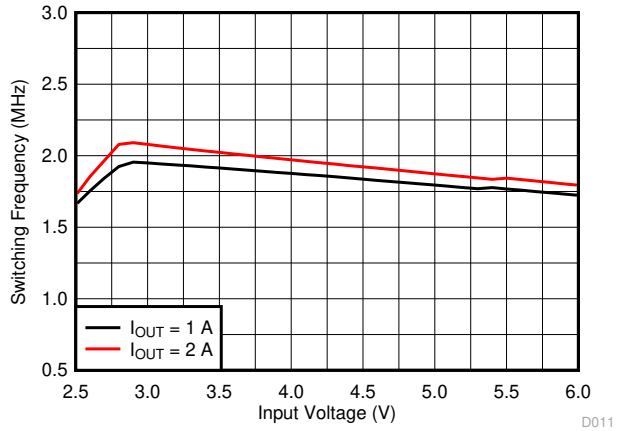
V_{OUT} = 1.2 V I_{OUT} = 500 mA

图 9-10. Line Regulation, Forced PWM Mode (2.0 MHz)



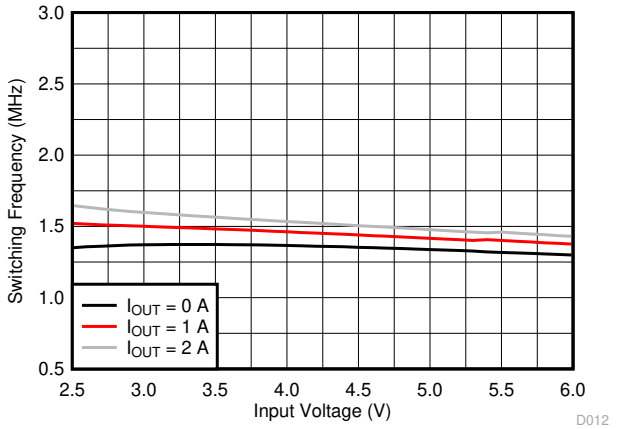
V_{OUT} = 1.2 V MODE = AGND

图 9-11. Switching Frequency, PWM/PSM Mode (2.0 MHz)



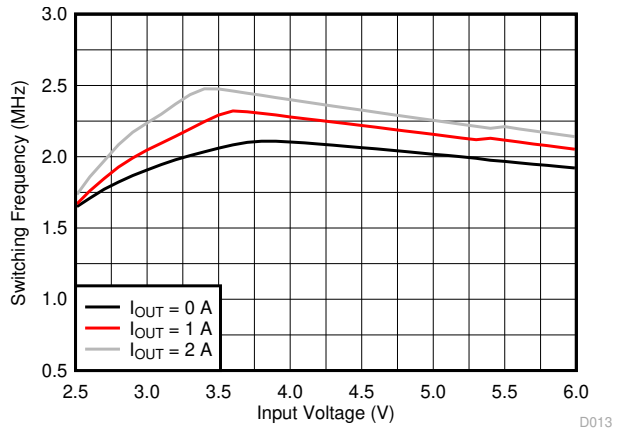
V_{OUT} = 1.2 V MODE = High after PWM/PSM Selection

图 9-12. Switching Frequency, Forced PWM Mode (2.0 MHz)



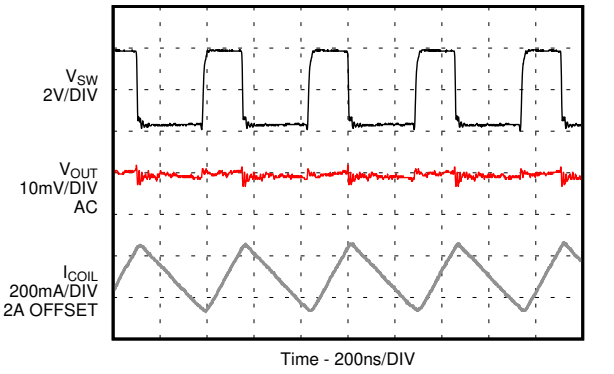
V_{OUT} = 1.2 V R_{Mode} = 8.2 kΩ

图 9-13. Switching Frequency, Forced PWM Mode (1.5 MHz)



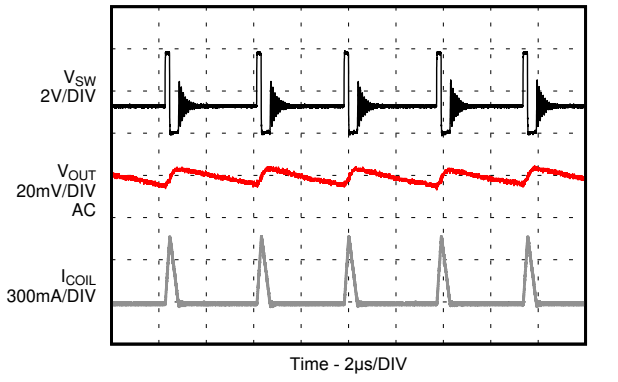
V_{OUT} = 1.2 V MODE = Open

图 9-14. Switching Frequency, Forced PWM Mode (2.5 MHz)



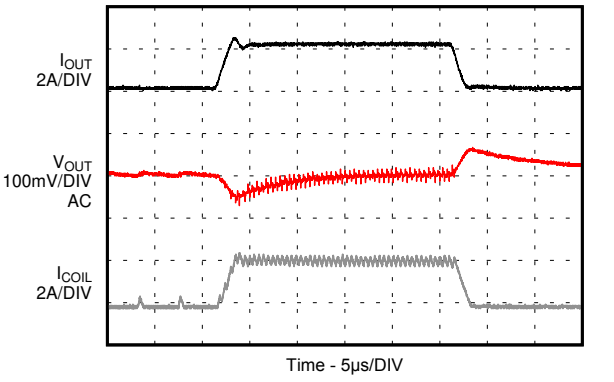
V_{OUT} = 1.2 V I_{OUT} = 2 A

图 9-15. Output Ripple, PWM Operation (2.0 MHz)



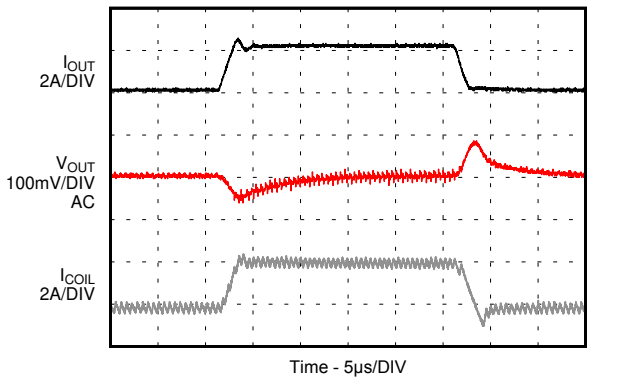
V_{OUT} = 1.2 V I_{OUT} = 30 mA

图 9-16. Output Ripple, Power Save Operation



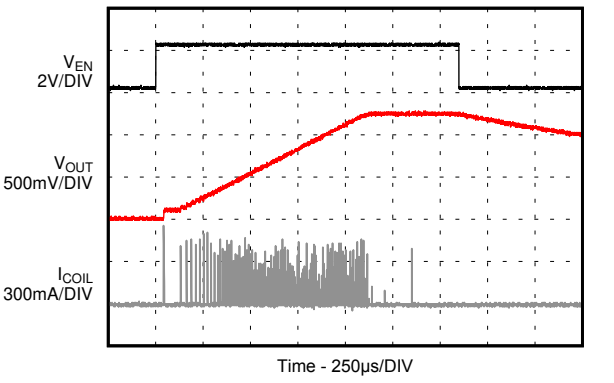
V_{OUT} = 1.2 V I_{OUT} = 0 A to 2 A, 1 A / µs

图 9-17. Load Transient, PWM/PSM Mode (2.0 MHz)



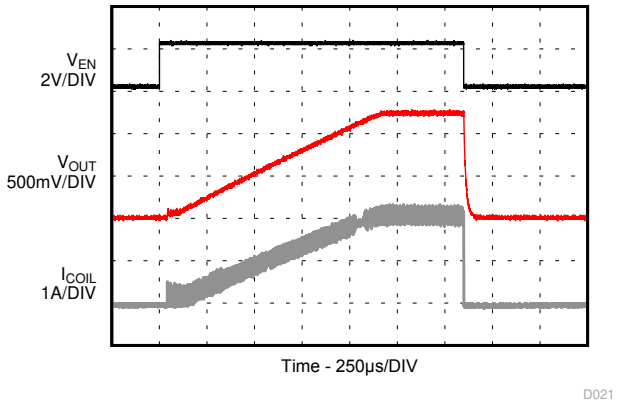
V_{OUT} = 1.2 V I_{OUT} = 0 A to 2 A, 1 A / µs

图 9-18. Load Transient, Forced PWM Mode (2.0 MHz)



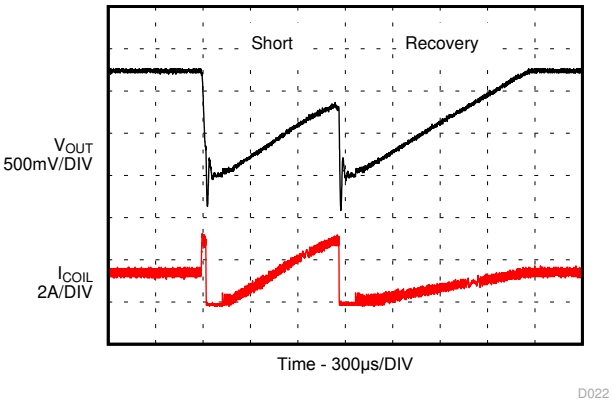
V_{OUT} = 1.2 V R_{OUT} = No Load

图 9-19. Startup and Shutdown without Load



V_{OUT} = 1.2 V R_{OUT} = 0.6 Ω (2 A)

图 9-20. Startup and Shutdown with Load



V_{OUT} = 1.2 V R_{OUT} = 0.8 Ω (1.5 A) with 1-ms short

图 9-21. Short Circuit Protection, HICCUP

9.2.4 Coincidental Voltage Tracking

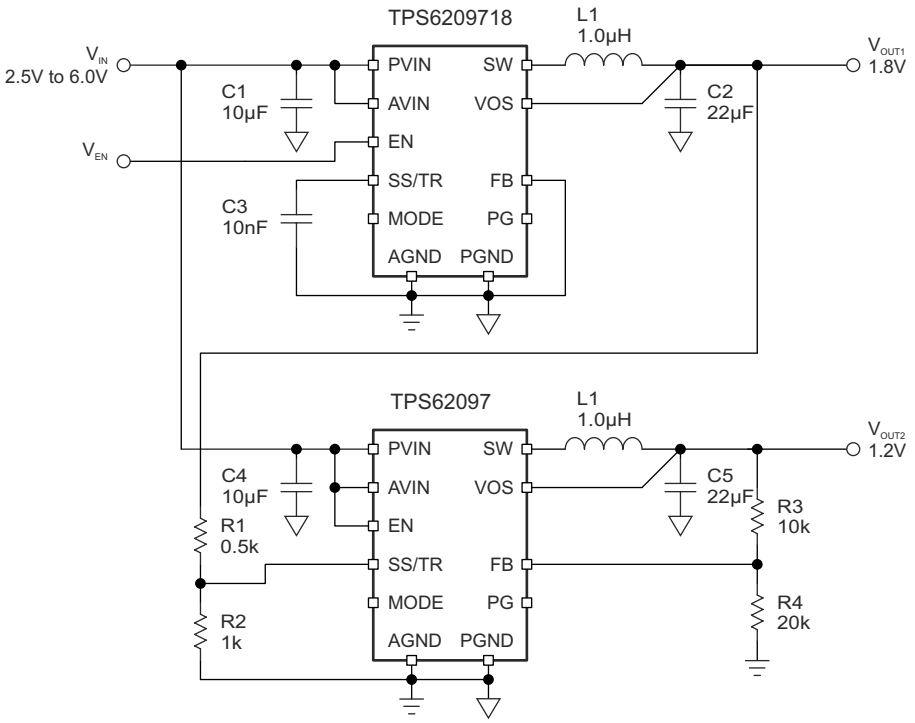


图 9-22. 1.8-V and 1.2-V Coincidental Voltage Tracking Schematic

9.2.4.1 Design Requirements

For this design example, use the following as the input parameters.

表 9-5. Design Parameters

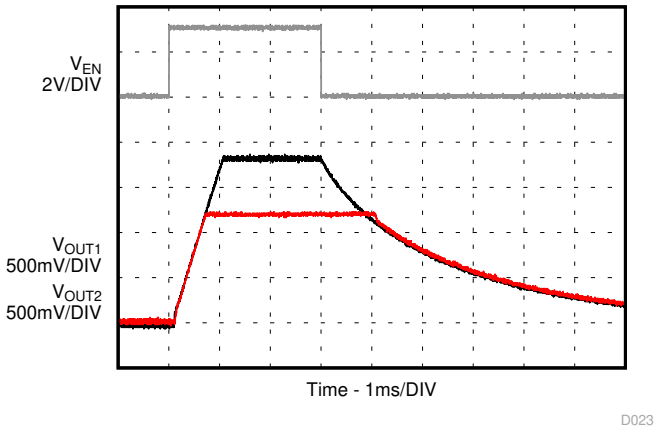
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 6 V
Output voltage 1	1.8 V
Output voltage 2	1.2 V
Output voltage 2 follows output voltage 1 coincidentally.	

9.2.4.2 Detailed Design Procedure

Set 1 kΩ for R2 and 0.5 kΩ for R1. Connect the two converters as shown in 图 9-22. Set up two converters in forced PWM mode.

9.2.4.3 Application Performance Curve

T_A = 25°C, V_{IN} = 5.0 V, unless otherwise noted.



V_{OUT1} = 1.8 V V_{OUT2} = 1.2 V

图 9-23. Coincidental Tracking Waveform

9.2.5 Switching Frequency Selection

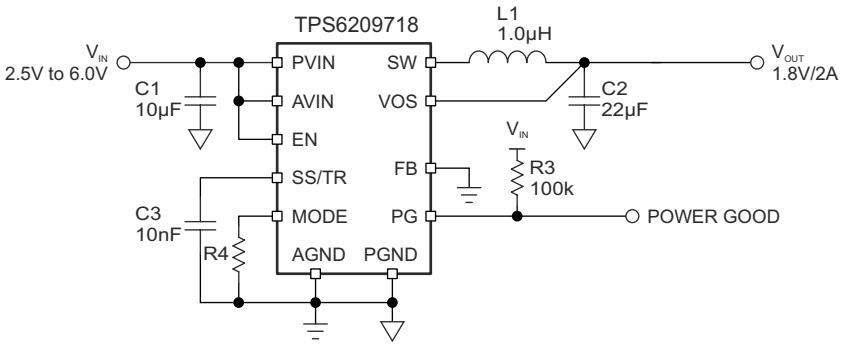


图 9-24. Switching Frequency Selection by an External Resistor

9.2.5.1 Design Requirements

For this design example, use the following as the input parameters.

表 9-6. Design Parameters

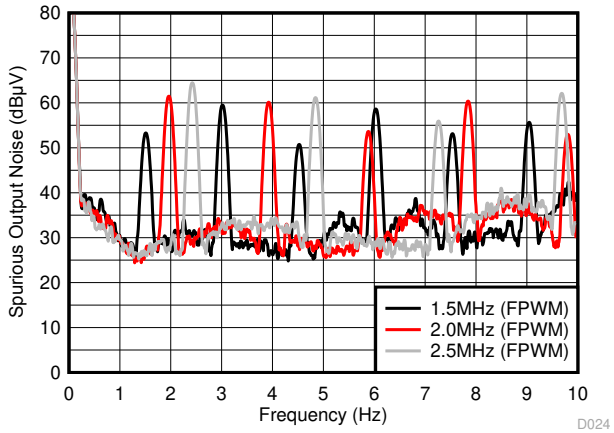
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 6 V
Output voltage 1	1.8 V
Switching Frequency Selection	1.5 MHz, 2.0 MHz, or 2.5 MHz

9.2.5.2 Detailed Design Procedure

Set 8.2 kΩ and 75 kΩ for 1.5-MHz, 2.0-MHz, and 2.5-MHz switching frequency. R4 uses the standard E24 series resistor values.

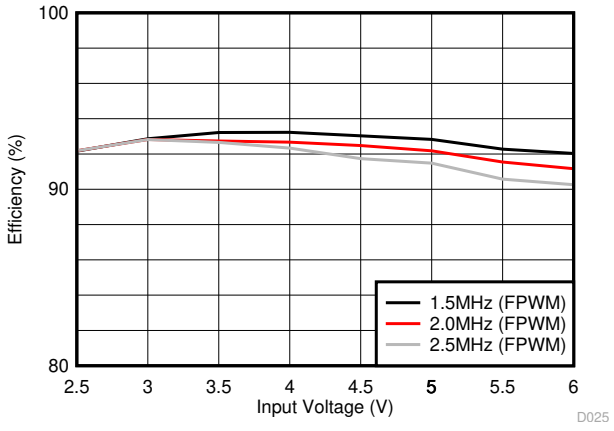
9.2.5.3 Application Performance Curves

T_A = 25°C, V_{IN} = 5.0, unless otherwise noted.



V_{OUT} = 1.8 V I_{OUT} = 1 A

图 9-25. Spurious Output Noise with Different Switching Frequency



V_{OUT} = 1.8 V I_{OUT} = 1 A

图 9-26. Efficiency with Different Switching Frequency

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.5 V and 6 V. The average input current of the TPS62097 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (6)$$

Ensure that a power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

- TI recommends to place all components as close as possible to the IC. Specifically, the input capacitor placement must be closest to the PVIN and PGND pins of the device.
- The low side of the input and output capacitors must be connected directly to the PGND pin to avoid a ground potential shift.
- Use the terminal of the input capacitor as the common node for AVIN and PVIN, AGND, and PGND. It helps reduce the noise coupling into the internal analog circuit blocks. Do not use a solid plane pour to connect these nodes.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- The sense trace connected to VOS pin is a signal trace. Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. Keep the trace away from SW nodes.
- Refer to the 图 11-1 for an example of component placement, routing, and thermal design.

11.2 Layout Example

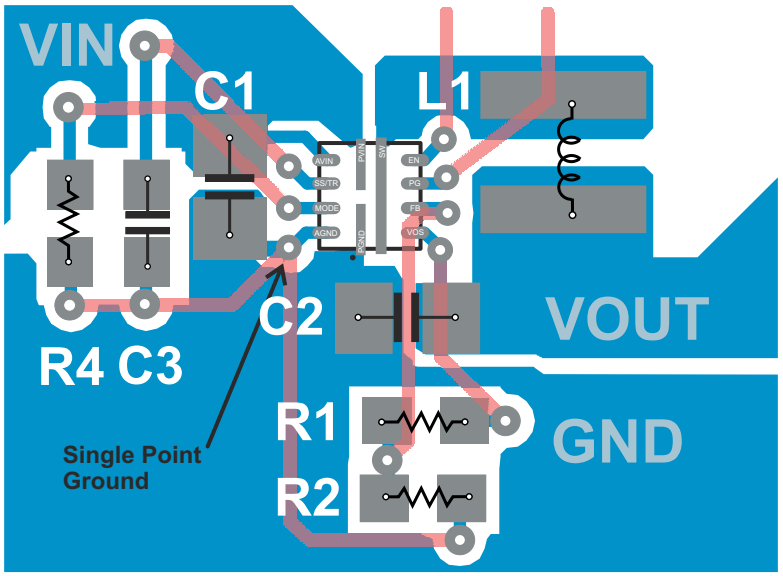


图 11-1. TPS62097 PCB Layout

11.2.1 Thermal Information

Implementation of integrated circuits in low-profile and fine pitch surface mount packages typically requires special attention to power dissipation. Many system dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

节 7.4 provides the thermal metric of the device on the TPS62097 EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB board improve the thermal performance of the device. For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6209718RWKR	ACTIVE	VQFN-HR	RWK	11	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGB5	Samples
TPS6209718RWKT	ACTIVE	VQFN-HR	RWK	11	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGB5	Samples
TPS6209733RWKR	ACTIVE	VQFN-HR	RWK	11	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGC5	Samples
TPS6209733RWKT	ACTIVE	VQFN-HR	RWK	11	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGC5	Samples
TPS62097RWKR	ACTIVE	VQFN-HR	RWK	11	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZFZ5	Samples
TPS62097RWKT	ACTIVE	VQFN-HR	RWK	11	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZFZ5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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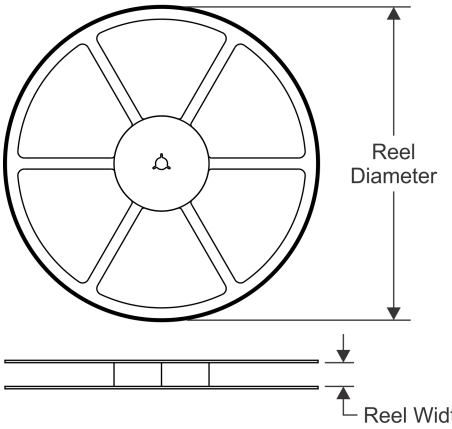
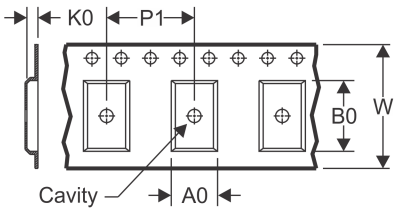
TAPE AND REEL INFORMATION

REEL DIMENSIONS

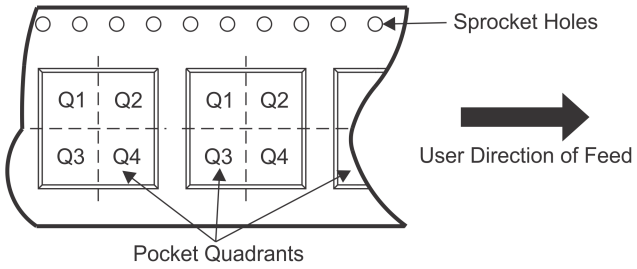


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

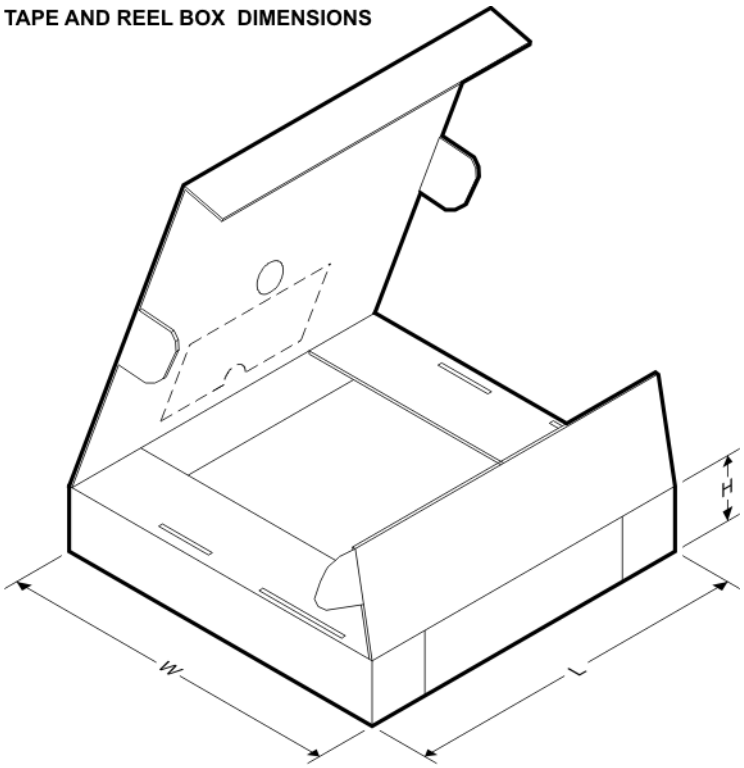
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6209718RWKR	VQFN-HR	RWK	11	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS6209718RWKT	VQFN-HR	RWK	11	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS6209733RWKR	VQFN-HR	RWK	11	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS6209733RWKT	VQFN-HR	RWK	11	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62097RWKR	VQFN-HR	RWK	11	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62097RWKT	VQFN-HR	RWK	11	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

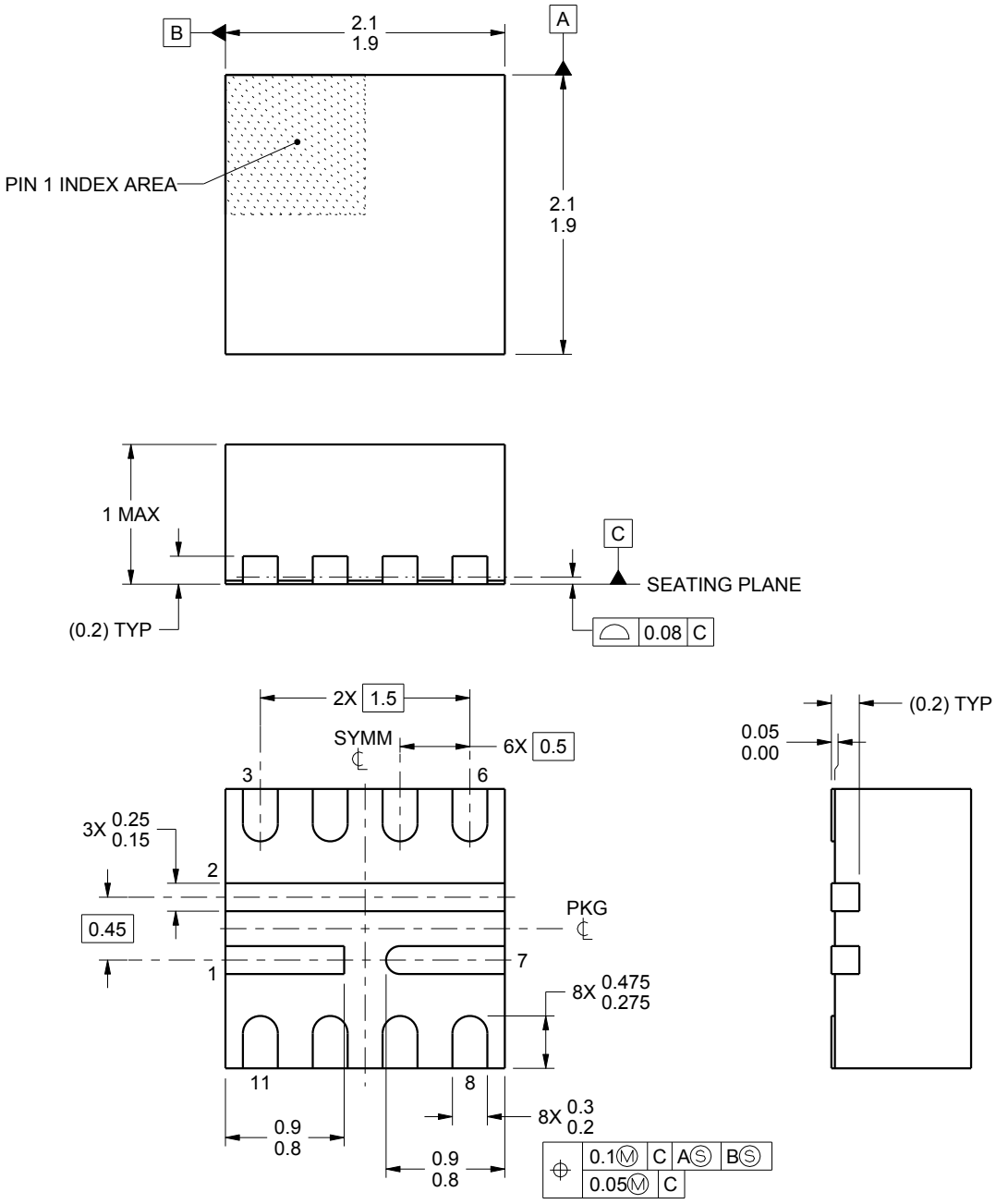
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6209718RWKR	VQFN-HR	RWK	11	3000	182.0	182.0	20.0
TPS6209718RWKT	VQFN-HR	RWK	11	250	182.0	182.0	20.0
TPS6209733RWKR	VQFN-HR	RWK	11	3000	182.0	182.0	20.0
TPS6209733RWKT	VQFN-HR	RWK	11	250	182.0	182.0	20.0
TPS62097RWKR	VQFN-HR	RWK	11	3000	182.0	182.0	20.0
TPS62097RWKT	VQFN-HR	RWK	11	250	182.0	182.0	20.0

PACKAGE OUTLINE

RWK0011B

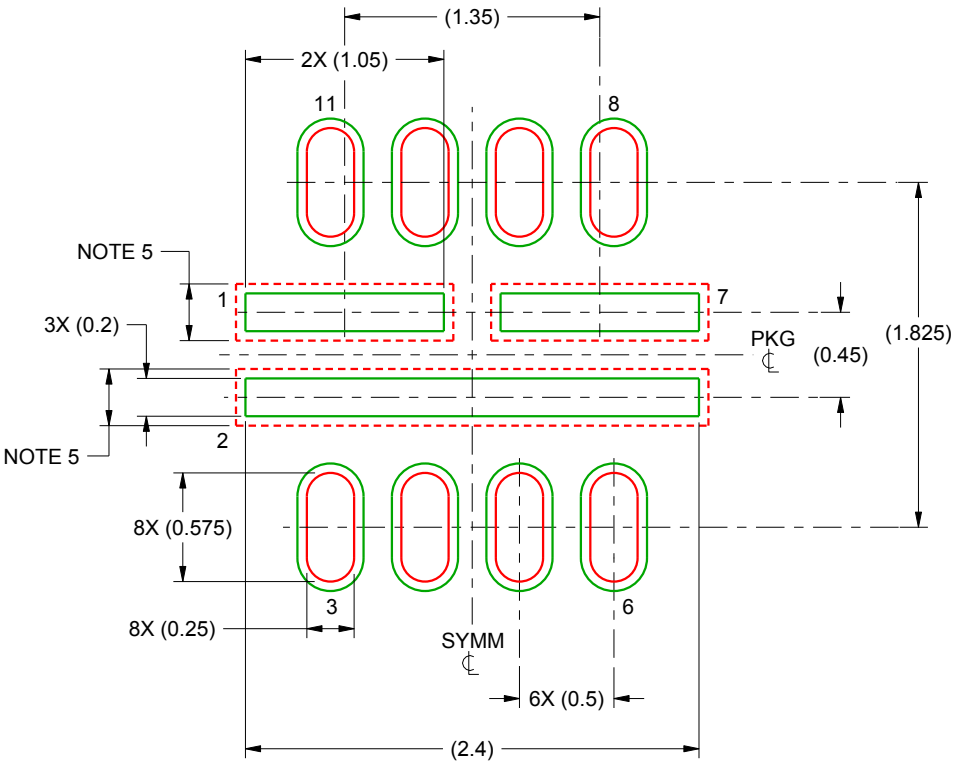
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

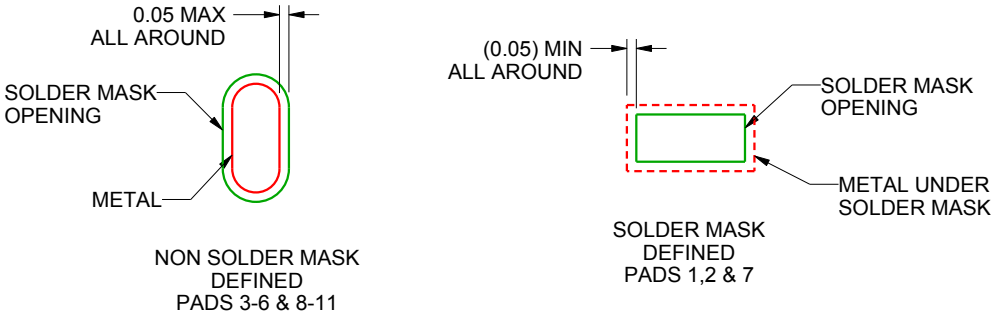


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Package pin numbers 1, 2, and 7 must be soldered to the printed circuit board for thermal and mechanical performance. Refer to product data sheet for specific thermal pad and via recommendations.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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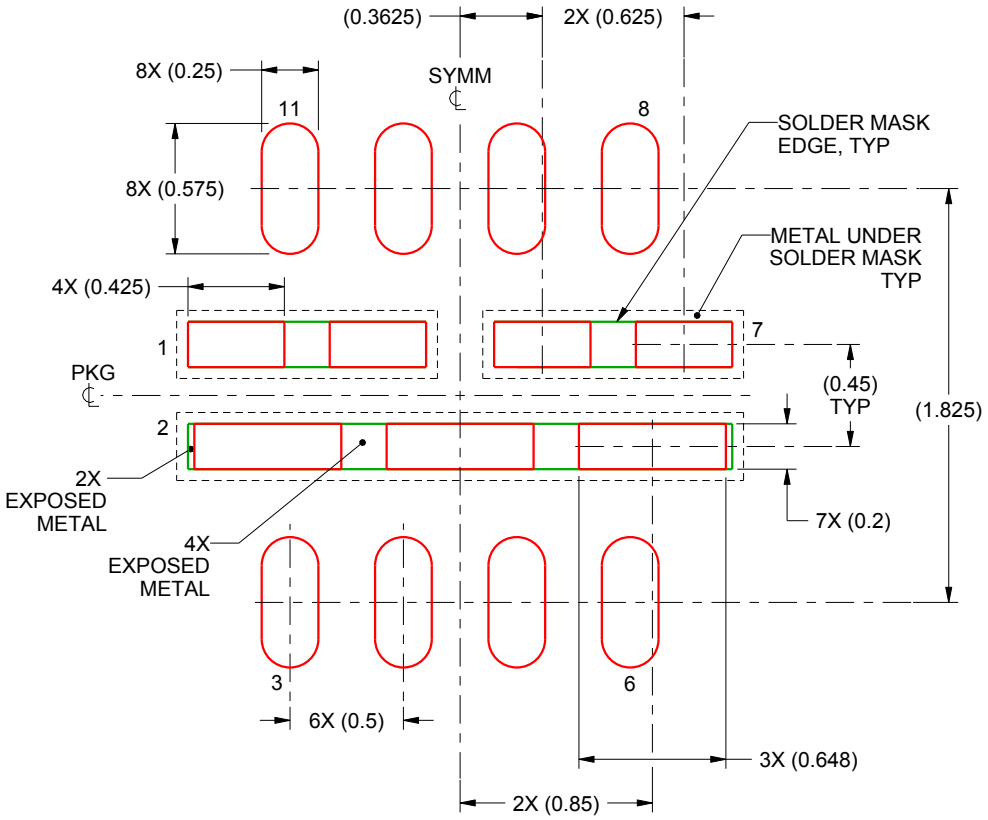
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Size of metal pad may vary due to creepage requirements.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2 & 7
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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