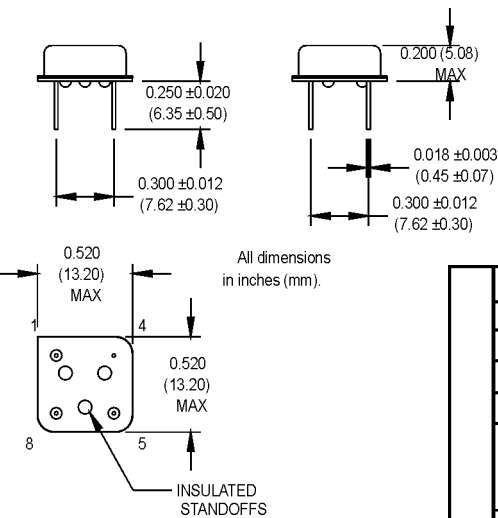


MVH Series

8 pin DIP, 5.0 Volt, HCMOS/TTL, VCXO



- General purpose VCXO for Phase Lock Loops (PLL), Clock Recovery, Reference Signal Tracking and Synthesizers
- Frequencies up to 50 MHz and tri-state option



Pin Connections

PIN	FUNCTION
1	Control Voltage
4	Circuit/Case Ground
5	Output
8	+Vdd

Ordering Information

Product Series	MVH	1	3	V	2	C	D	-R	00.0000	MHz
Temperature Range	1: 0°C to +70°C		2: -40°C to +85°C							
Stability	1: ±1000 ppm		2: ±500 ppm		3: ±100 ppm					
	4: ±50 ppm		5: ±35 ppm		6: ±25 ppm					
	8: ±20 ppm (Contact factory for availability)									
Output Type	V: Voltage Controlled									
Pull Range (Vc = .5 to 4.5 V)	1: ±50 ppm min.		2: ±100 ppm min.							
Symmetry/Logic Compatibility	A: 40/60 CMOS/TTL		C: 45/55 HCMOS							
Package/Lead Configurations	D: DIP; Nickel Header		G: Gull Wing; Nickel Header							
RoHS Compliance	Blank: non-RoHS compliant part -R: RoHS compliant part									
Frequency (customer specified)										

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	3		50	MHz	See Note 1	
Operating Temperature	T _A	(See Ordering Information)					
Storage Temperature	T _s	-55		+125	°C		
Frequency Stability	ΔF/F	(See Ordering Information)					
Aging							
1st Year		-3		+3	ppm		
Thereafter (per year)		-1		+1	ppm		
Pullability/APR		(See Ordering Information)					Over control voltage
Control Voltage	V _c	0.5	2.5	4.5	V		
Linearity				10	%	Positive Monotonic Slope	
Modulation Bandwidth	f _m	10			kHz		
Input Impedance	Z _{in}	50k			Ohms		
Input Voltage	V _{dd}	4.75	5.0	5.25	V		
Input Current	I _{dd}			35	mA		
Output Type						HCMOS/TTL	
Load		10 TTL or 50 pF				See Note 2	
Symmetry (Duty Cycle)		(See Ordering Information)					See Note 3
Logic "1" Level	V _{oh}	90% V _{dd}			V	HCMOS load	
		V _{dd} - 0.5			V	TTL load	
Logic "0" Level	V _{ol}			10% V _{dd}	V	HCMOS load	
				0.5	V	TTL load	
Rise/Fall Time	Tr/Tf			10	ns	See Note 4	
Start up Time			5		ms		
Phase Jitter	φ _J						
@ 19.44 MHz			0.4	1.0	ps RMS	Integrated 12 kHz - 20 MHz	
@ 38.88 MHz			0.2	0.5	ps RMS	Integrated 12 kHz - 20 MHz	
Phase Noise (Typical)						Offset from carrier	
@ 19.44 MHz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	dBc/Hz	
@ 38.88 MHz	-73	-106	-137	-152	-159	dBc/Hz	
	-71	-102	-135	-154	-161	dBc/Hz	

1. Higher frequencies available. Contact factory.
2. TTL load - see load circuit diagram #1. HCMOS load - see load circuit diagram #2.
3. Symmetry is measured at 1.4 V with TTL load, and at 50% with HCMOS load.
4. Rise/Fall times are measured between 0.5 V and 2.4 V for TTL load, and between 10% V_{dd} and 90% V_{dd} for HCMOS load.

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