Data Sheet | December 14, 2007 | FN9263.1

Boost + V_{ON} Slice + V_{COM}

The ISL97645 represents an integrated DC/DC regulator for monitor and notebook applications with screen sizes up to 20”. The device integrates a boost converter for generating A_{VDD}, a V_{ON} slice circuit, and a high performance V_{COM} amplifier.

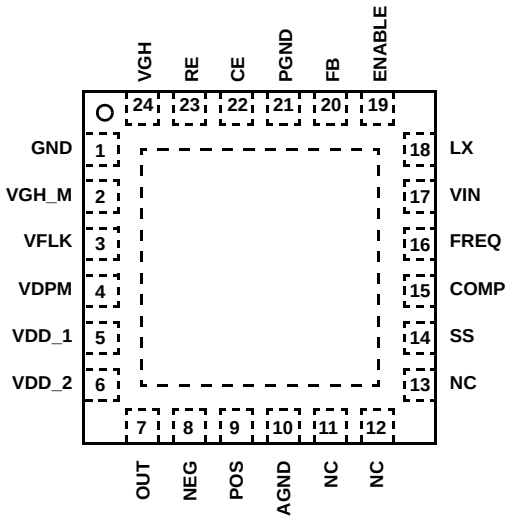
The boost converter features a 2.6A FET and has user programmable soft-start and compensation. With efficiencies up to 92%, the A_{VDD} is user selectable from 7V to 20V.

The V_{ON} slice circuit can control gate voltages up to 30V. High and low levels are programmable, as well as discharge rate and timing.

The integrated V_{COM} features high speed and drive capability. With 30MHz bandwidth and 50V/µs slew rate, the V_{COM} amplifier is capable of driving 400mA peaks, and 100mA continuous output current.

Pinout

ISL97645
(24 LD 4x4 QFN)
TOP VIEW



Features

- 2.7V to 5.5V Input
- 2.6A Integrated Boost for Up to 20V A_{VDD}
- Integrated V_{ON} Slice
- 600kHz/1.2MHz f_S
- V_{COM} Amplifier
  - 30MHz BW
  - 50V/µs SR
  - 400mA Peak Output Current
- UV and OT Protection
- 24 Ld 4x4 QFN
- Pb-Free (RoHS Compliant)

Applications

- LCD Monitors (15”+)
- Notebook Display (up to 16”)

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97645IRZ	97645IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4D
ISL97645IRZ-T*	97645IRZ	-40 to +85	24 Ld 4x4 QFN 6k pc Tape & Reel	L24.4x4D
ISL97645IRZ-TK*	97645IRZ	-40 to +85	24 Ld 4x4 QFN 1k pc Tape & Reel	L24.4x4D

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1	GND	Ground
2	VGH_M	Gate Pulse Modulation Output
3	VFLK	Gate Pulse Modulation Control Input
4	VDPM	Gate Pulse Modulation Enable
5	VDD_1	Gate Pulse Modulation Lower Voltage Input
6	VDD_2	V_{COM} Amplifier Supply
7	OUT	V_{COM} Amplifier Output
8	NEG	V_{COM} Amplifier Inverting Input
9	POS	V_{COM} Amplifier Noninverting Input
10	AGND	V_{COM} Amplifier Ground
11	NC	
12	NC	
13	NC	
14	SS	Boost Converter Soft-start. Connect a capacitor between this pin and GND to set the soft-start time.
15	COMP	Boost Converter Compensation Pin. Connect a series resistor and capacitor between this pin and GND to optimize transient response.
16	FREQ	Boost Converter Frequency Select.
17	VIN	Boost Converter Power Supply
18	LX	Boost Converter Switching Node
19	ENABLE	Chip Enable Pin. Connect to Vin for normal operation, GND for shutdown.
20	FB	Boost Converter Feedback
21	PGND	Boost Converter Power Ground
22	CE	Gate Pulse Modulator Delay Control. Connect a capacitor between this pin and GND to set the delay time.
23	RE	Gate Pulse Modulator Slew Control. Connect a resistor between this pin and GND to set the falling slew rate.
24	VGH	Gate Pulse Modulator High Voltage Input

Absolute Maximum Ratings

Lx to GND, AGND and PGND . . . . . -0.5 to +25V
VDD2, OUT, NEG and POS
to GND, AGND and PGND. . . . . -0.5 to +25V
VDD1, VGH and VGH_M
to GND, AGND and PGND. . . . . -0.5 to +32V
Differential Voltage Between POS and NEG . . . . . ±6V
Voltage Between GND, AGND and PGND . . . . . ±0.5V
All Other Pins to GND, AGND and PGND . . . . . -0.5 to +6.5V
Input, Output, or I/O Voltage . . . . . GND -0.3V to VIN + 0.3V

Recommended Operating Conditions

Input Voltage Range, VS . . . . . 2.7V to 5.5V
Boost Output Voltage Range, AVDD . . . . . 8V to 20V
Input Capacitance, CIN 22µF
Boost Inductor, L1 . . . . . 3.3µH to 10µH
Output Capacitance, COUT 2x22µF
Operating Ambient Temperature Range . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x4 QFN Package (Notes 1, 2)	39	2.5

Storage Temperature . . . . . -65°C to +150°C
Power Dissipation . . . . . See Curves
Maximum Continuous Junction Temperature . . . . . +125°C
Power Dissipation
$T_A \leq +25°C$ 2.44W
$T_A = +70°C$ 1.34W
$T_A = +85°C$ 0.98W
$T_A = +100°C$ 0.61W
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = ENABLE = 5V, VDD1 = VDD2 = 14V, VGH = 25V, AVDD = 10V, T_A = -40°C to +85°C Unless Otherwise Noted.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
GENERAL						
V_S	V_{IN} Input Voltage Range		2.7	3.3	5.5	V
I_{S_DIS}	V_{IN} Supply Currents when Disabled	ENABLE = 0V		0.2	2	µA
I_S	V_{IN} Supply Currents	ENABLE = 5V, LX not switching		1		mA
UVLO	Undervoltage Lockout Threshold	V_{IN2} Rising	2.3	2.45	2.6	V
		V_{IN2} Falling	2.2	2.35	2.5	V
OT_R	Thermal Shutdown Temperature	Temperature Rising		140		°C
OT_F		Temperature Falling		100		°C
LOGIC INPUT CHARACTERISTICS - ENABLE, VFLK, FREQ, VDPM						
V_{IL}	Low Voltage Threshold				0.8	V
V_{IH}	High Voltage Threshold		2.2			V
R_{IL}	Pull-Down Resistor	Enabled, Input at Vin	150	250	400	kΩ
STEP-UP SWITCHING REGULATOR						
A_{VDD}	Output Voltage Range		VIN*1.25		20	V
$\Delta A_{VDD}/\Delta I_{OUT}$	Load Regulation	50mA < ILOAD < 250mA		0.2		%
$\Delta A_{VDD}/\Delta V_{IN}$	Line Regulation	ILOAD = 150mA, 3.0 < V_{IN} < 5.5V		0.15	0.25	%/V
ACC_{AVDD}	Overall Accuracy (Line, Load, Temperature)	10mA < ILOAD < 300mA, 3.0 < Vin < 5.5V, 0°C < T_A < +85°C	-3		3	%
V_{FB}	Feedback Voltage (V_{FB})	I_{LOAD} = 100mA, T_A = +25°C	1.20	1.21	1.22	V
		I_{LOAD} = 100mA, T_A = -40°C to +85°C	1.19	1.21	1.23	V

Electrical Specifications V_{IN} = ENABLE = 5V, VDD1 = VDD2 = 14V, VGH = 25V, AVDD = 10V, T_A = -40°C to +85°C Unless Otherwise Noted. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{FB}	FB Input Bias Current			250	500	nA
$R_{DS(ON)}$	Switch On Resistance			150	300	mΩ
EFF	Peak Efficiency			92		%
I_{LIM}	Switch Current Limit		2.1	2.6		A
D_{MAX}	Max Duty Cycle		85	90		%
F_{OSC}	Oscillator Frequency	FREQ = 0V	550	650	800	kHz
		FREQ = V_{IN2}	1.0	1.2	1.4	MHz
I_{SS}	Soft-Start Slew Current	SS < 1V, T_A = +25°C		2.75		µA
VCOM AMPLIFIER RLOAD = 10k, CLOAD = 10pF, Unless Otherwise Stated						
V_{SAMP}	Supply Voltage		4.5		20	V
I_{SAMP}	Supply Current			3		mA
V_{OS}	Offset Voltage			3	20	mV
I_B	Noninverting Input Bias Current			0	100	nA
CMIR	Common Mode Input Voltage Range		0		VDD2	V
CMRR	Common-Mode Rejection Ratio		50	70		dB
PSRR	Power Supply Rejection Ratio		70	85		dB
VOH	Output Voltage Swing High	Iout(source) = 5mA		VDD2 - 50		mV
VOH	Output Voltage Swing High	Iout(source) = 50mA		VDD2 - 450		mV
VOL	Output Voltage Swing Low	Iout(sink) = 5mA		50		mV
VOL	Output Voltage Swing Low	Iout(sink) = 50mA		450		mV
I_{SC}	Output Short Circuit Current		250	400		mA
SR	Slew Rate			50		V/µs
BW	Gain Bandwidth	-3dB gain point		30		MHz
GATE PULSE MODULATOR						
VGH	VGH Voltage		7		30	V
I_{VGH}	VGH Input Current	VFLK = 0		260		µA
		RE = 33kΩ, VFLK = VDD1		40		µA
V_{DD1}	VDD1 Voltage		3		VGH - 2	V
I_{VDD1}	VDD1 Input Current		-2	0.1	2	µA
R_{ONVGH}	VGH to VGH_M On Resistance			70		Ω
I_{DIS_VGH}	VGH_M Discharge Current (Note 1)	RE = 33kΩ		8		mA
T_{DEL}	DELAY Time (Note 2)	CE = 470pF, RE = 33kΩ		1.9		µs

NOTES:

1. Nominal discharge current = 300/(RE+5kΩ).
2. Nominal delay time = 4000*CE.

Typical Performance Curves

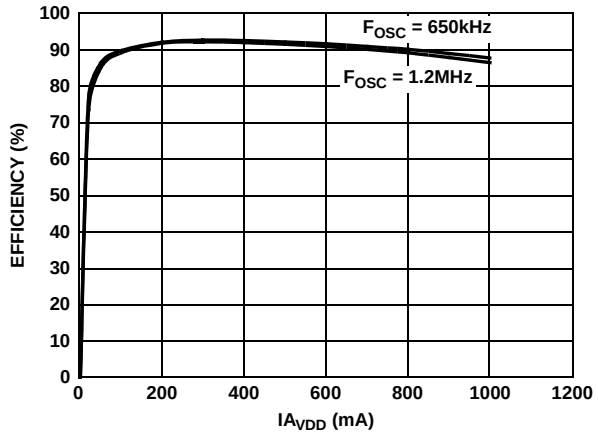


FIGURE 1. A_{VDD} EFFICIENCY vs IA_{VDD}

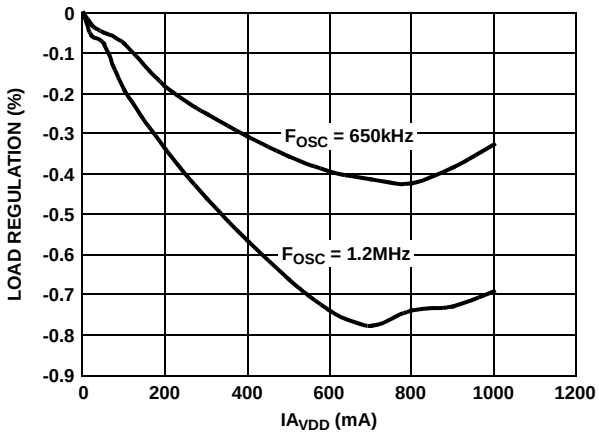


FIGURE 2. A_{VDD} LOAD REGULATION vs IA_{VDD}

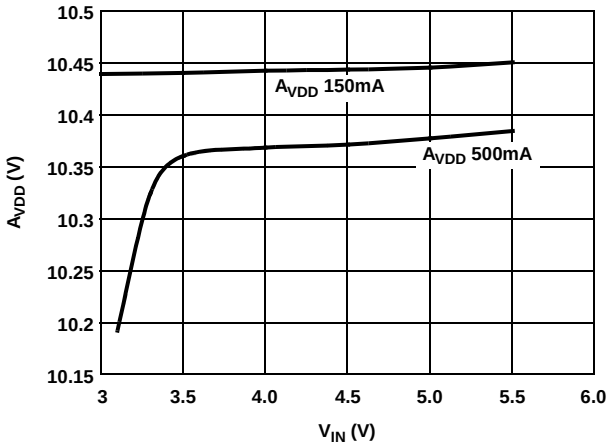


FIGURE 3. LINE REGULATION A_{VDD} vs V_{IN}

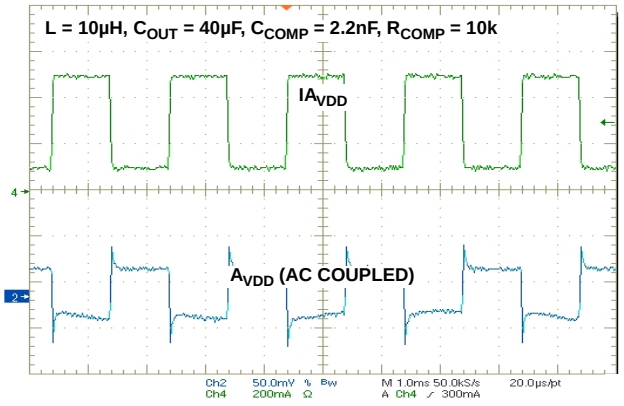


FIGURE 4. BOOST CONVERTER TRANSIENT RESPONSE

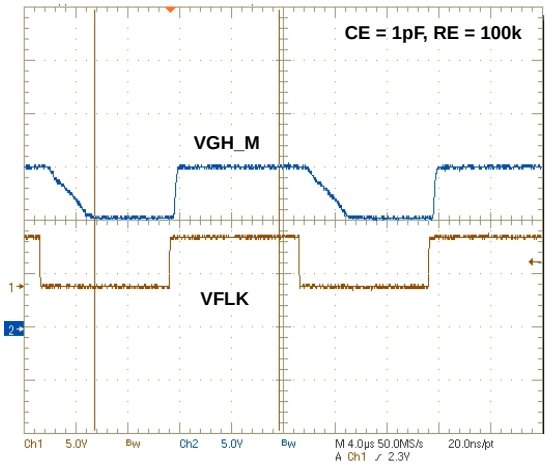


FIGURE 5. GPM CIRCUIT WAVEFORM

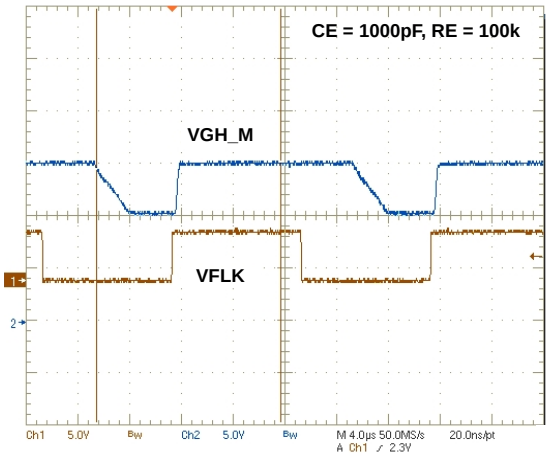


FIGURE 6. GPM CIRCUIT WAVEFORM

Typical Performance Curves (Continued)

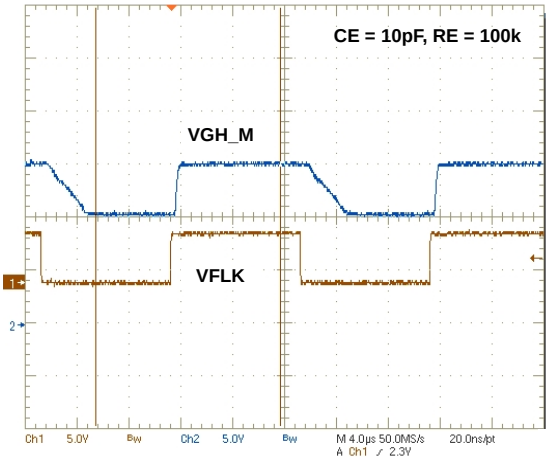


FIGURE 7. GPM CIRCUIT WAVEFORM

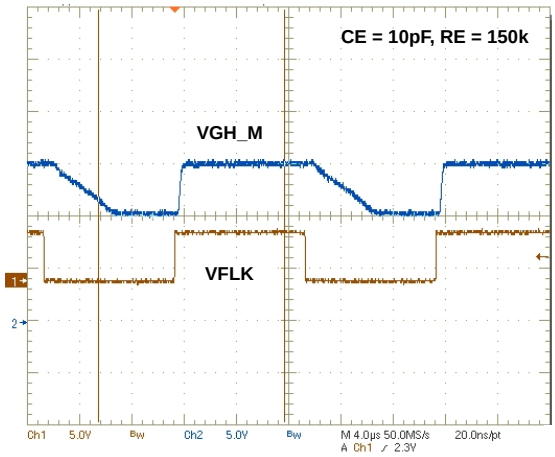


FIGURE 8. GPM CIRCUIT WAVEFORM

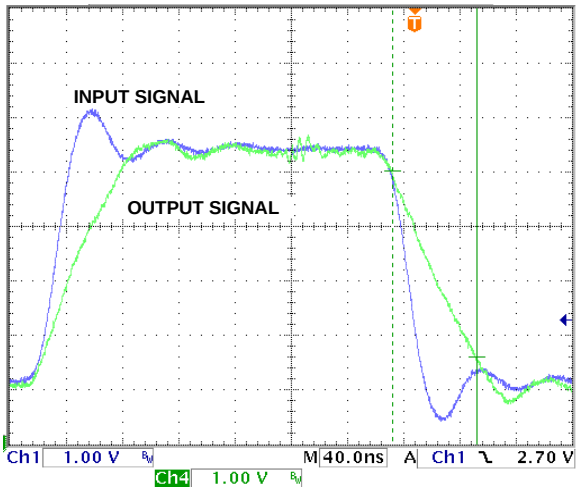


FIGURE 9. V_{COM} RISING SLEW RATE

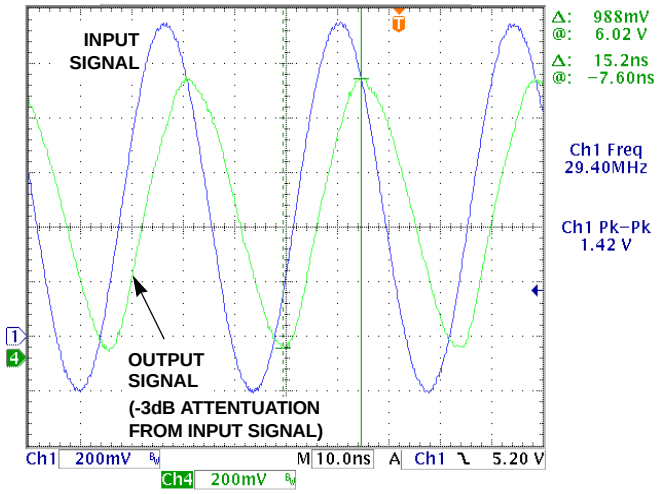


FIGURE 10. V_{COM} BANDWIDTH MEASUREMENT

Block Diagram

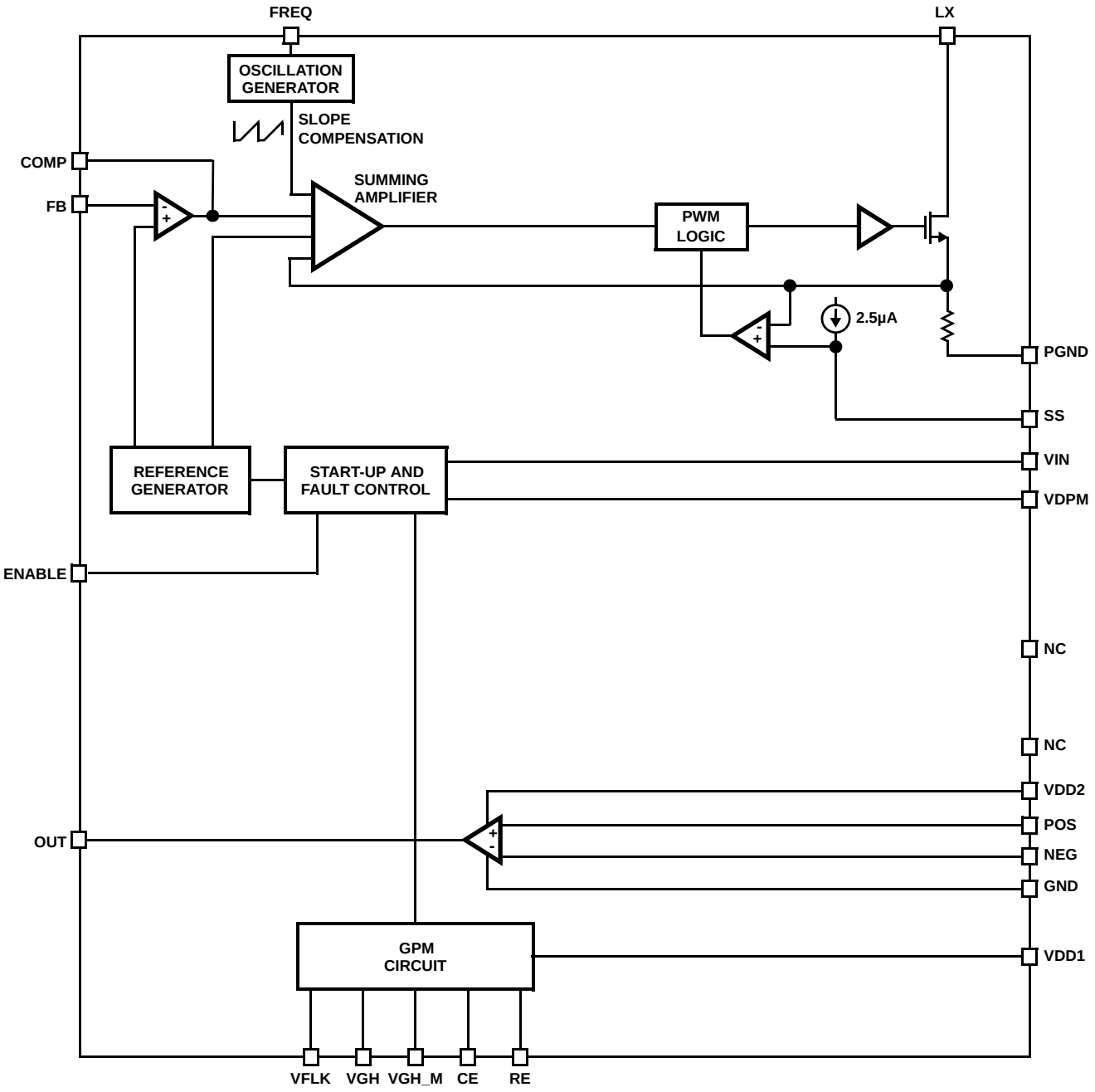


FIGURE 11. ISL97645 BLOCK DIAGRAM

Typical Application Diagram

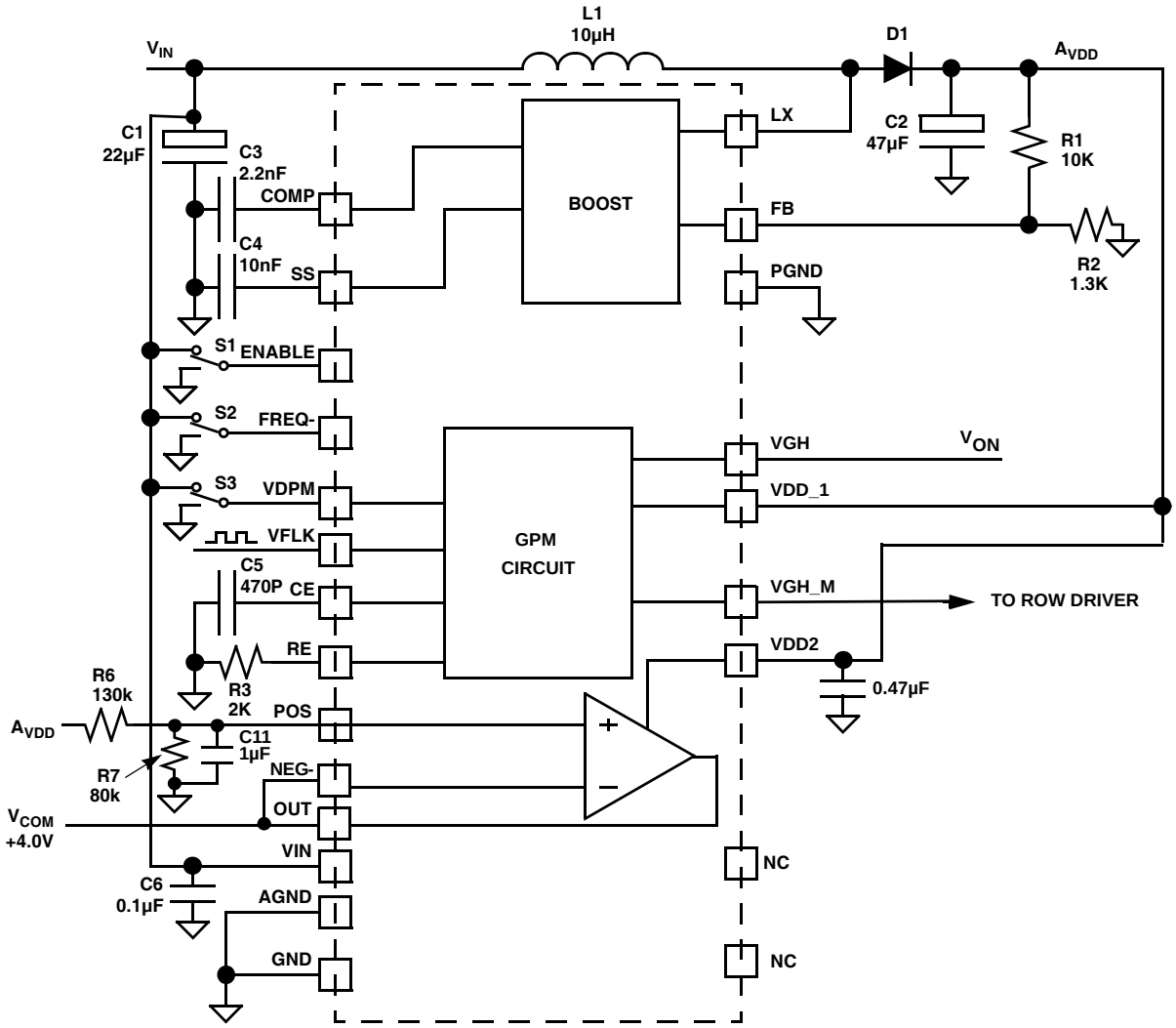


FIGURE 12. TYPICAL APPLICATION DIAGRAM

Applications Information

The ISL97645 provides a complete power solution for TFT LCD applications. The system consists of one boost converter to generate A_{VDD} voltage for column drivers, one integrated V_{COM} buffer which can provide up to 400mA peak current. This part also integrates Gate Pulse Modulator circuit that can help to optimize the picture quality.

Enable Control

When enable pin is pulling down, the ISL97645 is shut down reducing the supply current to <10µA. When the voltage at enable pin reaches 2.2V, the ISL97645 is on.

Boost Converter

Frequency Selection

The ISL97645 switching frequency can be user selected to operate at either constant 650kHz or 1.2MHz. Lower switching frequency can save power dissipation, while higher switching frequency can allow smaller external components like inductor and output capacitors, etc. Connecting FREQ pin to ground sets the PWM switching frequency to 650MHz, or connecting FREQ pin to V_{IN} for 1.2MHz.

Soft-Start

The soft-start is provided by an internal 2.5µA current source to charge the external soft start capacitor. The ISL97645 ramps up current limit from 0A up to full value, as the voltage at SS pin ramps from 0 to 1.2V. Hence the soft-start time is 4.8ms when the soft-start capacitor is 10nF, 22.6ms for 47nF and 48ms for 100nF.

Operation

The boost converter is a current mode PWM converter operating at either a 650kHz or 1.2MHz. It can operate in both discontinuous conduction mode (DCM) at light load and

continuous mode (CCM). In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by:

$$\frac{V_{Boost}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

Where D is the duty cycle of the switching MOSFET.

Figure 11 shows the block diagram of the boost regulator. It uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by the following equation:

$$V_{Boost} = \frac{R_1 + R_2}{R_2} \times V_{FB} \quad \text{(EQ. 2)}$$

The current through the MOSFET is limited to $2.6A_{PEAK}$.

This restricts the maximum output current (average) based on the following equation:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

Where ΔI_L is peak to peak inductor ripple current, and is set by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_s} \quad \text{(EQ. 4)}$$

where f_S is the switching frequency (650kHz or 1.2MHz).

The Table 2 gives typical values (margins are considered 10%, 3%, 20%, 10% and 15% on V_{IN}, V_O, L, f_S and I_{OMAX}).

Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. The ceramic capacitor with capacitance larger than 10µF is recommended. The voltage rating of input capacitor should be larger than the maximum input voltage. Some capacitors are recommended in Table 1 for input capacitor.

TABLE 1. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
10µF/16V	1206	TDK	C3216X7R1C106M
10µF/10V	0805	Murata	GRM21BR61A106K
22µF/10V	1210	Murata	GRB32ER61A226K

TABLE 2. MAXIMUM OUTPUT CURRENT CALCULATION

V_{IN} (V)	V_O (V)	L (µH)	F_s (MHz)	I_{OMAX} (mA)
3	9	10	0.65	636
3	12	10	0.65	419
3	15	10	0.65	289
5	9	10	0.65	1060
5	12	10	0.65	699
5	15	10	0.65	482
5	18	10	0.65	338
3	9	10	1.2	742
3	12	10	1.2	525
3	15	10	1.2	395
5	9	10	1.2	1236
5	12	10	1.2	875
5	15	10	1.2	658
5	18	10	1.2	514

Inductor

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are used to match the internal slope compensation. The inductor must be able to handle the following average and peak current:

$$I_{LAVG} = \frac{I_O}{1-D}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 5)}$$

Some inductors are recommended in Table 3.

TABLE 3. BOOST INDUCTOR RECOMMENDATION

INDUCTOR	DIMENSIONS (mm)	MFG	PART NUMBER
6.8µH/3A_{PEAK}	7.3x6.8x3.2	TDK	RLF7030T-6R8N3R0
10µH/4A_{PEAK}	8.3x8.3x4.5	Sumida	CDR8D43-100NC
5.2µH/4.55A_{PEAK}	10x10.1x3.8	Cooper Bussmann	CD1-5R2

Rectifier Diode

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output voltage. The rectifier diode must meet the output current and peak inductor current requirements. The following table is some recommendations for boost converter diode.

TABLE 4. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATION

DIODE	V_R/I_{AVG} RATING	PACKAGE	MFG
SS23	30V/2A	SMB	Fairchild Semiconductor
MBRS340	40V/3A	SMC	International Rectifier
SL23	30V/2A	SMB	Vishay Semiconductor

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_s} \quad \text{(EQ. 6)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

Note: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across then increases. C_{OUT} in the equation above assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at zero volts.

The following table shows some selections of output capacitors.

TABLE 5. BOOST OUTPUT CAPACITOR RECOMMENDATION

CAPACITOR	SIZE	MFG	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Compensation

The boost converter of ISL97645 can be compensated by a RC network connected from CM1 pin to ground. 4.7nF and 10k RC network is used in the demo board. The larger value resistor and lower value capacitor can lower the transient overshoot, however, at the expense of stability of the loop.

Cascaded MOSFET Application

An 20V N-channel MOSFET is integrated in the boost regulator. For the applications where the output voltage is greater than 20V, an external cascaded MOSFET is needed as shown in Figure 13. The voltage rating of the external MOSFET should be greater than A_{VDD}.

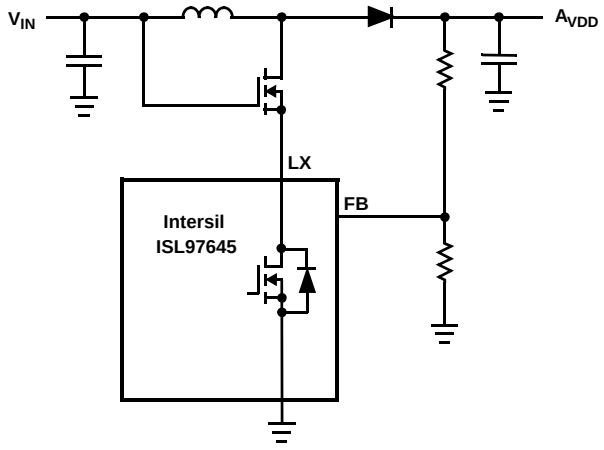


FIGURE 13. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS

Gate Pulse Modulator Circuit

The gate pulse modulator circuit functions as a three way multiplexer, switching VGHM between ground, VDD1 and VGH. Voltage selection is provided by digital inputs VDPM (enable) and VFLK (control). High to low delay and slew control is provided by external components on pins CE and RE, respectively. A block diagram of the gate pulse modulator circuit is shown in Figure 14.

When VDPM is LOW, the block is disabled and VGHM is grounded. When VDPM is HIGH, the output is determined by VFLK. When VFLK goes high, VGHM is pulled to VGH by a 70Ω switch. When VFLK goes low, there is a delay controlled by capacitor CE, following which VGHM is driven to VDD1, with a slew rate controlled by resistor RE. Note that VDD1 is used only as a reference voltage for an amplifier, thus does not have to source or sink a significant DC current.

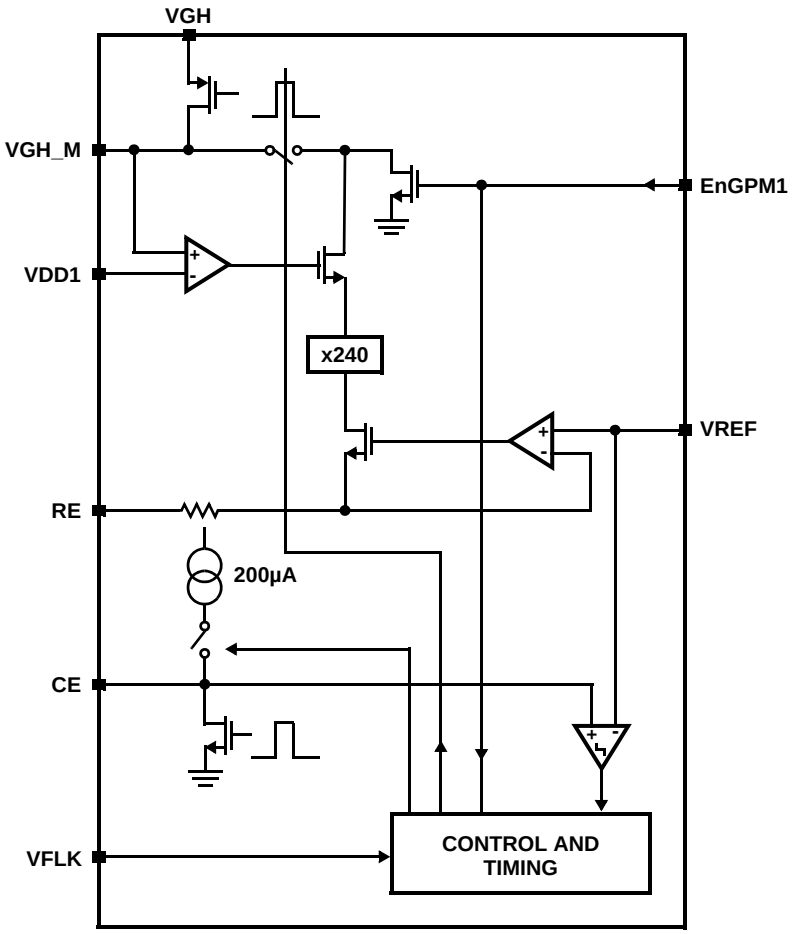


FIGURE 14. GATE PULSE MODULATOR CIRCUIT BLOCK DIAGRAM

Low to high transition is determined primarily by the switch resistance and the external capacitive load. High to low transition is more complex. Take the case where the block is already enabled (VDPM is H). When VFLK is H, pin CE is grounded. On the falling edge of VFLK, a current is passed into pin CE, to charge an external capacitor to 1.2V. This creates a delay, equal to CE*4200. At this point, the output begins to pull down from VGH to VDD1. The slew current is equal to 300/(RE+5000)*Load Capacitance.

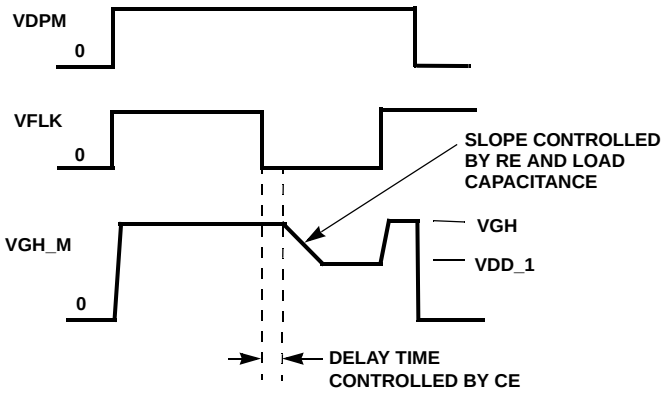


FIGURE 15. GATE PULSE MODULATOR TIMING DIAGRAM

Start-Up Sequence

Figure 16 shows a detailed start-up sequence waveform.

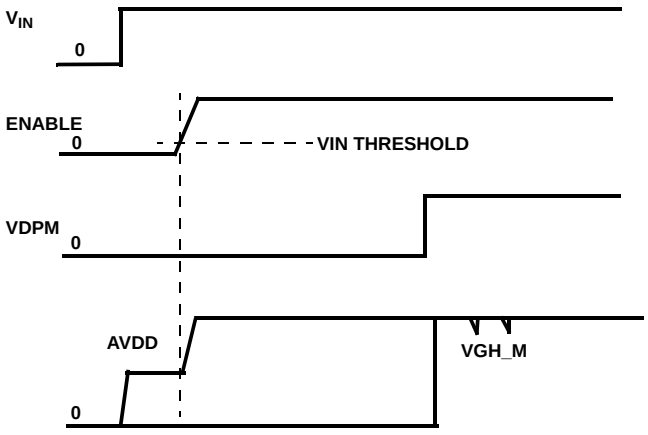


FIGURE 16. START-UP SEQUENCE

When V_{IN} exceeds 2.5V and ENABLE reaches the VIH threshold value, Boost converter starts up, and gate pulse modulator circuit output holds until VDPM goes to high. Note that there is a DC path in the boost converter from the input to the output through the inductor and diode, hence the input voltage will be seen at output with a forward voltage drop of diode before the part is enabled. If this voltage is not desired, the following circuit can be inserted between input and inductor to disconnect the DC path when the part is disabled.

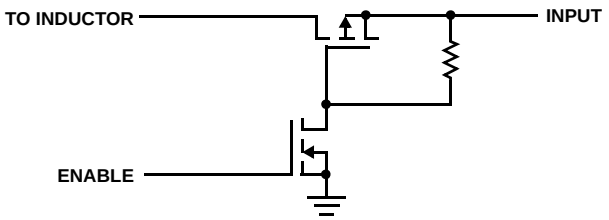


FIGURE 17. CIRCUIT TO DISCONNECT THE DC PATH OF BOOST CONVERTER

V_{COM} Amplifier

The V_{COM} amplifier is designed to control the voltage on the back plate of an LCD display. This plate is capacitively coupled to the pixel drive voltage which alternately cycles positive and negative at the line rate for the display. Thus the amplifier must be capable of sourcing and sinking capacitive pulses of current, which can occasionally be quite large (a few 100mA for typical applications).

The ISL97645 V_{COM} amplifier's output current is limited to 400mA. This limit level, which is roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained. (In this case the whole chip may be shut down by the thermal trip to protect functionality.) If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir capacitor back up once the pulse has stopped. This will happen on the µs time scale in practical systems and for pulses 2 or 3 times the current limit, the V_{COM} voltage will have settled again before the next line is processed.

Fault Protection

ISL97645 provides the overall fault protections including over current protection and over-temperature protection.

An internal temperature sensor continuously monitors the die temperature. In the event that die temperature exceeds the thermal trip point, the device will shut down and disable itself. The upper and lower trip points are typically set to +140°C and +100°C respectively.

Layout Recommendation

The device's performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

There are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} and VDD bypass capacitors close to the pins.
3. Reduce the loop area with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point.
6. The exposed die plate, on the underneath of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. A signal ground plane, separate from the power ground plane and connected to the power ground pins only at the exposed die plate, should be used for ground return connections for control circuit.
9. Minimize feedback input track lengths to avoid switching noise pick-up.

A demo board is available to illustrate the proper layout implementation.

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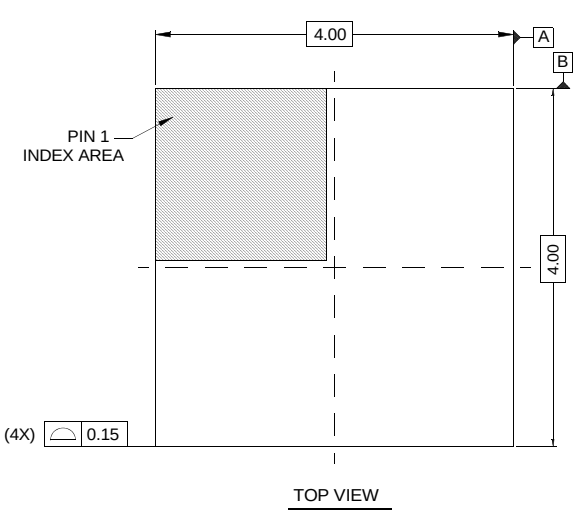
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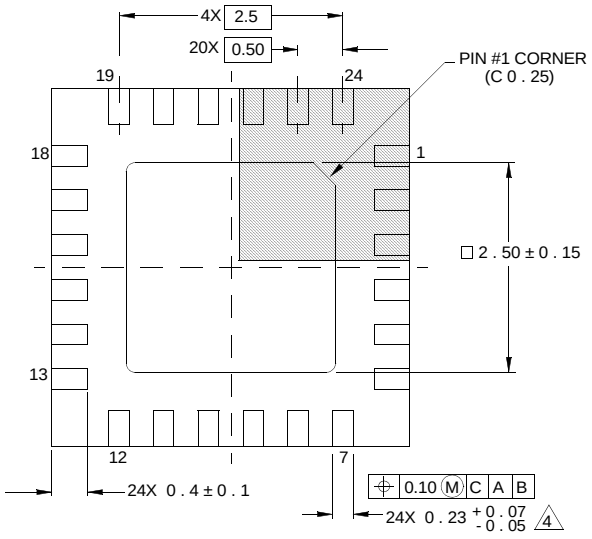
Package Outline Drawing

L24.4x4D

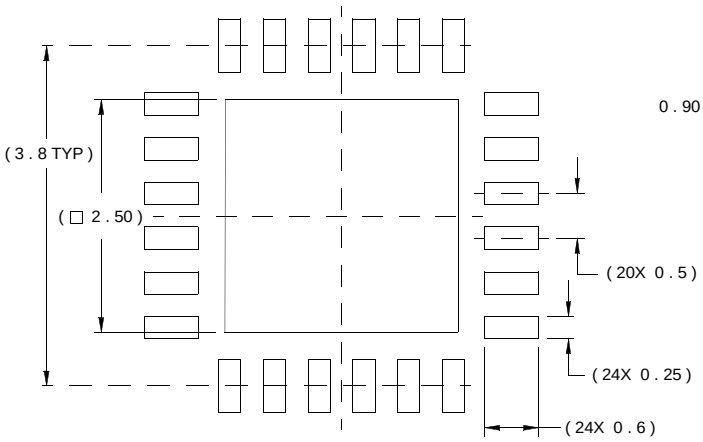
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



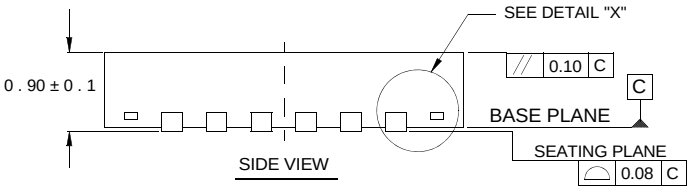
TOP VIEW



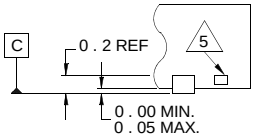
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.