



DESCRIPTION

PT6305 is a 48-Bit High Voltage Display Driver utilizing CMOS technology specially designed for VFD display panels. It provides a 48-bit shift register, a 48-bit latch and a high-voltage CMOS driver. The logic circuit operates on a 5 volt power supply (CMOS level input) making it possible for the PT6305 to be used in conjunction with a microcomputer. The driver block consists of an 80 volt, 50mA (max.) high voltage output buffer. Pin assignments and application circuits are optimized for easy PCB layout and cost saving benefits.

FEATURES

- CMOS technology
- Low power consumption
- 48-bit shift registers
- Data controlled via external transfer clock and latch
- High speed data transfer
- Wide operating temperature range: -40 to +85°C
- High voltage output (70V, 40mA)
- Polarities of all drivers may be inverted by using PCB pin
- Available in 100-pins QFP package

APPLICATION

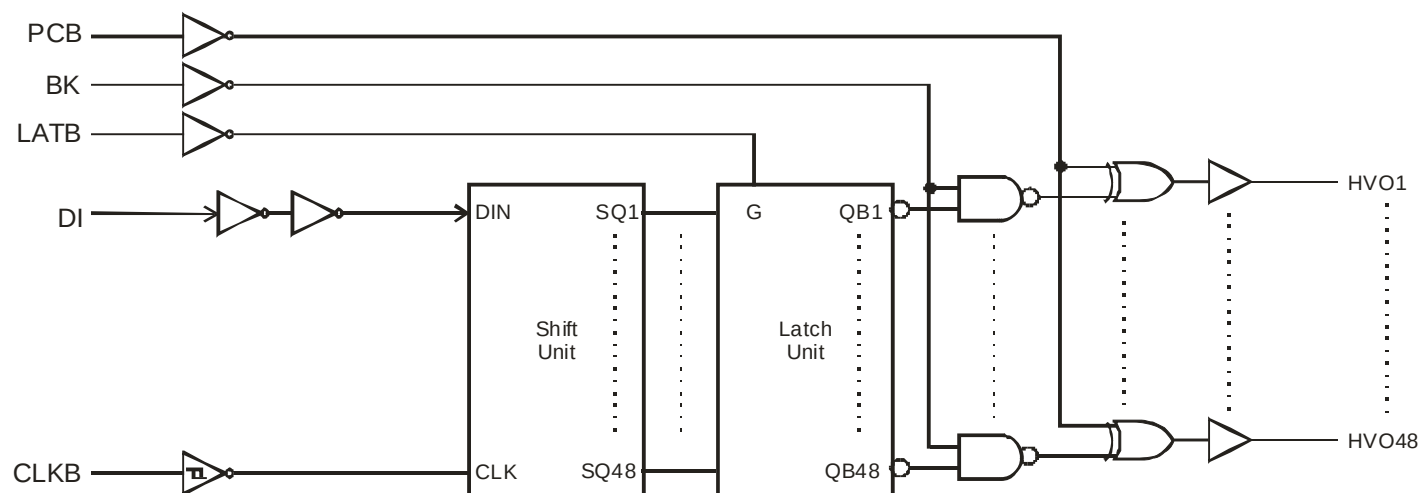
- Microcomputer peripherals



VFD Driver/Controller IC

PT6305

BLOCK DIAGRAM

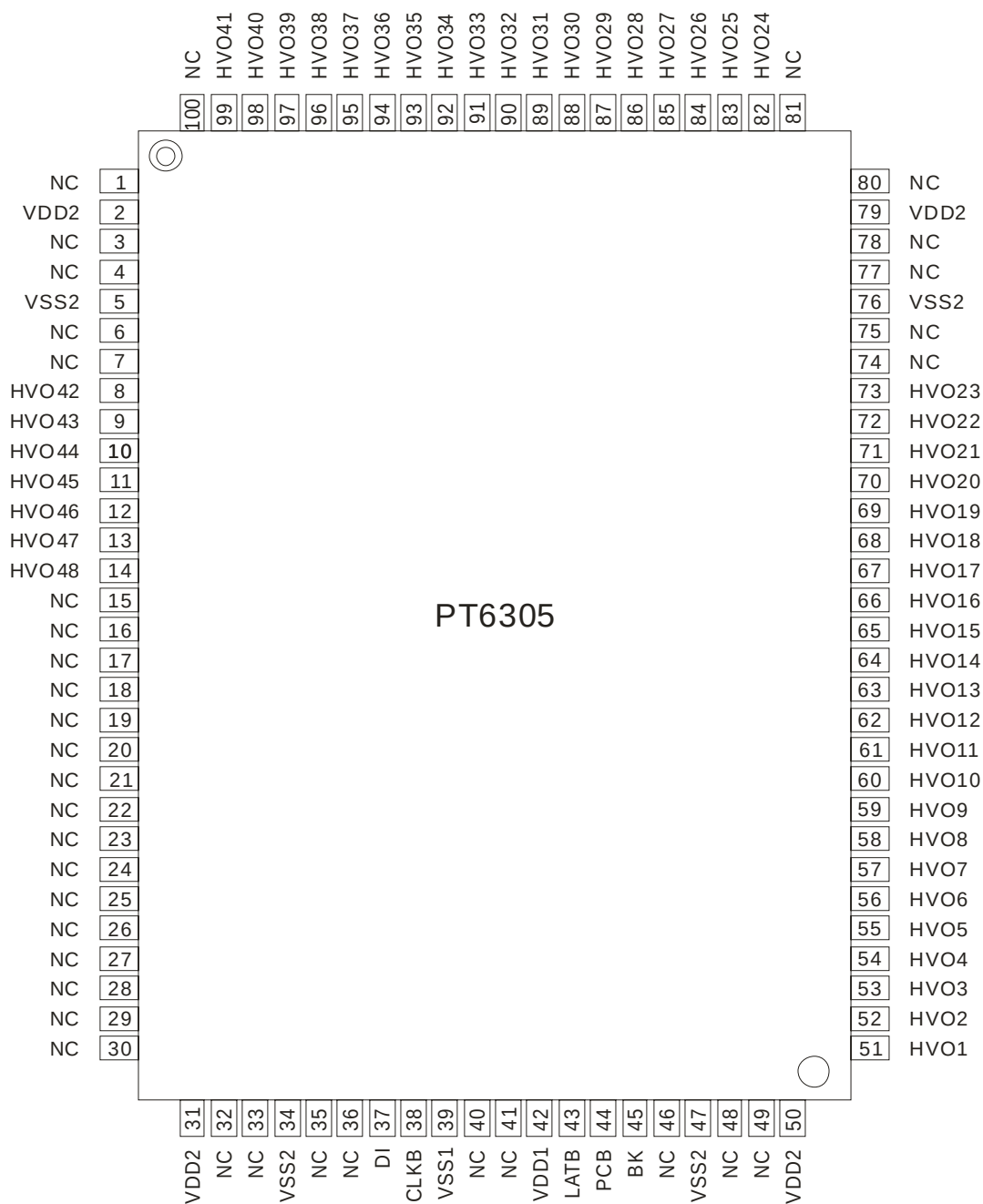




VFD Driver/Controller IC

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PIN CONFIGURATION





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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VDD2	-	Power supply: 10 to 70V	2, 31, 50, 79
VSS2	-	Ground	5, 34, 47, 76
HVO1 ~ HVO23 HVO24 ~ HVO41 HVO42 ~ HVO48	O	High voltage output pins	51 ~ 73 82 ~ 99 8 ~ 14
DI	I	Data input pin	37
CLKB	I	Clock input pin	38
VSS1	-	Ground	39
VDD1	-	Power supply: 5V $\pm$ 10%	42
LATB	I	Latch strobe input pin	43
PCB	I	Reversed polarity pin	44
BK	I	Blank input pin	45
NC	-	Not connected	1, 3, 4, 6, 7, 15 ~ 30, 32, 33, 35, 36, 40, 41, 46, 48, 49, 74, 75, 77, 78, 80, 81, 100

Notes:

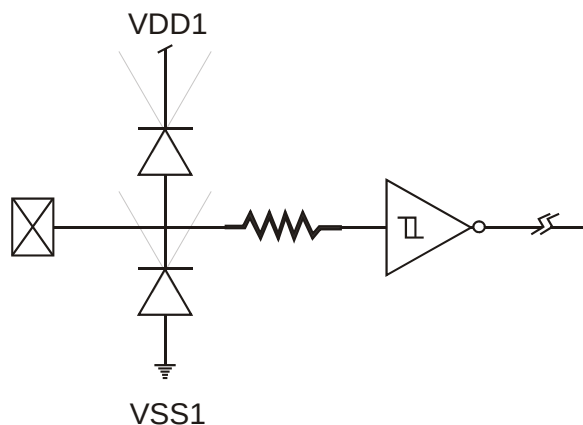
1. Use all the Power Supply Pins: VDD1, VDD2, VSS1, VSS2 (Make sure that VSS1 and VSS2 Pins have the same Voltage Level.)
2. Power must be supplied to VDD1, Logic Inputs and VDD2 so that the device may be protected from any harm caused by latch up. Power must be turned off in a reversed manner. Power ON. OFF sequences must be observed at all times, even during the transition period.



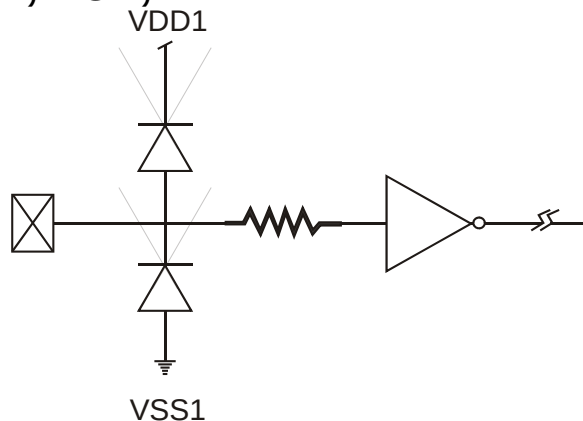
INPUT/OUTPUT PORT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

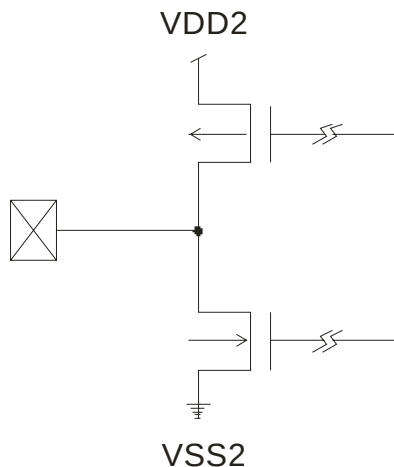
INPUT PIN: CLKB



INPUT PINS: DI, LATB, PCB, BK



OUTPUT PINS: HVO1 TO HVO48





FUNCTION DESCRIPTION

SHIFT REGISTER TRUTH TABLE

Input CLKB	Input DI	Shift Register
↓	H or L	Right Shift
H or L		Hold

LATCH AND DRIVER TRUTH TABLE

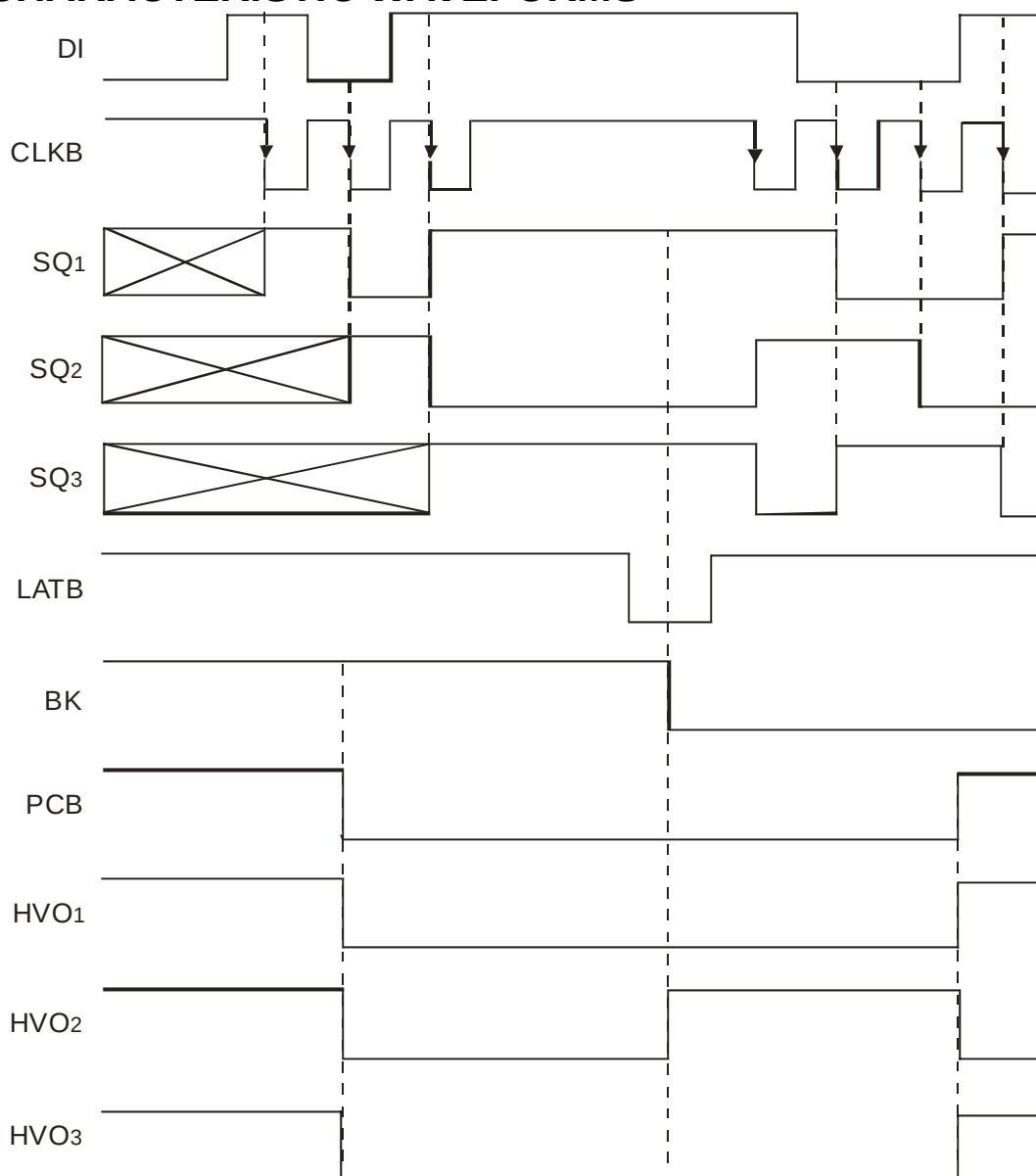
Input				Driver Output Stage
DI	LATB	BK	PCB	
x	x	H	H	H (All driver outputs are "HIGH").
x	x	H	L	L (All driver outputs are "LOW")
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
x	H	L	H	Outputs data immediately before LATB goes to "HIGH".
x	H	L	L	Reverses and outputs data immediately before LATB goes to "HIGH".

Notes:

1. x="High" or "Low" State
2. H="High" State
3. L="Low" State



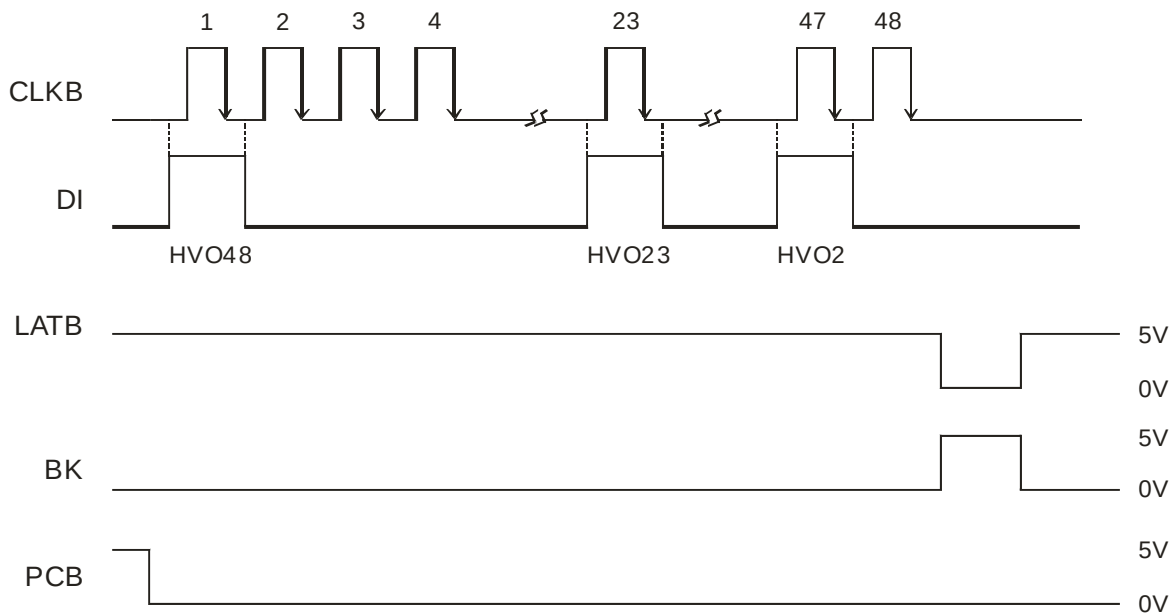
TIMING CHARACTERISTIC WAVEFORMS





FUNCTION CONTROL TIMING WAVEFORMS

An example of function control timing waveforms are given in the diagram below.





ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25°C, Vss1=Vss2=0V)

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD1	-0.5 to +7.0	VL
Logic input voltage	V1	-0.5 to VDD1 + 0.5	V
Logic output voltage	VO1	-0.5 to VDD1 + 0.5	V
Driver supply voltage	VDD2	-0.5 to +80	V
Driver output voltage	VO2	-0.5 to VDD2 + 0.5	V
Driver output current	IO2	± 50	mA
Power dissipation	PD	1000	mW
Operating temperature	Topr	-40 to + 85	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, Ta=25°C, Vss1=Vss2=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	4.5	5.0	5.5	V
High level input voltage	VIH	0.7VDD1	-	VDD1	V
Low level input voltage	VIL	0	-	0.2VDD1	V
Driver supply voltage	VDD2	10	-	70	V
Driver output current	IOL2	-	-	+40	mA
	IOH2	-	-	-40	mA



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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25°C, VDD1=5.0V, VDD2=70V, Vss1=Vss2=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	VOH1	Logic IOH1=-1.0mA	0.9VDD1	-	-	V
High level output voltage	VOH21	HVO1 ~ HVO48, IOH2=-1.0mA	69	-	-	V
	VOH22	HVO1 ~ HVO48, IOH2=-10.0mA	65	-	-	V
Low level output voltage	VOL21	HVO1 ~ HVO48, IOL2=5.0mA	-	-	1.0	V
	VOL22	HVO1 ~ HVO48, IOL2=40.0mA	-	-	1.0	V
High level input current	IIH	VI=VDD1	-	-	1.0	μA
Low level input current	IIL	VI=0V	-	-	-1.0	μA
High level input voltage	VIH	Logic	0.7VDD1	-	-	V
Low level input voltage	VIL	Logic	-	-	0.2VDD1	V
State current dissipation	IDD11	Logic, Ta=25°C	-	-	10	μA
	IDD12	Logic, Ta=-40 to +85°C	-	-	100	μA
	IDD21	Driver, Ta=25°C	-	-	100	μA
	IDD22	Driver, Ta=-40 to +85°C	-	-	1000	μA



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SWITCHING CHARACTERISTICS

(Unless otherwise specified, Ta=25°C, VDD1=5.0V, VDD2=70V, VSS1=VSS2=0V, Logic CL=15pF, Driver CL=50pF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	tPHL1	CLKB→HVO1 ~ HVO48	-	-	160	ns
	tPLH1		-	-	160	ns
	tPHL2	LATB→HVO1 ~ HVO48	-	-	150	ns
	tPLH2		-	-	150	ns
	tPHL3	BK→HVO1 ~ HVO48	-	-	145	ns
	tPLH3		-	-	145	ns
	tPHL4	PCB→HVO1 ~ HVO48	-	-	140	ns
	tPLH4		-	-	140	ns
Rise time	tTLH	HVO1 ~ HVO48	-	-	100	ns
Fall time	tTHL	HVO1 ~ HVO48	-	-	100	ns
Clock frequency	f	Duty=50%, data loading	-	-	16	MHz
		In cascade connection	-	-	16	MHz
Input capacitance	CI		-	-	20	pF

TIMING CHARACTERISTICS

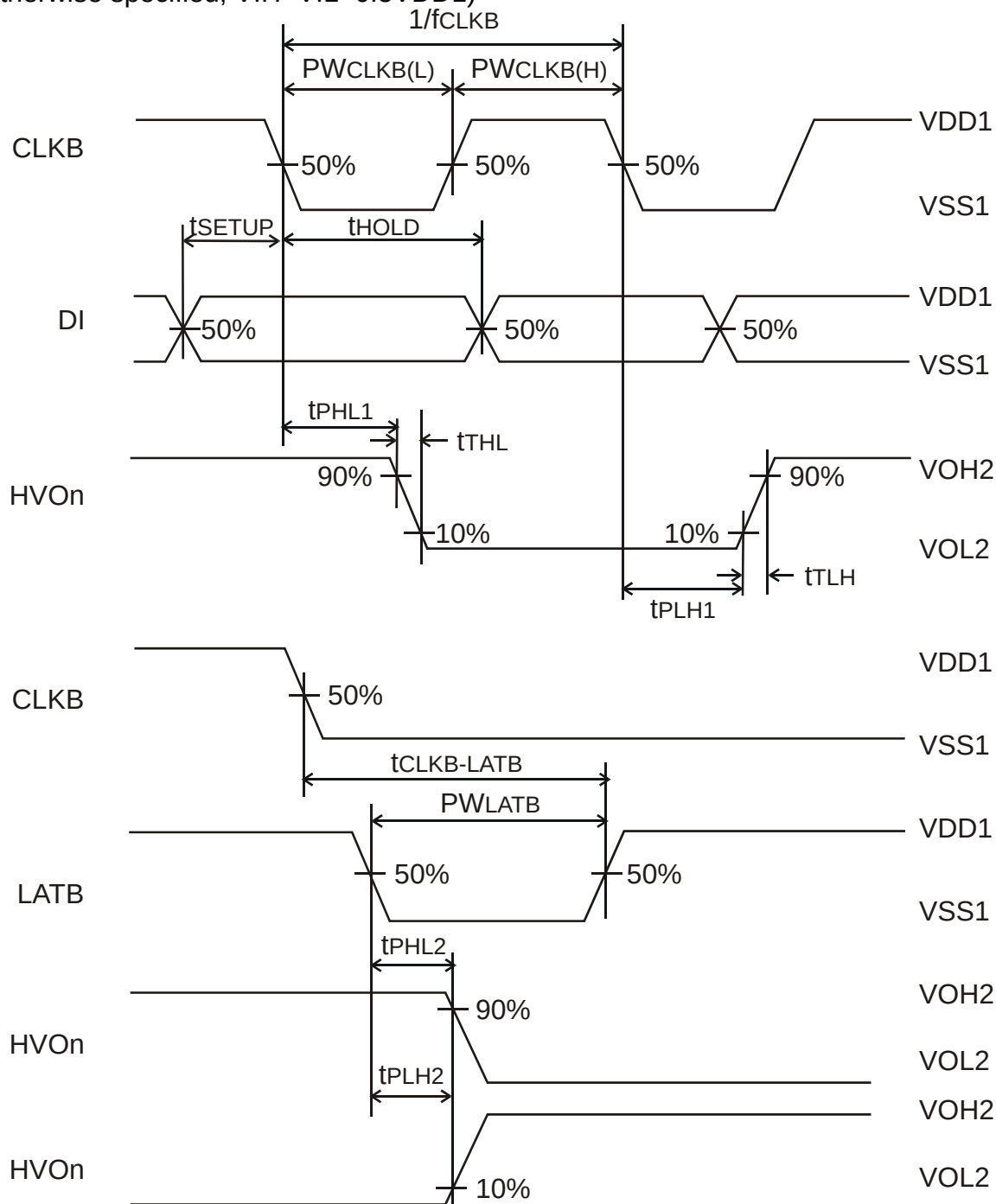
(Unless otherwise specified, Ta=-40 to +80°C, VDD1=4.5 to 5.5V, VSS1=VSS2=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLKB (L), (H)		40	-	-	ns
Strobe pulse width	PWLATB		20	-	-	ns
Blank pulse width	PWBK		200	-	-	ns
PCB pulse width	PWPCB		200	-	-	ns
Data setup time	tSETUP		40	-	-	ns
Data hold time	tHOLD		50	-	-	ns
Clock-strobe time	tCLKB-LATB	CLKB↓ → LATB↑	70	-	-	ns



SWITCHING CHARACTERISTICS WAVEFORMS

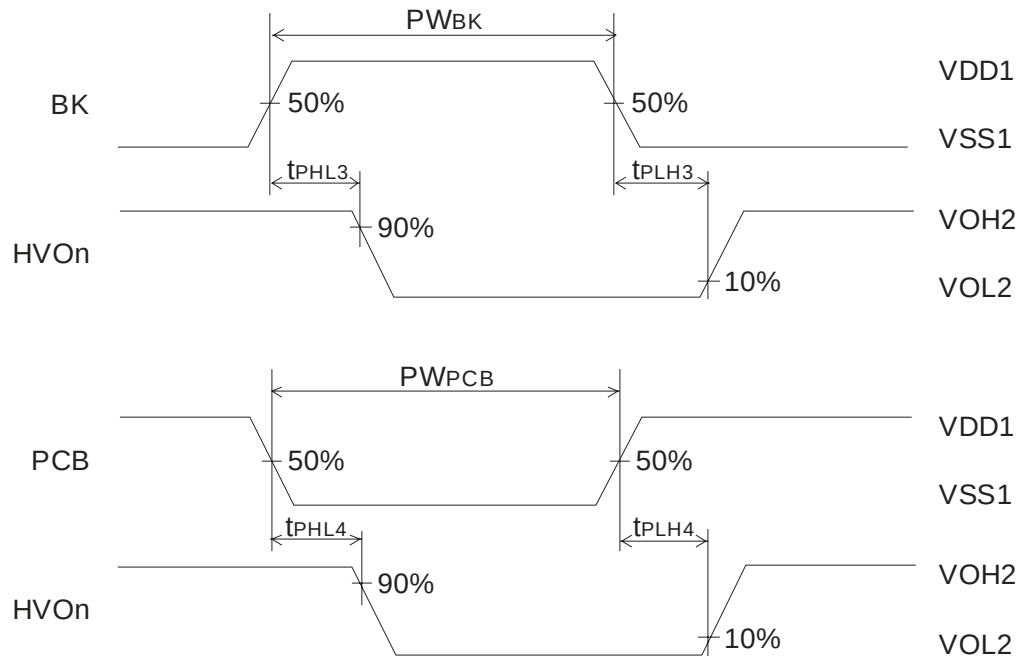
(Unless otherwise specified, $V_{IH}=V_{IL}=0.5V_{DD1}$)





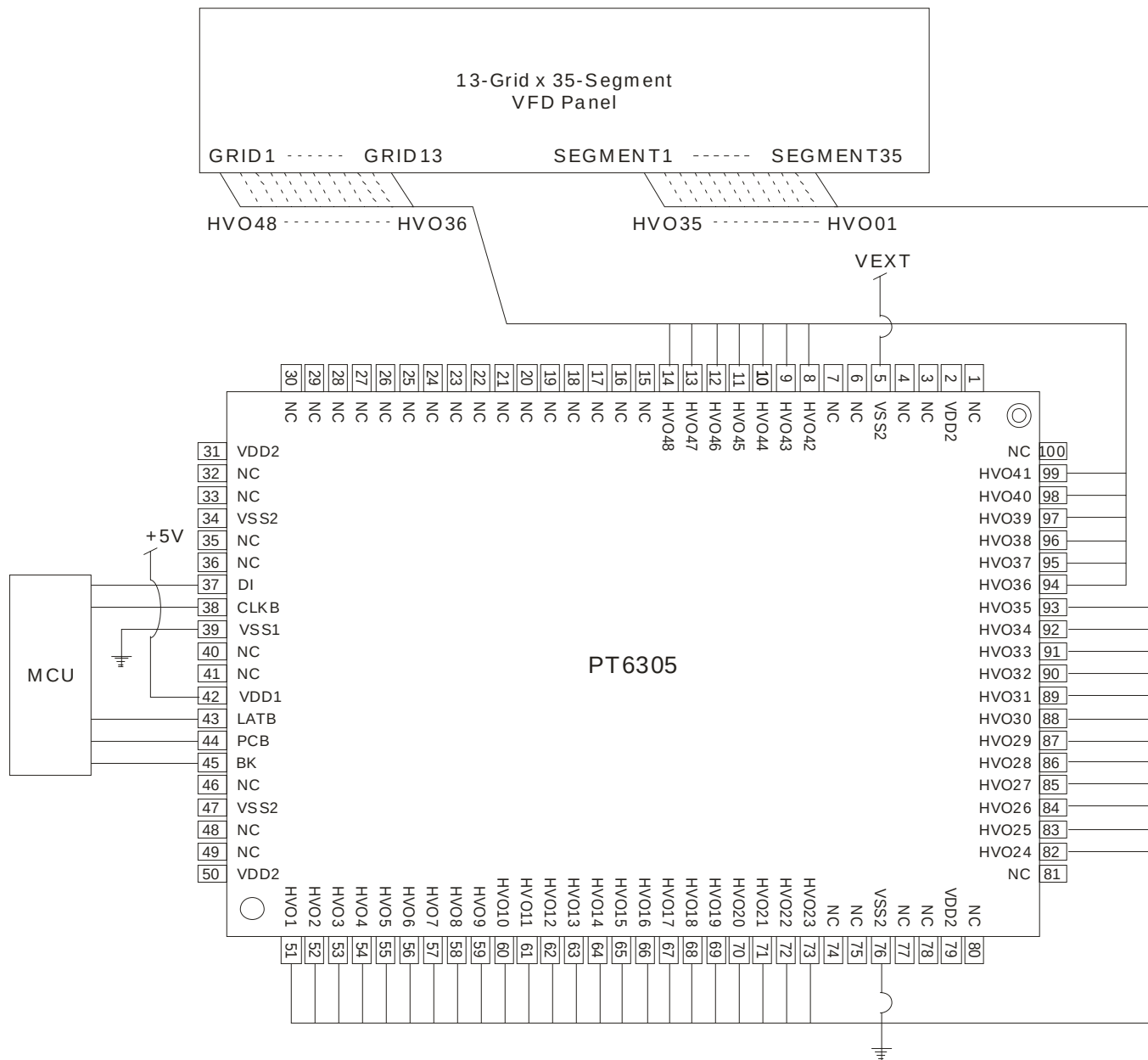
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APPLICATION CIRCUIT



Note: VEXT=External Supply Voltage (Maximum Value=70V, different panel with different voltage)



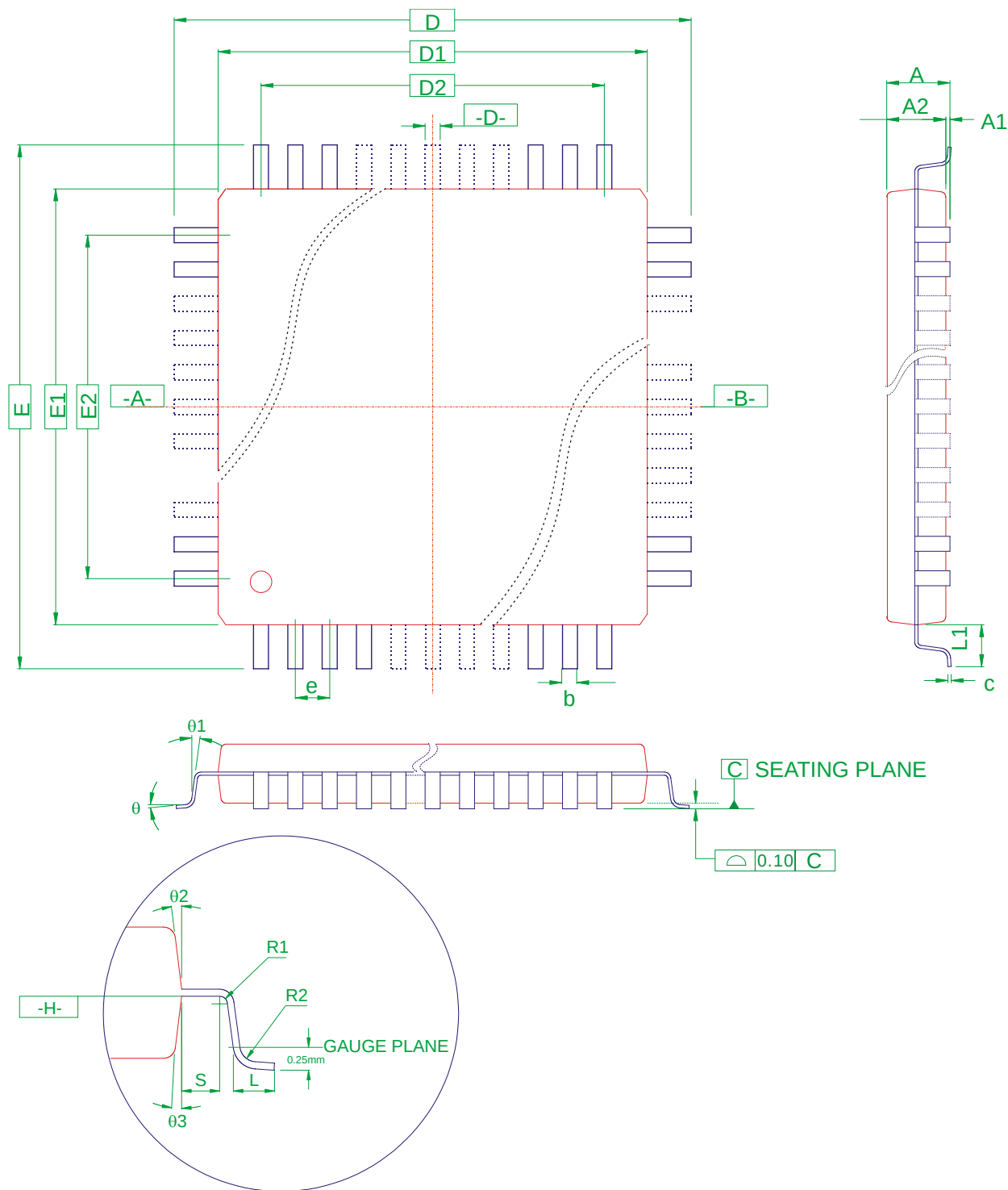
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6305	100 Pins, QFP	PT6305



PACKAGE INFORMATION

100 PINS, QFP PACKAGE (BODY SIZE: 20MM X 14MM, PITCH: 0.65MM)





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Symbol	Min.	Nom.	Max
c	0.11	-	0.23
L	0.73	0.88	1.03
L1	1.60 BSC.		
A			3.40
A1	0.25		0.50
A2	2.50	2.70	2.90
b	0.22		0.40
D	23.20 BSC.		
D1	20.00 BSC.		
D2	18.85 REF.		
E	17.20 BSC.		
E1	14.00 BSC.		
E2	12.35 REF.		
e	0.65 BSC.		
S	0.2	-	-
R1	0.13	-	-
R2	0.13	-	0.30
θ	0°	-	7°
θ1	0°	-	-
θ2	5°	-	16°
θ3	5°	-	16°

Notes:

1. All dimensioning and tolerancing dimension conform to ASME Y14.5M-19942.
2. Dimensions "D1" and "E1" do not include mold protrusion, allowable protrusion is 0.25 mm per side.
3. Regardless of the relative size of the upper and lower body sections, dimensions "D1" and "E1" are determined at the largest feature of the body exclusive of mold flash and gate burrs but including any mismatch between the upper and lower sections of the molded body.
4. All dimensions are in millimeters
5. Dimension "b" do not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed "B" maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
6. Refer to JEDEC MS-022 Variation GC-1

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