ROHM's Selection Operational Amplifier/Comparator Series

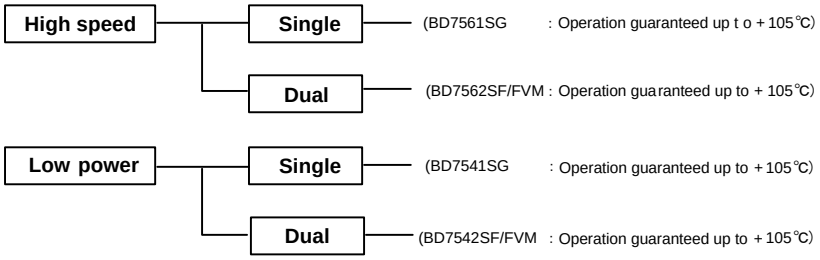
High Voltage Operation CMOS Operational Amplifiers:Input/Output Full Swing

BD7561G,BD7561SG,BD7541G,BD7541SG,
BD7562F/FVM,BD7562SF/FVM,BD7542F/FVM,BD7542SF/FVM

No.09049EBT05

●Description

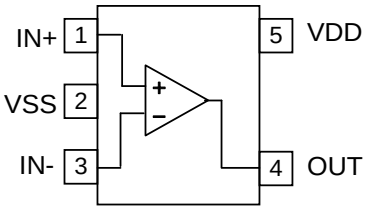
High voltage operable CMOS Op-Amp BD7561/BD7541 family and BD7562/BD7542 family Integrate one or two independent input-output fullswing Op-amps and phase compesation capacitorson a single chip.
Especially, characteristics are wide operating voltagerange of +5[V]～+14.5[V](single power supply),low supply current and little input bias current.

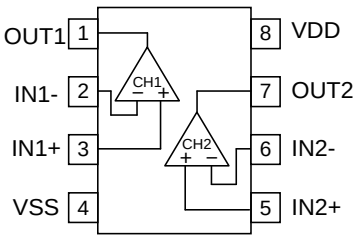


●Features

1) Wide operating supply voltage(＋5[V]～＋14.5[V])
2) ＋5[V]～＋14.5[V](single supply)
   ±2.5[V]～±7.25[V](split supply)
3) Input and Output full swing
4) Internal phase compensation
5) High slew rate (BD7561 family, BD7562 family)
6) Low supply current (BD7541 family, BD7542 family)
7) High large signal voltage gain
8) Internal ESD protection
   Human body model (HBM) ±4000[V](Typ.)
9) Wide temperature range
   -40[℃]～＋85[℃] (BD7561G,BD7562 family, BD7541G,BD7542 family)
   -40[℃]～＋105[℃] (BD7561SG,BD7562S family, BD7541SG,BD7542S family)

●Pin Assignment





SSOP5	SOP8	MSOP8
BD7561G	BD7562F	BD7562FVM
BD7561SG	BD7562SF	BD7562SFVM
BD7541G	BD7542F	BD7542FVM
BD7541SG	BD7542SF	BD7542SFVM

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●Absolute Maximum Ratings (Ta=25[℃])

Parameter	Symbol	Rating		Unit
		BD7561G, BD7562 F/FVM BD7541G, BD7542 F/FVM	BD7561SG, BD7562S F/FVM BD7541SG, BD7542S F/FVM	
Supply Voltage	VDD-VSS	＋15.5		V
Differential Input Voltage(*1)	Vid	VDD-VSS		V
Input Common-mode Voltage Range	Vicm	(VSS-0.3)～(VDD＋0.3)		V
Operating Temperature	Topr	-40～＋85	-40～＋105	℃
Storage Temperature	Tstg	-55～＋125		℃
Maximum Junction Temperature	Tjmax	＋125		℃

Note: Absolute maximum rating item indicates the condition which must not be exceeded.
Application of voltage in excess of absolute maximum rating or use out absoluted maximum rated temperature environment may cause deterioration of characteristics.
(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more then VSS.

●Electric Characteristics

○BD7561 family (Unless otherwise specified VDD=+12[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed limit BD7561G,BD7561SG			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*2)(*4)	Vio	25℃	-	1	9	mV	VDD=5～14.5[V],VOUT=VDD/2
		Full range	-	-	10		
Input Offset Current (*2)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*2)	Ib	25℃	-	1	-	pA	-
Supply Current (*4)	IDD	25℃	-	370	550	μA	RL=∞ All Op-Amps AV=0[dB],VDD=5[V],VIN=2.5[V]
		Full range	-	-	600		
		25℃	-	440	650		RL=∞ All Op-Amps AV=0[dB],VDD=12[V],VIN=6.0[V]
		Full range	-	-	700		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Single Voltage Gain	AV	25℃	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	12	V	VDD-VSS=12[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	-
Output Source Current (*3)	IOH	25℃	3	8	-	mA	VDD-0.4[V]
Output Sink Current (*3)	IOL	25℃	4	14	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	0.9	-	V/μs	CL=25[pF]
Gain Bandwidth Product	FT	25℃	-	1.0	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	50°	-	-	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	-	0.05	-	%	VOUT=1[Vp-p],f=1[kHz]

(*2) Absolute value
(*3) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.
(*4) Full range：BD7561：Ta=-40[℃]～+85[℃] BD7561S：Ta=-40[℃]～+105[℃]

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○BD7562 family (Unless otherwise specified VDD=+12[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed limit BD7562F/FVM BD7562SF/FVM			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*2)(*4)	Vio	25℃	-	1	9	mV	VDD=5～14.5[V],VOUT=VDD/2
		Full range	-	-	10		
Input Offset Current (*2)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*2)	Ib	25℃	-	1	-	pA	-
Supply Current (*4)	IDD	25℃	-	750	1300	μA	RL=∞ All Op-Amps AV=0[dB],VDD=5[V],VIN=2.5[V]
		Full range	-	-	1500		
		25℃	-	900	1400		RL=∞ All Op-Amps AV=0[dB],VDD=12[V],VIN=6.0[V]
		Full range	-	-	1600		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Single Voltage Gain	AV	25℃	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	12	V	VDD-VSS=12[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	-
Output Source Current (*3)	IOH	25℃	3	8	-	mA	VDD-0.4[V]
Output Sink Current (*3)	IOL	25℃	4	14	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	0.9	-	V/μs	CL=25[pF]
Gain Bandwidth Product	FT	25℃	-	1.0	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	50°	-	-	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	-	0.05	-	%	VOUT=1[Vp-p],f=1[kHz]

(*2) Absolute value
(*3) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.
(*4) Full range： BD7562：Ta=-40[℃]～+85[℃] BD7562S：Ta=-40[℃]～+105[℃]

○BD7541 family (Unless otherwise specified VDD=+12[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed limit BD7541G,BD7541SG			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*5)(*7)	Vio	25℃	-	1	9	mV	VDD=5～14.5[V],VOUT=VDD/2
		Full range	-	-	10		
Input Offset Current (*5)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*5)	Ib	25℃	-	1	-	pA	-
Supply Current (*7)	IDD	25℃	-	170	300	μA	RL=∞ All Op-Amps AV=0[dB],VDD=5[V],VIN=2.5[V]
		Full range	-	-	400		
		25℃	-	180	320		RL=∞ All Op-Amps AV=0[dB],VDD=12[V],VIN=6.0[V]
		Full range	-	-	420		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Single Voltage Gain	AV	25℃	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	12	V	VDD-VSS=12[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	-
Output Source Current (*6)	IOH	25℃	2	4	-	mA	VDD-0.4[V]
Output Sink Current (*6)	IOL	25℃	3	7	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	0.3	-	V/μs	CL=25[pF]
Gain Bandwidth Product	FT	25℃	-	0.6	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	50°	-	-	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	-	1	9	%	VOUT=1[Vp-p],f=1[kHz]

(*5) Absolute value
(*6) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.
(*7) Full range：BD7541：Ta=-40[℃]～+85[℃] BD7541S：Ta=-40[℃]～+105[℃]

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○BD7542 family (Unless otherwise specified VDD=+12[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed limit BD7542 F/FVM BD7542S F/FVM			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*5)(*7)	Vio	25℃	-	1	9	mV	VDD=5～14.5[V],VOUT=VDD/2
		Full range	-	-	10		
Input Offset Current (*5)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*5)	Ib	25℃	-	1	-	pA	-
Supply Current (*7)	IDD	25℃	-	340	650	μA	RL=∞ All Op-Amps AV=0[dB],VDD=5[V],VIN=2.5[V]
		Full range	-	-	850		
		25℃	-	400	780		RL=∞ All Op-Amps AV=0[dB],VDD=12[V],VIN=6.0[V]
		Full range	-	-	900		
High Level Output Voltage	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Large Single Voltage Gain	AV	25℃	70	95	-	dB	RL=10[kΩ]
Input Common-mode Voltage Range	Vicm	25℃	0	-	12	V	VDD-VSS=12[V]
Common-mode Rejection Ratio	CMRR	25℃	45	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25℃	60	80	-	dB	-
Output Source Current (*6)	IOH	25℃	2	4	-	mA	VDD-0.4[V]
Output Sink Current (*6)	IOL	25℃	3	7	-	mA	VSS+0.4[V]
Slew Rate	SR	25℃	-	0.3	-	V/μs	CL=25[pF]
Gain Bandwidth Product	FT	25℃	-	0.6	-	MHz	CL=25[pF], AV=40[dB]
Phase Margin	θ	25℃	-	50°	-	-	CL=25[pF], AV=40[dB]
Total Harmonic Distortion	THD	25℃	-	0.05	-	%	VOUT=1[Vp-p],f=1[kHz]

(*5) Absolute value
(*6) Under the high temperature environment, consider the power dissipation of IC when selecting the output current.
When the terminal short circuits are continuously output, the output current is reduced to climb to the temperature inside IC.
(*7) Full range：BD7542：Ta=-40[℃]～+85[℃] BD7542S：Ta=-40[℃]～+105[℃]

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●Example of electrical characteristics

○BD7561 family

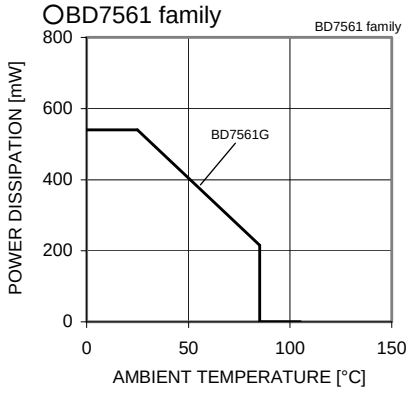


Fig. 1
Derating Curve

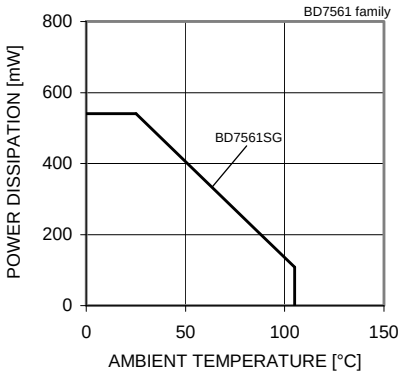


Fig. 2
Derating Curve

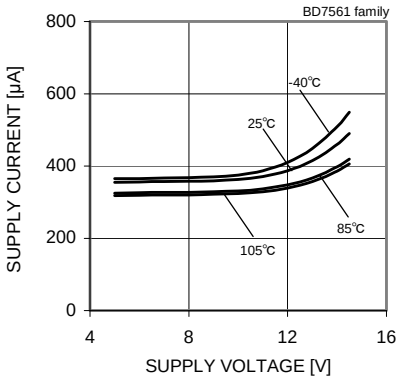


Fig. 3
Supply Current – Supply Voltage

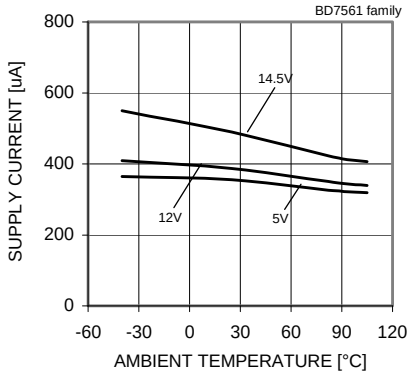


Fig. 4
Supply Current – Ambient Temperature

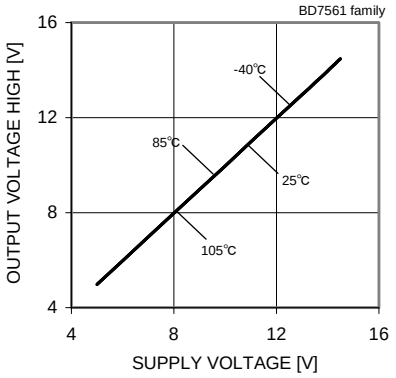


Fig. 5
Output Voltage High – Supply Voltage
(RL=10[kΩ])

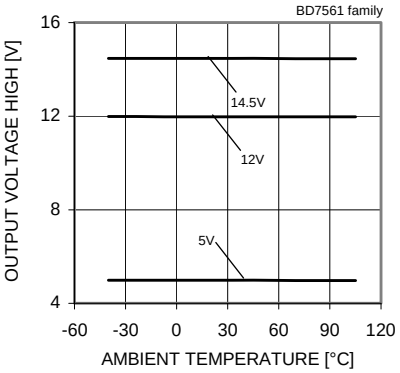


Fig. 6
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

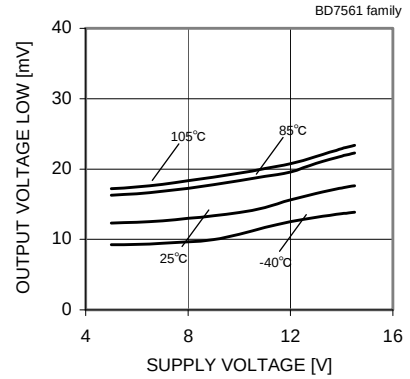


Fig. 7
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

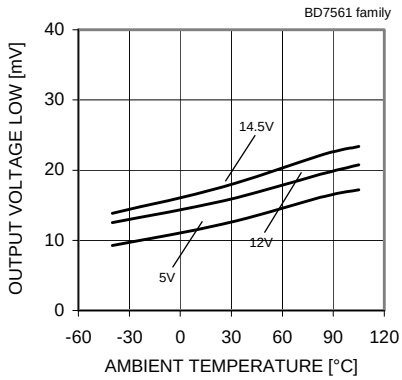


Fig. 8
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

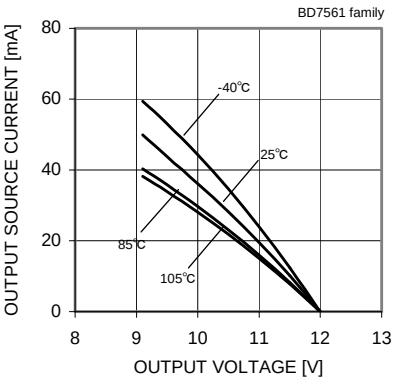


Fig. 9
Output Source Current – Output Voltage
(VDD=12[V])

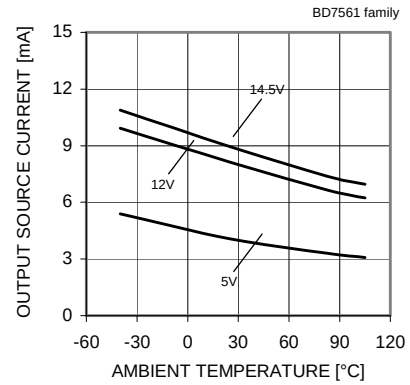


Fig. 10
Output Source Current – Ambient Temperature(VOUT=VDD-0.4[V])

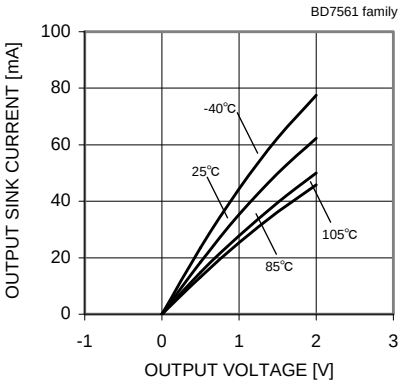


Fig. 11
Output Sink Current – Output Voltage
(VDD=12[V])

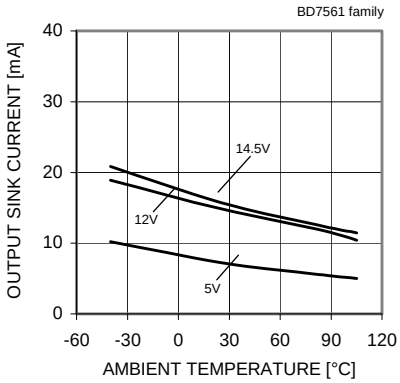


Fig. 12
Output Sink Current – Ambient Temperature
(VOUT=VDD-11.6[V])

(＊)The above data is ability value of sample, it is not guaranteed. BD7561 : -40[℃]～+85[℃] BD7561S : -40[℃]～+105[℃]

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○BD7561 family

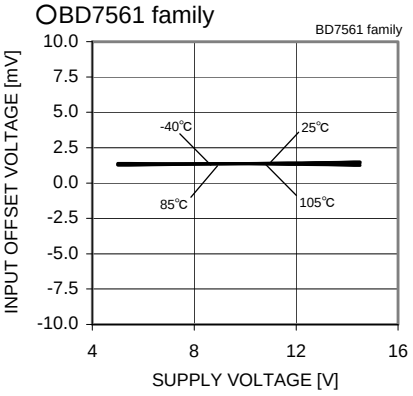


Fig. 13
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=VDD/2)

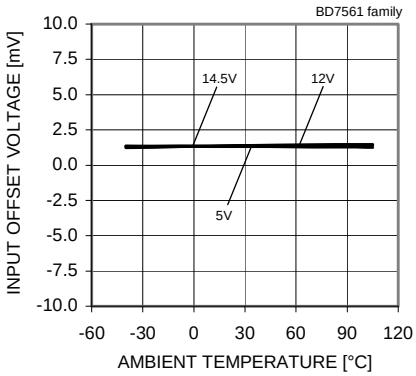


Fig. 14
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=VDD/2)

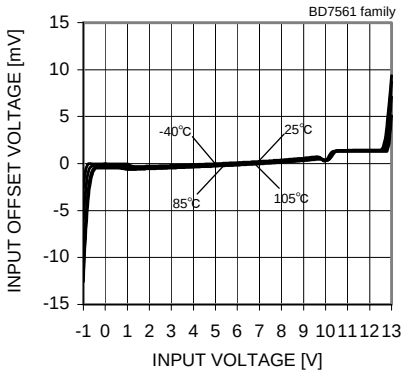


Fig. 15
Input Offset Voltage – Input Voltage
(VDD=12[V])

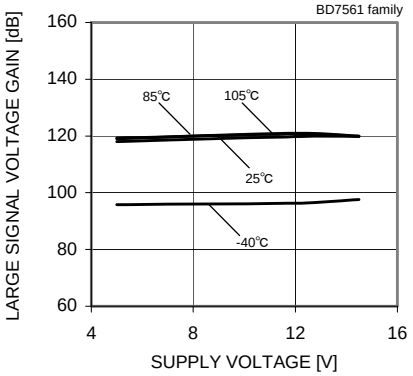


Fig. 16
Large Signal Voltage Gain
– Supply Voltage

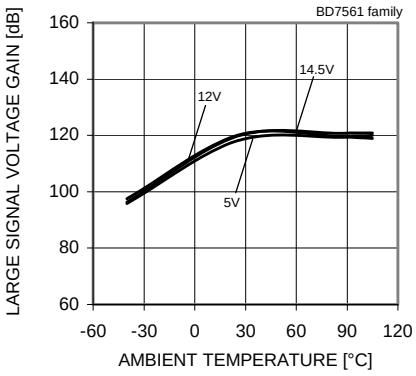


Fig. 17
Large Signal Voltage Gain
– Ambient Temperature

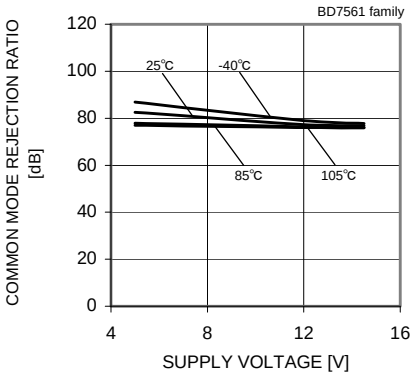


Fig. 18
Common Mode Rejection Ratio
– Supply Voltage
(VDD=12[V])

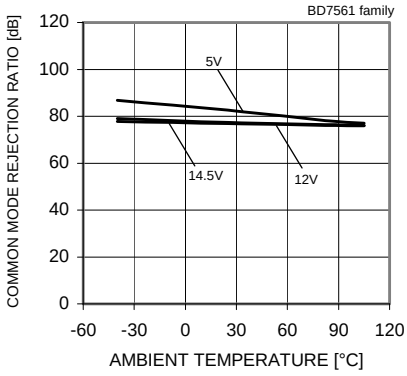


Fig. 19
Common Mode Rejection Ratio
– Ambient Temperature
(VDD=12[V])

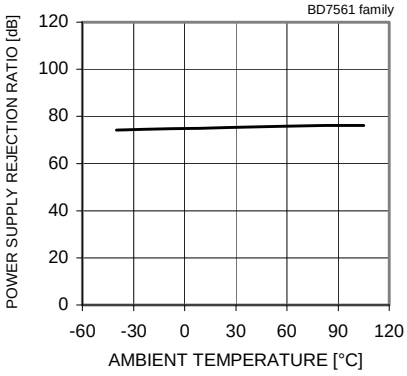


Fig. 20
Power Supply Rejection Ratio
– Ambient Temperature

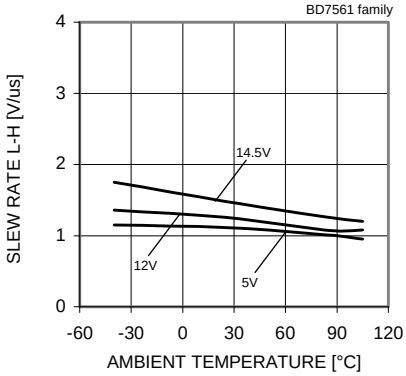


Fig. 21
Slew Rate L-H – Ambient Temperature

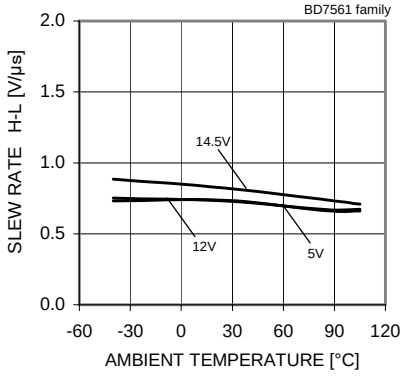


Fig. 22
Slew Rate H-L – Ambient Temperature

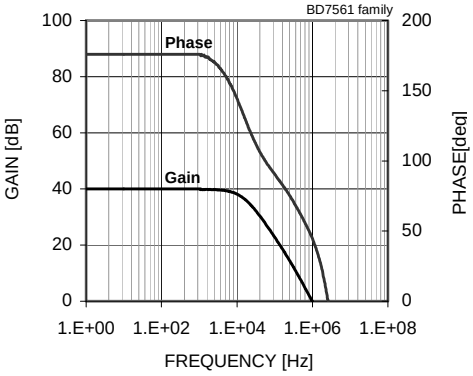


Fig. 23
Gain - Frequency

(＊)The above data is ability value of sample, it is not guaranteed. BD7561：-40[℃]～+85[℃] BD7561S：-40[℃]～+105[℃]

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○BD7562 family

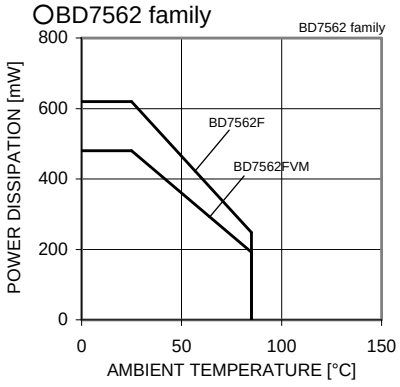


Fig. 24
Derating Curve

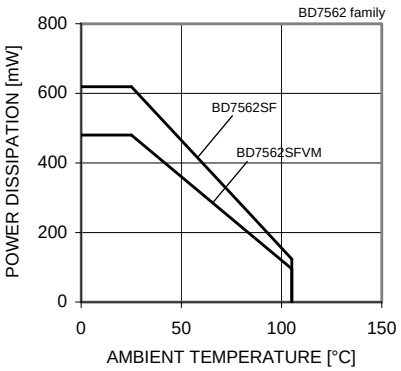


Fig. 25
Derating Curve

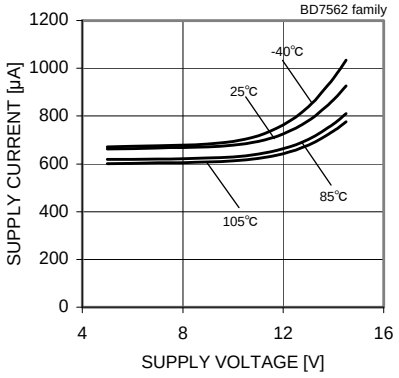


Fig. 26
Supply Current – Supply Voltage

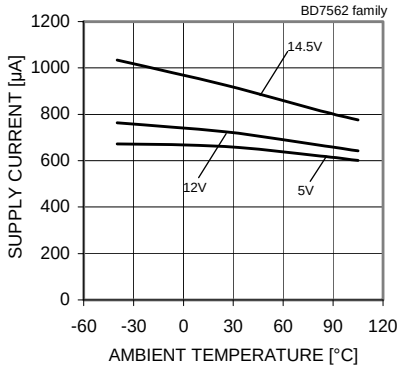


Fig. 27
Supply Current – Ambient Temperature

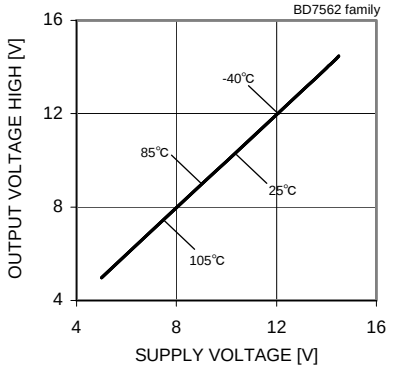


Fig. 28
Output Voltage High – Supply Voltage
(RL=10[kΩ])

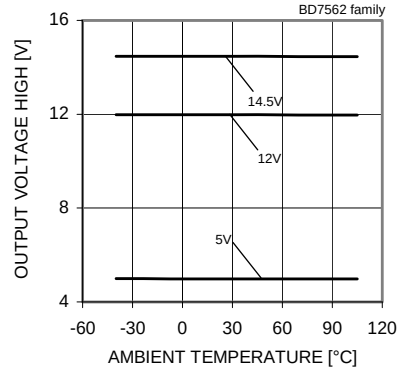


Fig. 29
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

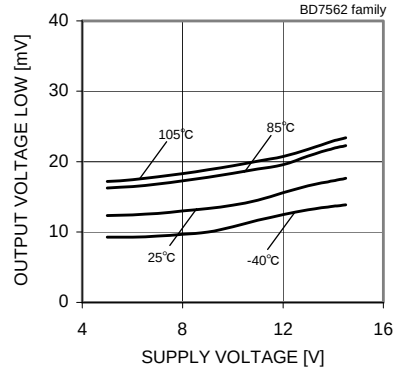


Fig. 30
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

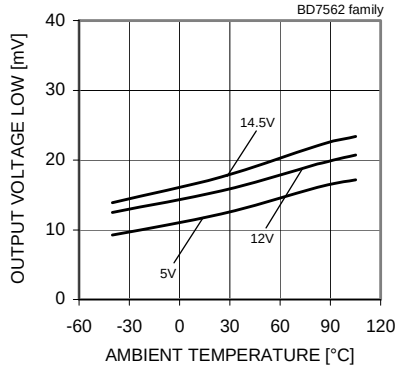


Fig. 31
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

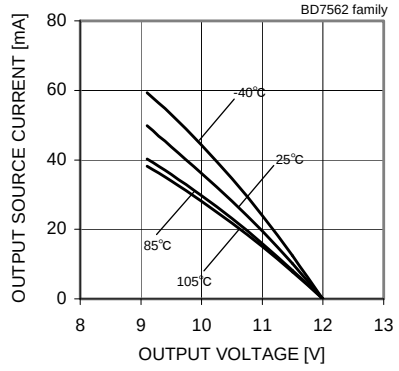


Fig. 32
Output Source Current – Output Voltage
(VDD=12[V])

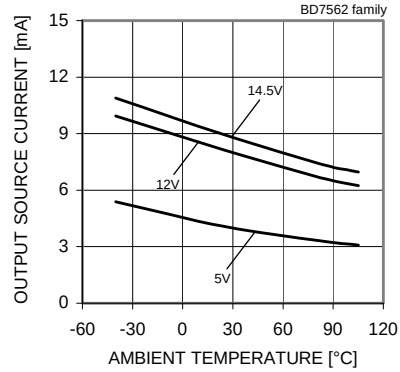


Fig. 33
Output Source Current – Ambient Temperature

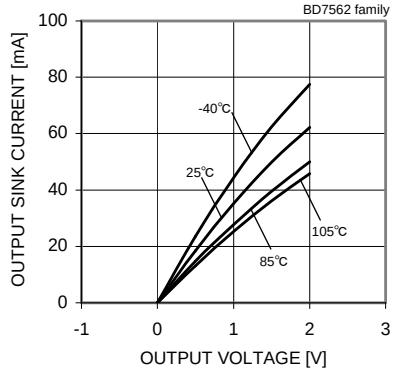


Fig. 34
Output Sink Current – Output Voltage
(VDD=12[V])

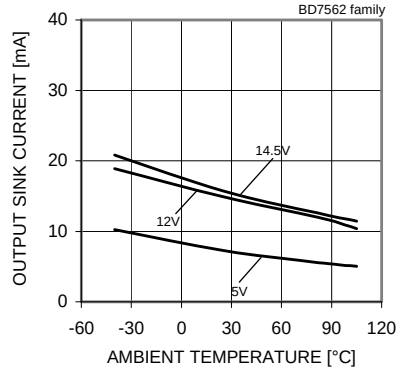


Fig. 35
Output Sink Current – Ambient Temperature
(VOUT=VDD-11.6[V])

(∗)The above data is ability value of sample, it is not guaranteed. BD7562 : -40[℃]～+85[℃] BD7562S : -40[℃]～+105[℃]

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○BD7562 family

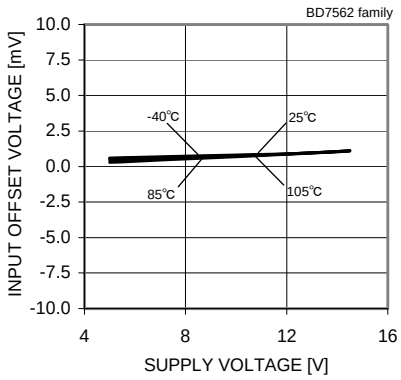


Fig. 36
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=VDD/2)

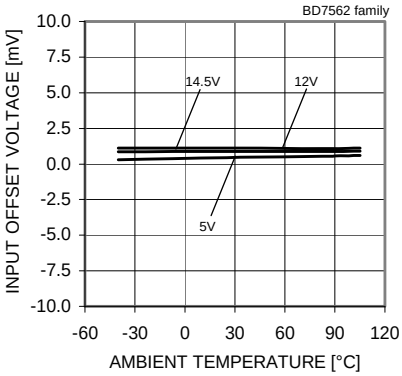


Fig. 37
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=VDD/2)

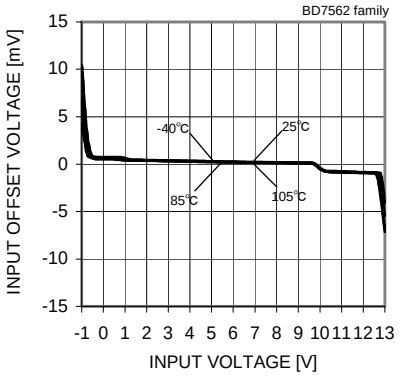


Fig. 38
Input Offset Voltage – Input Voltage
(VDD=12[V])

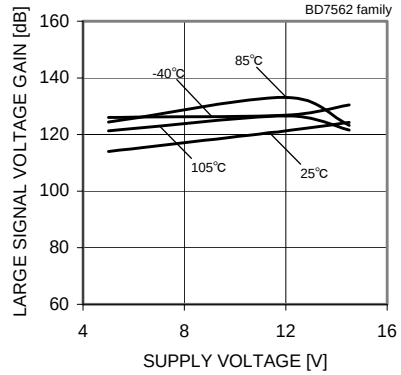


Fig. 39
Large Signal Voltage Gain
– Supply Voltage

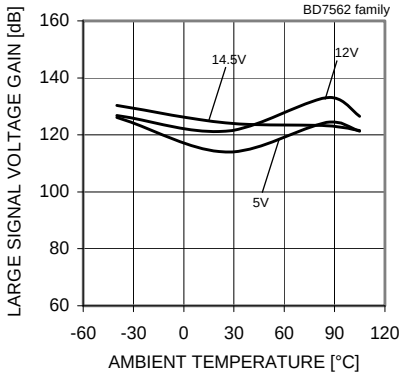


Fig. 40
Large Signal Voltage Gain
– Ambient Temperature

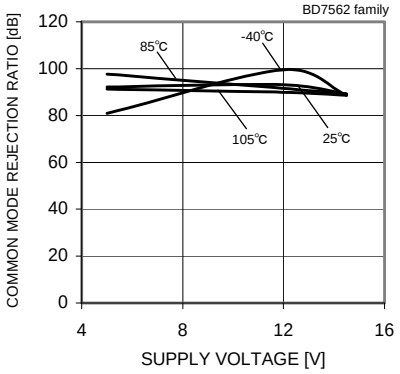


Fig. 41
Common Mode Rejection Ratio
– Supply Voltage
(VDD=12[V])

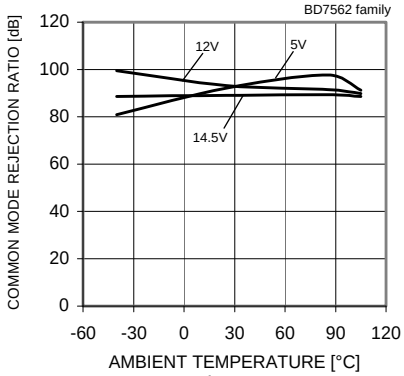


Fig. 42
Common Mode Rejection Ratio
– Ambient Temperature
(VDD=12[V])

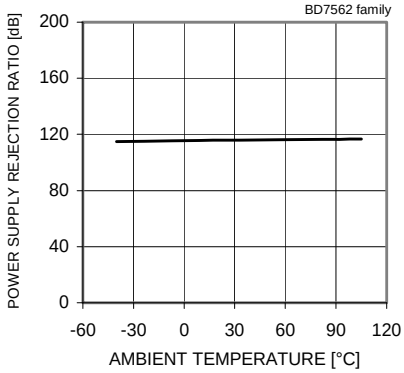


Fig. 43
Power Supply Rejection Ratio
– Ambient Temperature

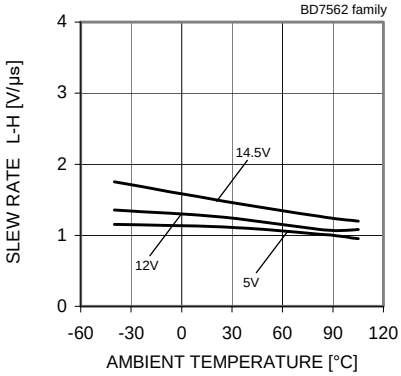


Fig. 44
Slew Rate L-H – Ambient Temperature

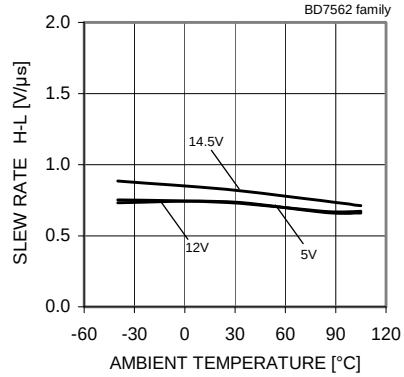


Fig. 45
Slew Rate H-L – Ambient Temperature

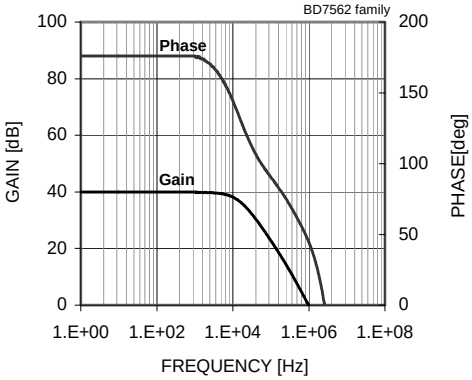


Fig. 46
Gain - Frequency

(∗)The above data is ability value of sample, it is not guaranteed. BD7562：-40[℃]～+85[℃] BD7562S：-40[℃]～+105[℃]

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○BD7541 family

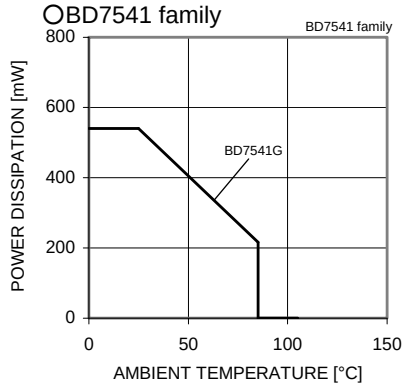


Fig. 47
Derating Curve

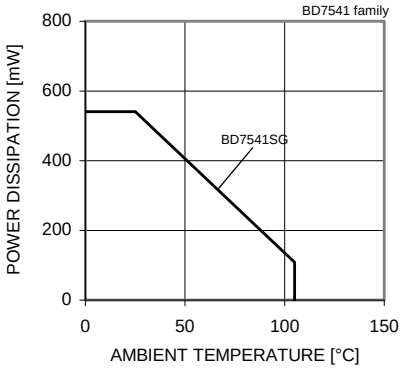


Fig. 48
Derating Curve

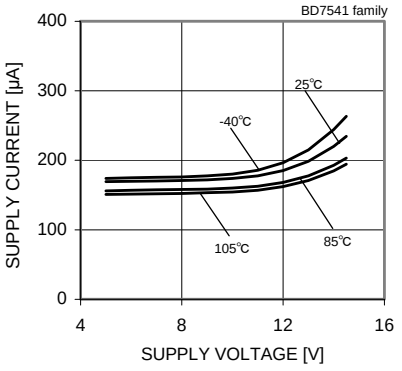


Fig. 49
Supply Current – Supply Voltage

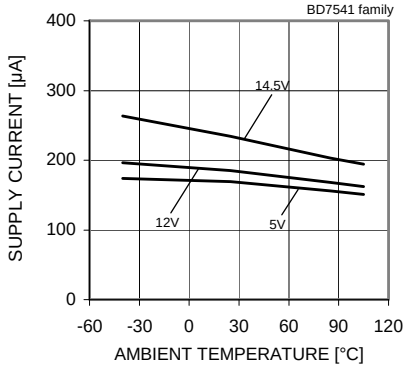


Fig. 50
Supply Current – Ambient Temperature

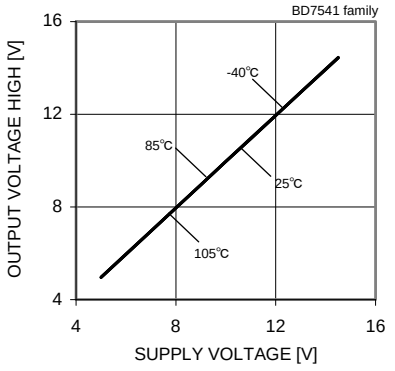


Fig. 51
Output Voltage High – Supply Voltage
(RL=10[kΩ])

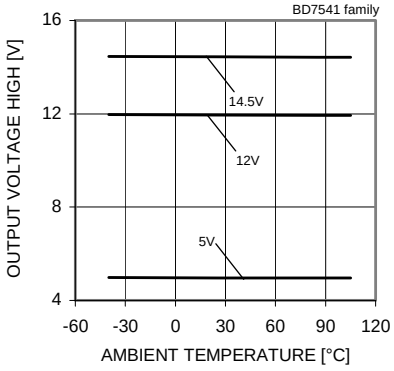


Fig. 52
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

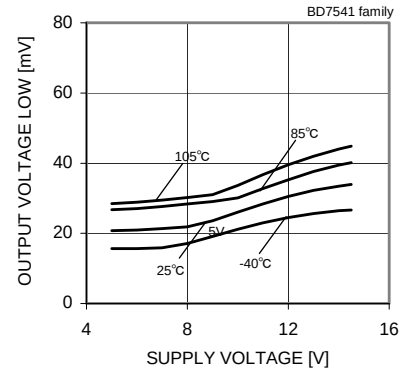


Fig. 53
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

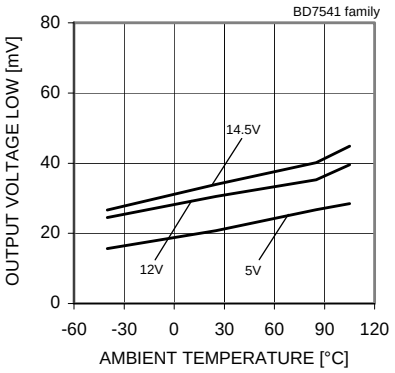


Fig. 54
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

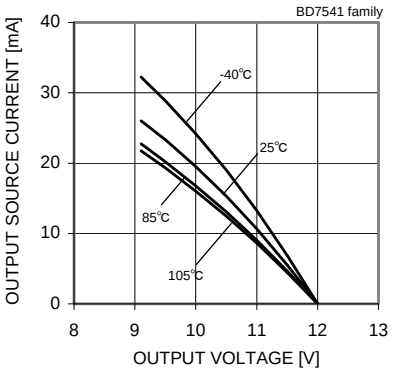


Fig. 55
Output Source Current – Output Voltage
(VDD=12[V])

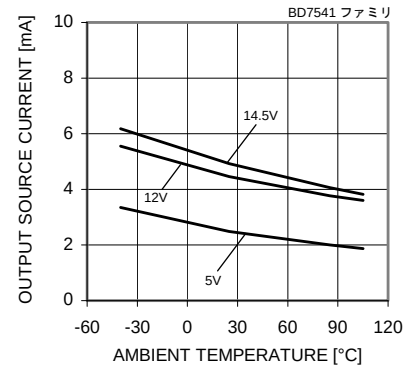


Fig. 56
Output Source Current – Ambient Temperature

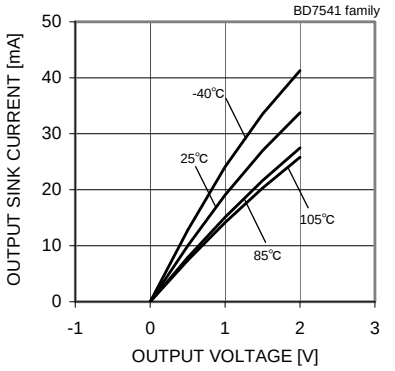


Fig. 57
Output Sink Current – Output Voltage
(VDD=12[V])

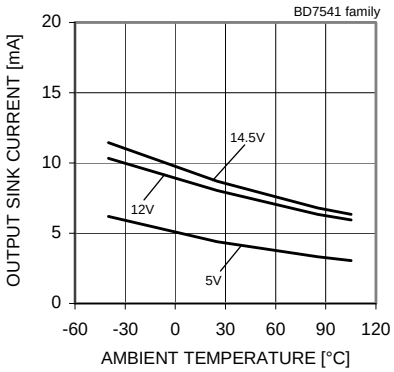


Fig. 58
Output Sink Current – Ambient Temperature
(VOUT=VDD-11.6[V])

(＊)The above data is ability value of sample, it is not guaranteed. BD7541 : -40[℃]～+85[℃]　BD7541S : -40[℃]～+105[℃]

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○BD7541 family

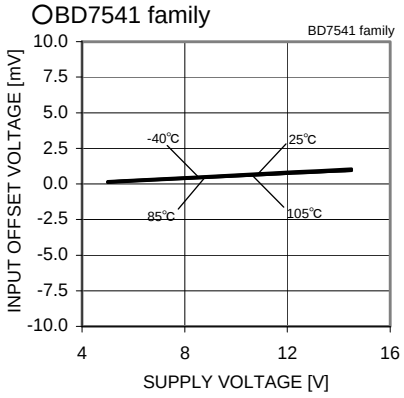


Fig. 59
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=VDD/2)

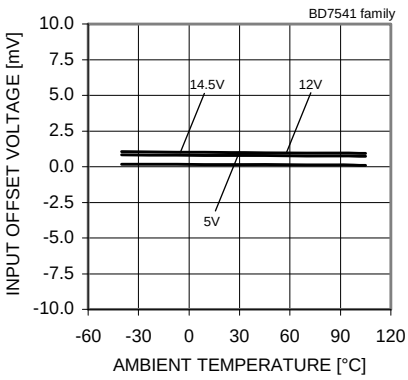


Fig. 60
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=VDD/2)

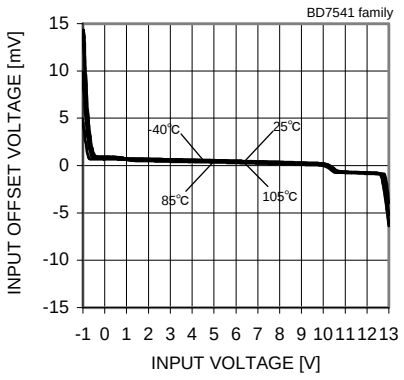


Fig. 61
Input Offset Voltage – Input Voltage
(VDD=12[V])

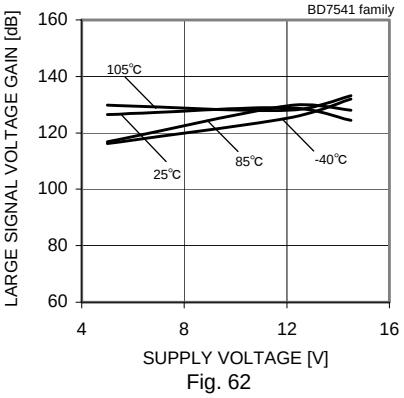


Fig. 62
Large Signal Voltage Gain
– Supply Voltage

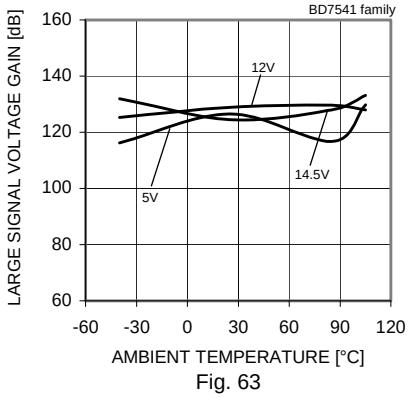


Fig. 63
Large Signal Voltage Gain
– Ambient Temperature

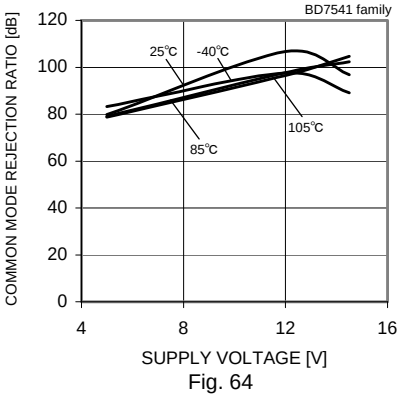


Fig. 64
Common Mode Rejection Ratio
– Supply Voltage
(VDD=12[V])

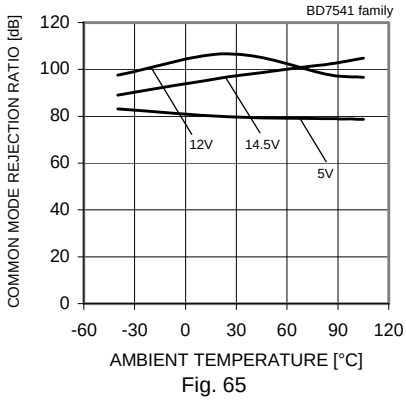


Fig. 65
Common Mode Rejection Ratio
– Ambient Temperature
(VDD=12[V])

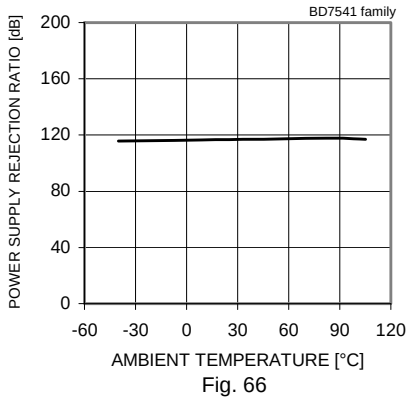


Fig. 66
Power Supply Rejection Ratio
– Ambient Temperature

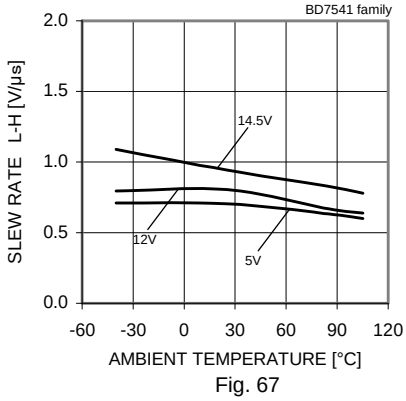


Fig. 67
Slew Rate L-H – Ambient Temperature

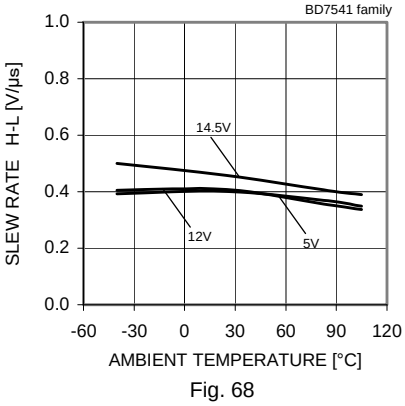


Fig. 68
Slew Rate H-L – Ambient Temperature

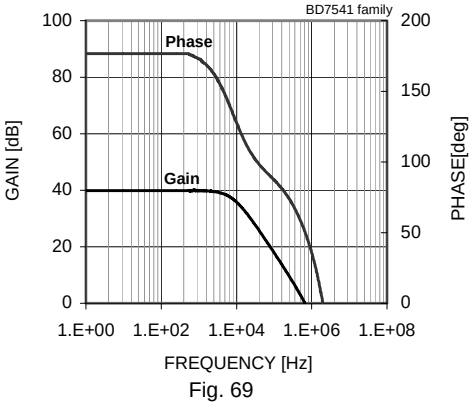


Fig. 69
Gain - Frequency

(＊)The above data is ability value of sample, it is not guaranteed. BD7541：-40[℃]～+85[℃] BD7541S：-40[℃]～+105[℃]

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○BD7542 family

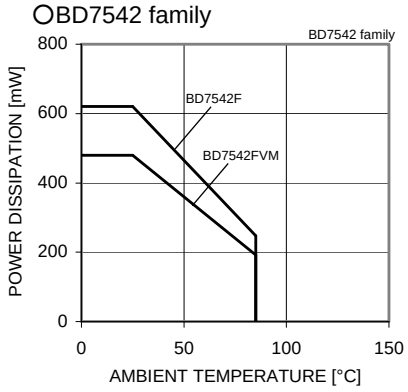


Fig. 70
Derating Curve

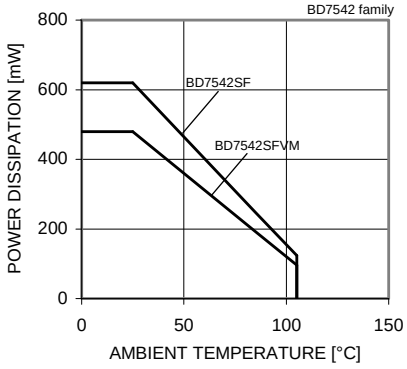


Fig. 71
Derating Curve

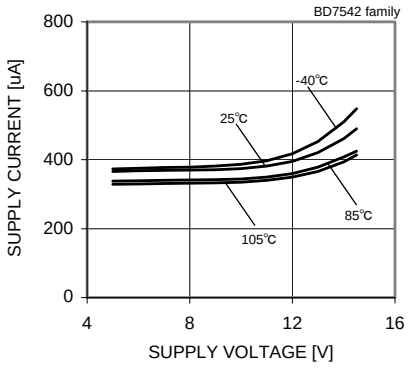


Fig. 72
Supply Current – Supply Voltage

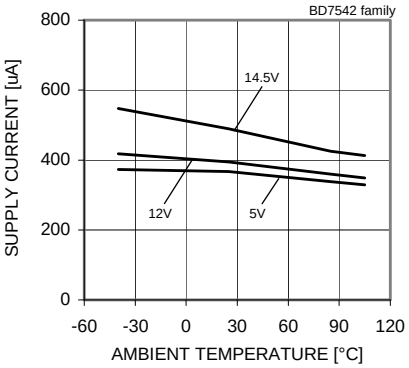


Fig. 73
Supply Current – Ambient Temperature

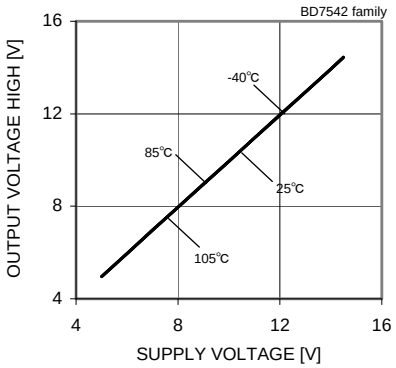


Fig. 74
Output Voltage High – Supply Voltage
(RL=10[kΩ])

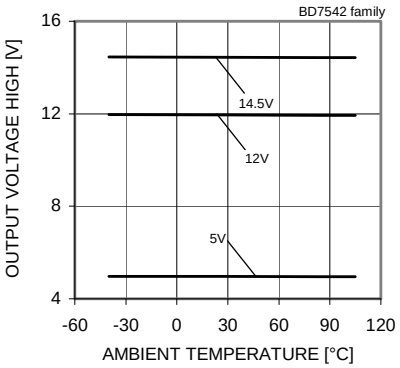


Fig. 75
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

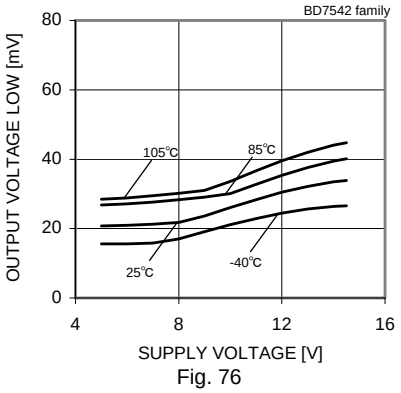


Fig. 76
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

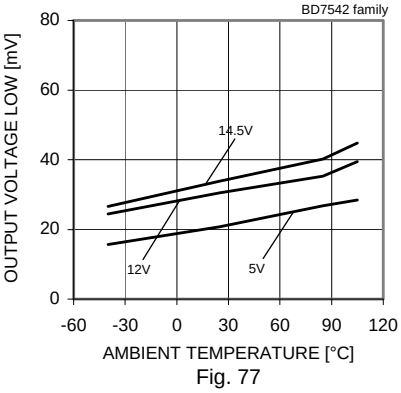


Fig. 77
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

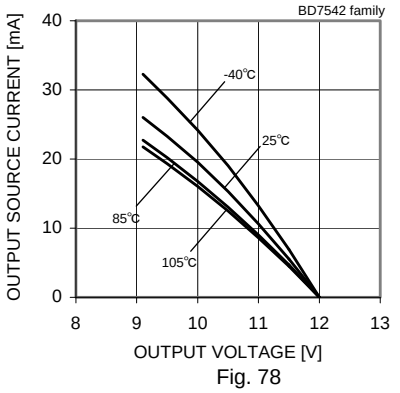


Fig. 78
Output Source Current – Output Voltage
(VDD=12[V])

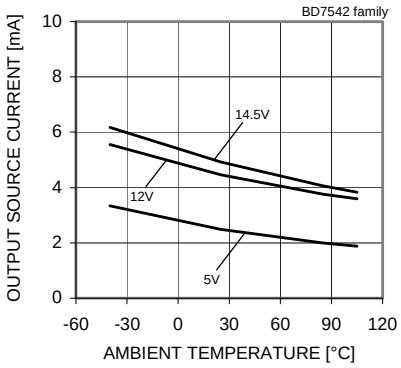


Fig. 79
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

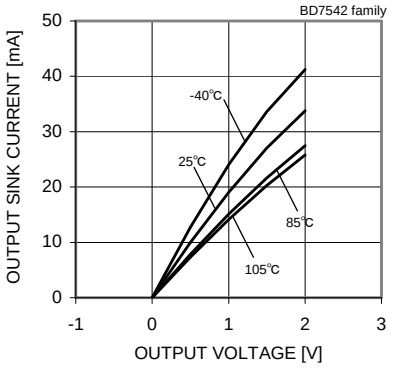


Fig. 80
Output Sink Current – Output Voltage
(VDD=12[V])

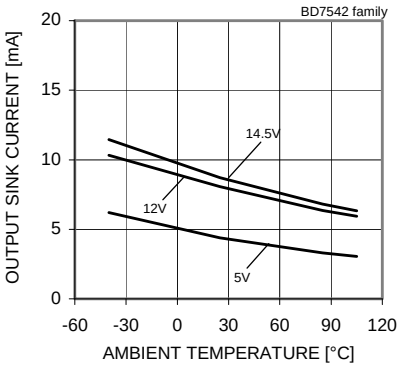


Fig. 81
Output Sink Current – Ambient Temperature
(VOUT=VDD-11.6[V])

(＊)The above data is ability value of sample, it is not guaranteed. BD7561：-40[℃]～+85[℃]　BD7561S：-40[℃]～+105[℃]

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○BD7542 family

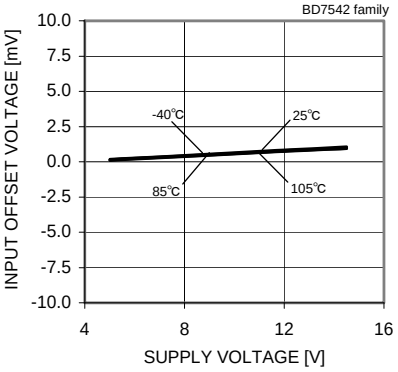


Fig. 82
Input Offset Voltage – Supply Voltage
(Vicm=VDD, VOUT=VDD/2)

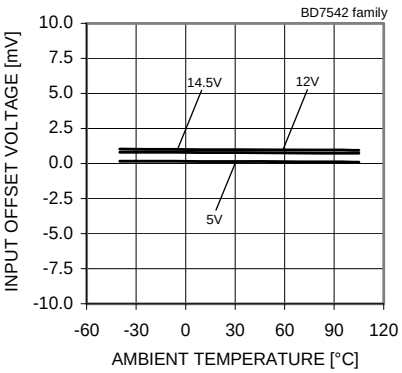


Fig. 83
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=VDD/2)

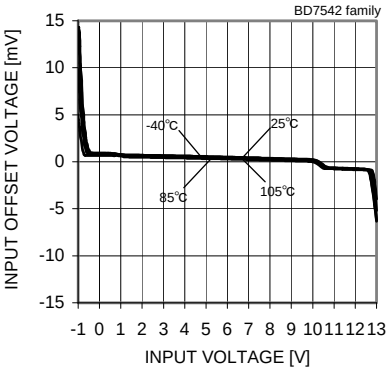


Fig. 84
Input Offset Voltage – Input Voltage
(VDD=12[V])

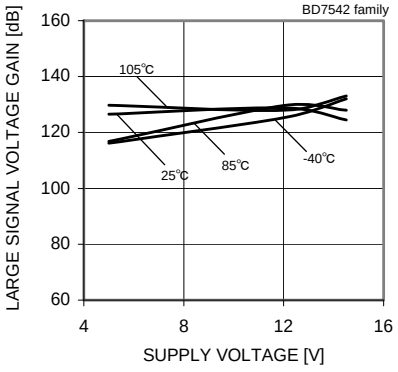


Fig. 85
Large Signal Voltage Gain
– Supply Voltage

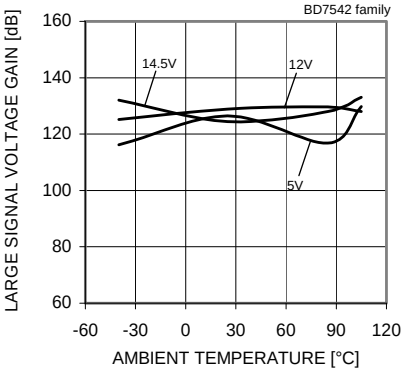


Fig. 86
Large Signal Voltage Gain
– Ambient Temperature

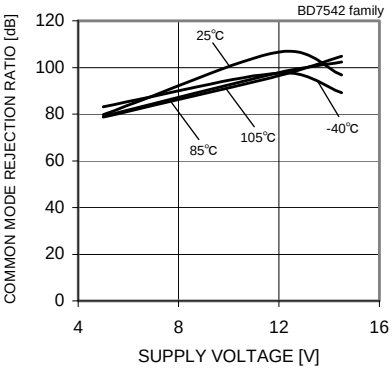


Fig. 87
Common Mode Rejection Ratio
– Supply Voltage
(VDD=12[V])

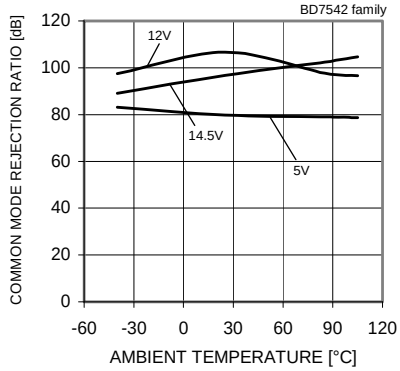


Fig. 88
Common Mode Rejection Ratio
– Ambient Temperature
(VDD=12[V])

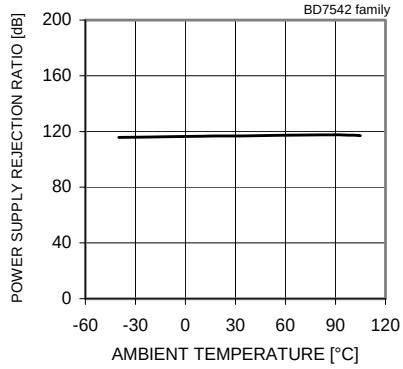


Fig. 89
Power Supply Rejection Ratio
– Ambient Temperature

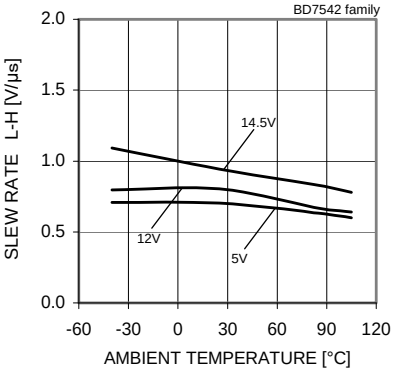


Fig. 90
Slew Rate L-H – Ambient Temperature

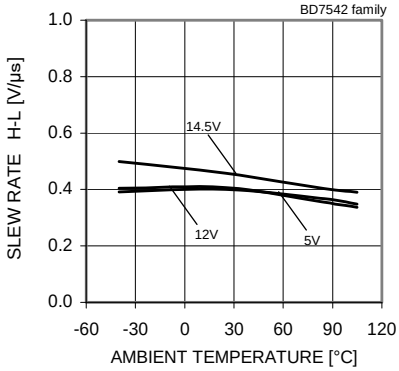


Fig. 91
Slew Rate H-L – Ambient
Temperature

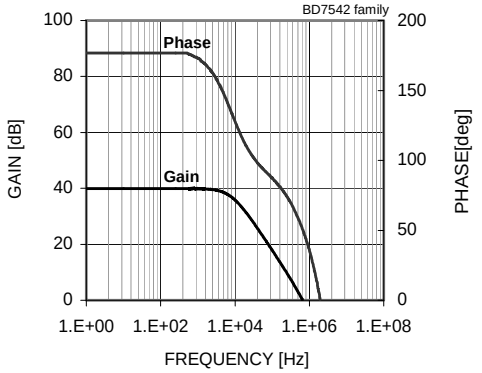


Fig. 92
Gain - Frequency

(＊)The above data is ability value of sample, it is not guaranteed. BD7561：-40[℃]～+85[℃] BD7561S：-40[℃]～+105[℃]

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●Schematic diagram

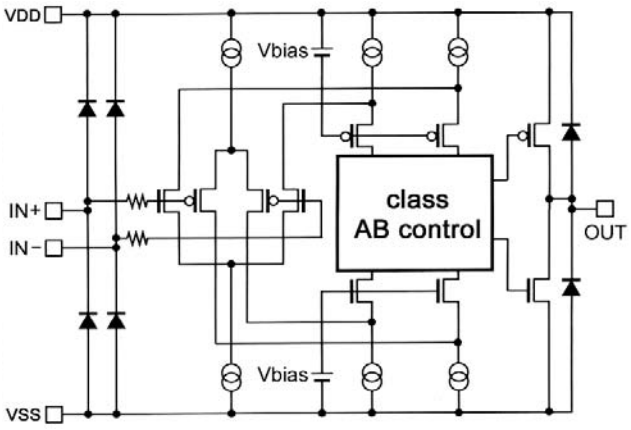


Fig. 93. Schematic diagram

●Test circuit1 NULL method
VDD,VSS,EK,Vicm Unit : [V]

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation
Input Offset Voltage	VF1	ON	ON	OFF	12	0	-6	12	1
Large Signal Voltage Gain	VF2	ON	ON	ON	12	0	-0.5	6	2
	VF3						-11.5		
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF4	ON	ON	OFF	12	0	-6	0	3
	VF5							12	
Power Supply Rejection Ratio	VF6	ON	ON	OFF	5	0	-2.5	0	4
	VF7				14.5				

-Calculation-

1. Input Offset Voltage (Vio) $$Vio = \frac{|VF1|}{1+Rf/Rs} \ [V]$$

2. Large Signal Voltage Gain (Av) $$Av = 20Log\frac{2\times(1+Rf/Rs)}{|VF2-VF3|} \ [dB]$$

3. Common-mode Rejection Ratio (CMRR) $$CMRR = 20Log\frac{1.8\times(1+Rf/Rs)}{|VF4-VF5|} \ [dB]$$

4. Power Supply Rejection Ratio (PSRR) $$PSRR = 20Log\frac{3.8\times(1+Rf/Rs)}{|VF6-VF7|} \ [dB]$$

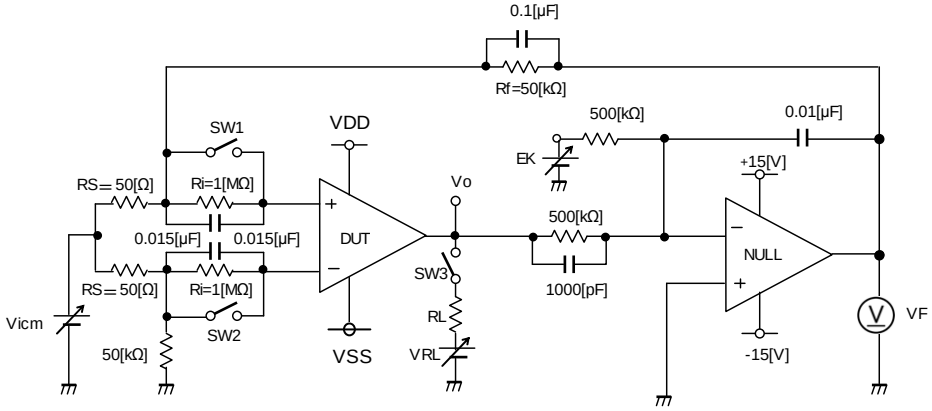


Fig. 94. Test circuit 1 (one channel only)

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●Test circuit2 switch condition

Unit : [V]

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage RL=10 [kΩ]	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Maximum Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

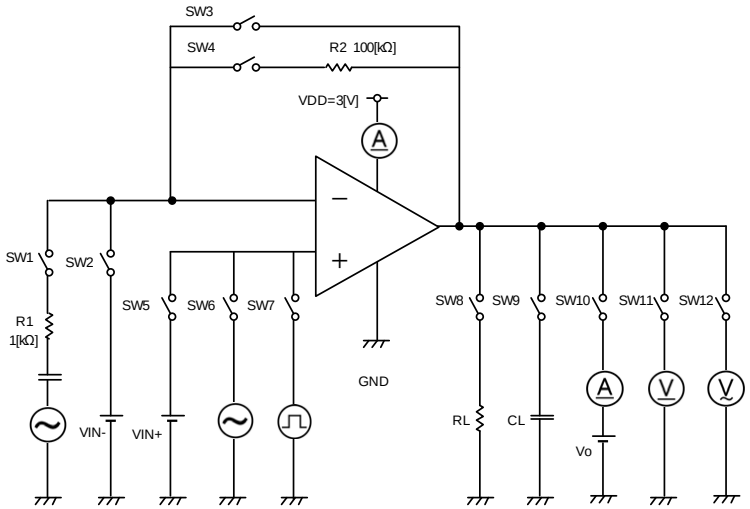


Fig. 95.. Test circuit2

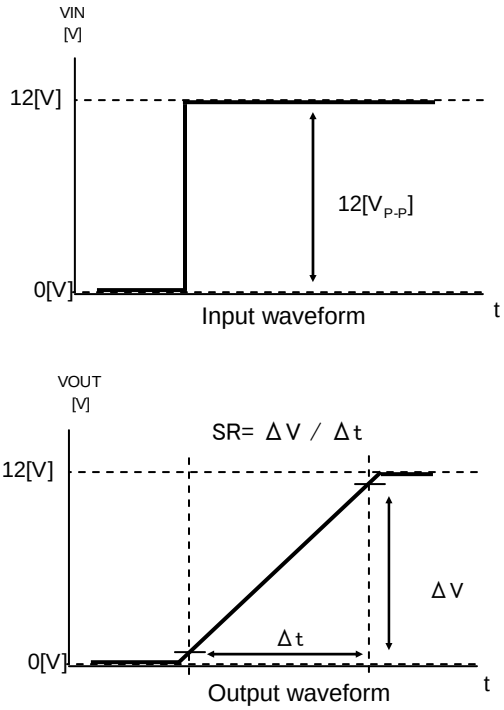


Fig. 96.. Slew rate input output wave

●Test circuit3 Channel separation

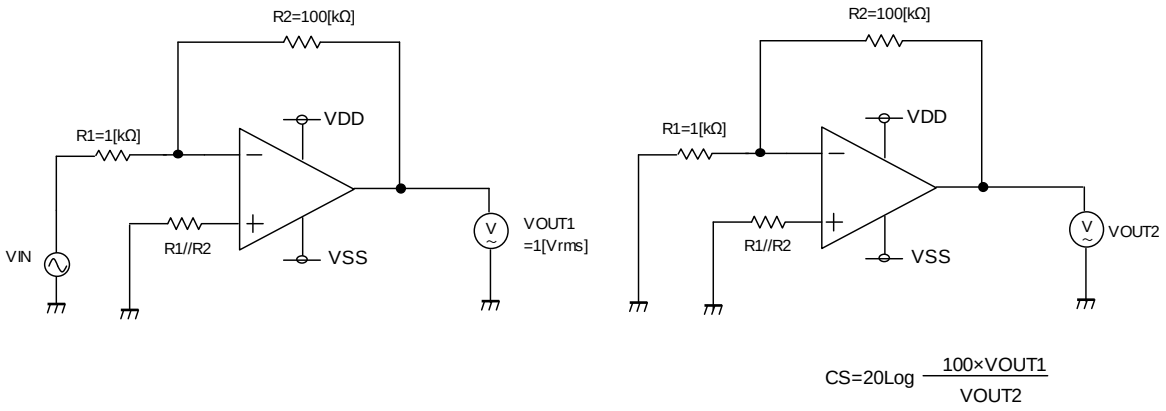


Fig. 97.. Test circuit3

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●Description of electrical characteristics

Described here are the terms of electric characteristics used in this technical note. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage (VDD/VSS)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminalwithout deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (Pd)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25℃(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package(maximum junction temperature)and thermal resistance of the package.

2. Electrical characteristics item

2.1 Input offset voltage (Vio)

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 [V].

2.2 Input offset current (Iio)

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current (Ib)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Circuit current (ICC)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.5 High level output voltage / Low level output voltage(VOH/VOL)

Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into high-level output voltage and low-level output voltage. High-level output voltage indicates the upper limit of output voltage. Low-level output voltage indicates the lower limit.

2.6 Large signal voltage gain (AV)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal.It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage fluctuation) / (Input offset fluctuation)

2.7 Input common-mode voltage range (Vicm)

Indicates the input voltage range where IC operates normally.

2.8 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
CMRR ＝(Change of Input common-mode voltage)/(Input offset fluctuation)

2.9 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
PSRR＝(Change of power supply voltage)/(Input offset fluctuation)

2.10 Channel separation(CS)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

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2.11 Slew rate (SR)
Indicates the time fluctuation ratio of voltage output when step input signal is applied.

2.12 Unity gain frequency (ft)
Indicates a frequency where the voltage gain of Op-Amp is 1.

2.13 Total harmonic distortion + Noise (THD＋N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

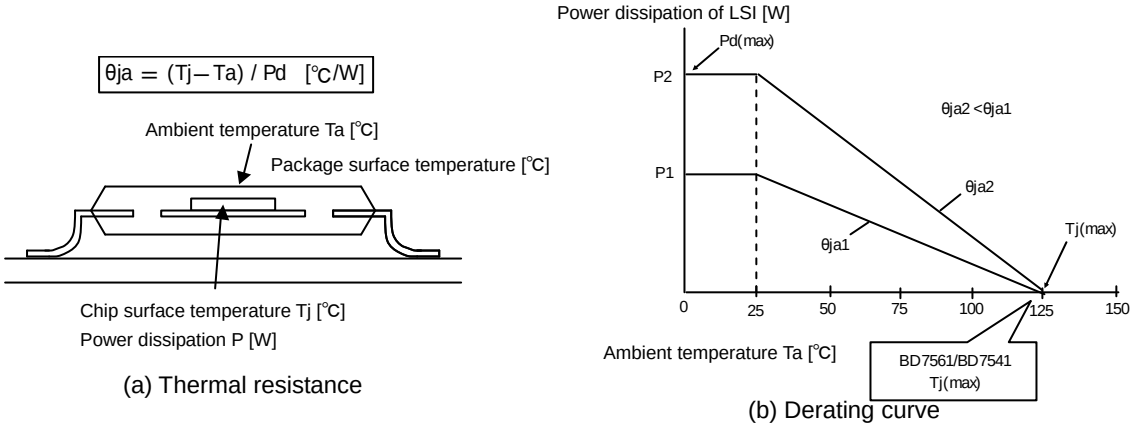
2.14 Input referred noise voltage (Vn)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

●Derating curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature).
IC is heatedwhen it consumed power, and the temperature of IC ship becomes higher than ambient temperature.
The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability).
The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability).
The maximum junction temperature is typically equal to the maximum value in the storage temperature range.
Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package.
The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θj-a[℃/W]. The temperature of IC inside the package can be estimated by this thermal resistance.
Fig.98 (a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below :

$$\theta ja = (Tj-Ta) / Pd \quad [℃/W] \qquad \cdots\cdots (I)$$

Derating curve in Fig.98 (b) indicates power that can be consumed by IC with reference to ambient temperature.
Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient iis determined by thermal resistance θja.
Thermal resistance θja depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used.
Thermal reduction curve indicates a reference value measured at a specified condition. Fig99(c)-(f) show a derating curve for an example of BU7561family, BU7562family, 7541family, 7542family.

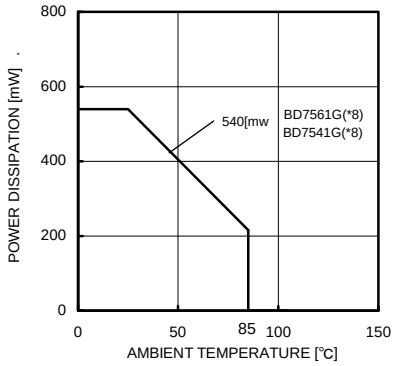


(a) Thermal resistance

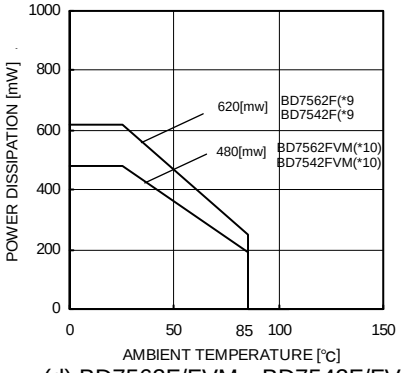
(b) Derating curve

Fig. 98. Thermal resistance and derating

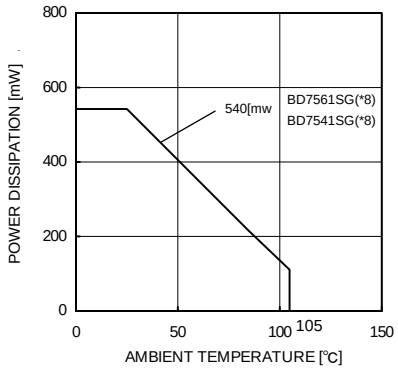
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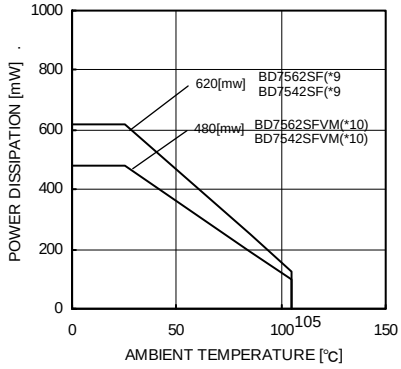
(c) BD7561G



(d) BD7562F/FVM BD7542F/FVM



(e) BD7561SG



(f) BD7562S F/FVM BD7542S F/FVM

(*8)	(*9)	(*10)	Unit
5.4	6.2	4.8	[mW/℃]

When using the unit above Ta=25[℃], subtract the value above per degree[℃]. Permissible dissipation is the value when FR4 glass epoxy board 70[mm] × 70[mm] × 1.6[mm] (cooper foil area below 3[%]) is mounted.

Fig. 99. Derating curve

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●N0tes for use

1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits,within which the given voltage range can be safely charged to the terminal.However, it does not guarantee the circuit operation.

2) Applied voltage to the input terminal
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage VDD+0.3[V].Then, regardless of power supply voltage,VSS-0.3[V] can be applied to inputterminals without deterioration or destruction of its characteristics.

3) Operating power supply (split power supply/single power supply)
The voltage comparator operates if a given level of voltage is applied between VDD and VSS. Therefore, the operational amplifier can be operated under single power supply or split power supply.

4) Power dissipation (Pd)
If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC. For example, reduction of current capability. Take consideration of the effective power dissipation andthermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.

5) Short circuits between pins and incorrect mounting
Short circuits between pins and incorrect mounting when mounting the IC on a printed circuits board, take notice of the direction and positioning of the IC.If IC is mounted erroneously, It may be damaged. Also, when a foreign object is inserted between output, between output and VDD terminal or VSS terminal which causes short circuit, the IC may be damaged.

6) Using under strong electromagnetic field
Be careful when using the IC under strong electromagnetic field because it may malfunction.

7) Usage of IC
When stress is applied to the IC through warp of the printed circuit board, The characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.

8) Testing IC on the set board
When testing IC on the set board, in cases where the capacitor is connected to the low impedance,make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress.
When removing IC from the set board, it is essential to cut supply voltage.As a countermeasure against the static electricity, observe proper grounding during fabrication processand take due care when carrying and storage it.

9) The IC destruction caused by capacitive load
The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor. When IC is used as a operational amplifier or as an application circuit,where oscillation is not activated by an output capacitor, the output capacitor must be kept below 0.1[μF] in order to prevent the damage mentioned above.

10) Decupling capacitor
Insert the deculing capacitance between VDD and VSS, for stable operation of operational amplifier.

11) Latch up
Be careful of input vltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation.
And protect the IC from abnormaly noise.

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●Ordering part number

B	D	7	5	6	2	F	V	M	-	T	R

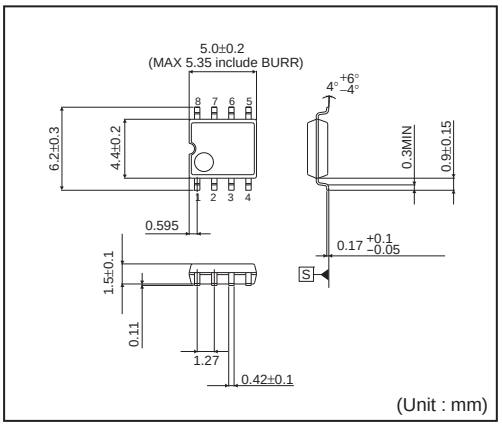
ローム形名

品番
7561 , 7561S
7541 , 7541S
7562 , 7562S
7542 , 7542S

パッケージ
G: SSOP5
F: SOP8
FVM: MSOP8

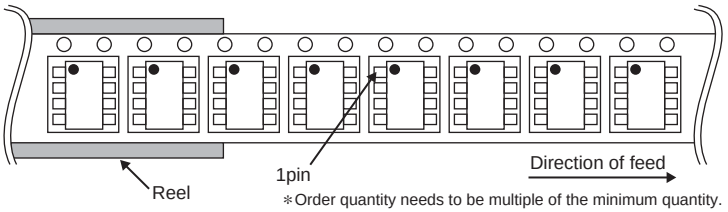
Packaging and forming specification
E2: Embossed tape and reel (SOP8)
TR: Embossed tape and reel (SSOP5/MSOP8)

SOP8



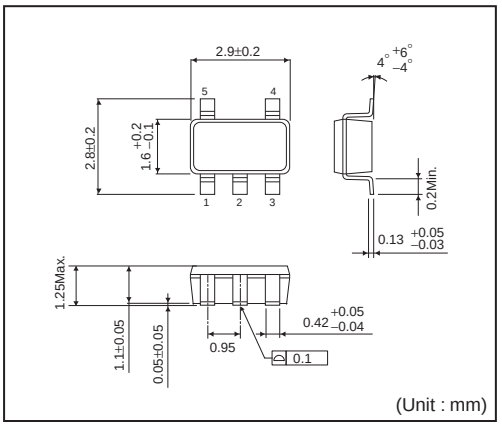
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



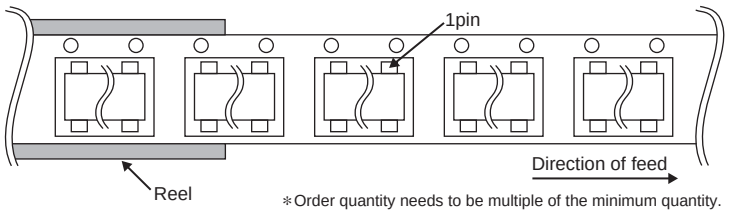
∗Order quantity needs to be multiple of the minimum quantity.

SSOP5



<Tape and Reel information>

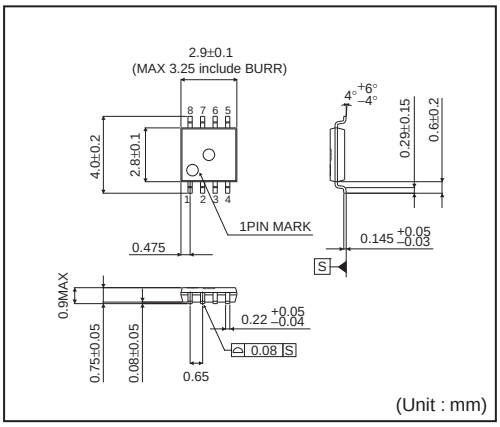
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

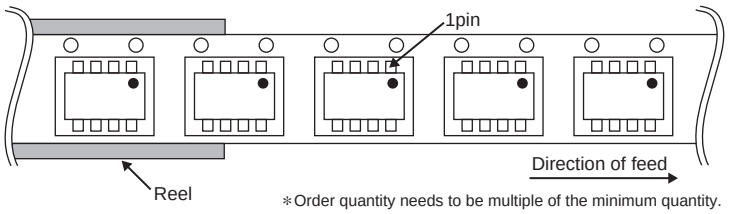
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MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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