TPS56x210A, 4.5-V to 17-V Input, 2-A, 3-A Synchronous Step-Down Voltage Regulator In 8-Pin SOT-23

1 Features

- TPS562210A: 2-A Converter With Integrated 133-mΩ and 80-mΩ FETs
- TPS563210A: 3-A Converter With Integrated 68-mΩ and 39-mΩ FETs
- D-CAP2™ Mode Control for Fast Transient Response
- Advanced Eco-mode™ Pulse-skip
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- 650-kHz Switching Frequency
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle By Cycle Over-current Limit
- Hiccup-mode Under Voltage Protection
- Non-latch OVP, UVLO and TSD Protections
- Adjustable Soft Start
- Power Good Output

2 Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

3 Description

The TPS562210A and TPS563210A are simple, easy-to-use, 2-A, 3-A synchronous step-down converters in 8 pin SOT-23 package.

The devices are optimized to operate with minimum external component counts and optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2™ mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

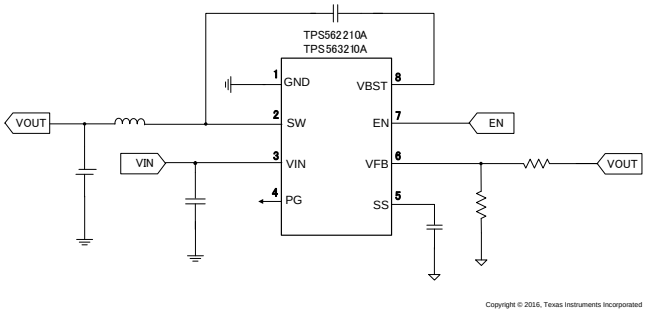
The devices operate in Advanced Eco-mode™, which maintains high efficiency during light load operation. The TPS562210A and TPS563210A are available in a 8-pin 1.6 × 2.9 (mm) SOT (DDF) package, and specified from –40°C to 85°C of ambient temperature.

Device Information(1)

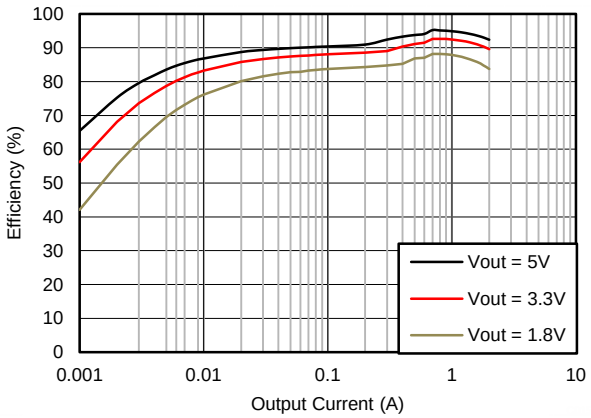
ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
TPS562210A	DDF(8)	1.60 mm × 2.90 mm
TPS563210A		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 5
6.7 Typical Characteristics ... 6
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 12
8 Application and Implementation ... 13
8.1 Application Information ... 13
8.2 Typical Application ... 13
9 Power Supply Recommendations ... 21
10 Layout ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 22
11 Device and Documentation Support ... 23
11.1 Device Support ... 23
11.2 Related Links ... 23
11.3 Receiving Notification of Documentation Updates 23
11.4 Community Resources ... 23
11.5 Trademarks ... 23
11.6 Electrostatic Discharge Caution ... 23
11.7 Glossary ... 23
12 Mechanical, Packaging, and Orderable Information ... 23

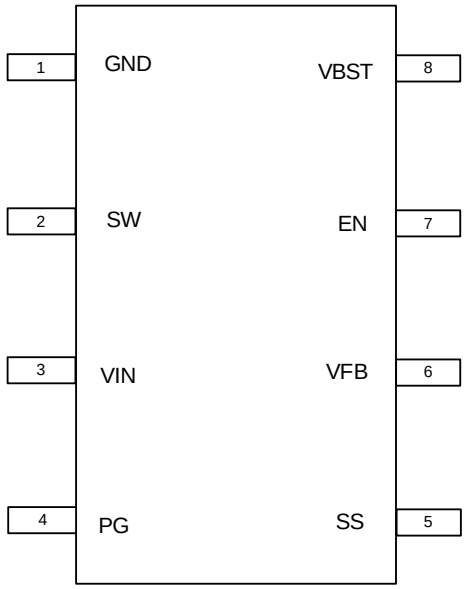
4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

Copyright © 2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

DDF Package
8 Pin
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
PG	4	Power good open drain output
SS	5	Soft-start control. An external capacitor should be connected to GND.
VFB	6	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	7	Enable input control. Active high and must be pulled up to enable the device.
VBST	8	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.

Copyright © 2016, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

T_J = -40°C to 150°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27.5	V
	VBST (vs SW)	–0.3	6.5	V
	VFB, PG	–0.3	6.5	V
	SS	–0.3	5.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_J = –40°C to 150°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	17	V
V_I	Input voltage range	VBST	–0.1	23	V
		VBST (10 ns transient)	–0.1	26	V
		VBST(vs SW)	–0.1	6	V
		EN	–0.1	17	V
		VFB, pg	–0.1	5.5	V
		SS	–0.1	5	V
		SW	–1.8	17	V
		SW (10 ns transient)	–3.5	20	V
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS562210A	TPS563210A	UNIT
		DDF (8 PINS)		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.1	87.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.1	41.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.9	14.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.6	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.8	14.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2016, Texas Instruments Incorporated

6.5 Electrical Characteristics

over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V		190	290	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.0	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage TPS562210A	T_A = 25°C, V_O = 1.05 V, I_O = 10 mA, Eco-mode™ operation		772		mV
	V_{FB} threshold voltage TPS562210A and TPS563210A	T_A = 25°C, V_O = 1.05 V	758	765	772	mV
		T_A = 0°C to 85°C, V_O = 1.05 V(1)	753		777	
		T_A = -40°C to 85°C, V_O = 1.05 V(1)	751		779	
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
MOSFET						
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V, TPS562210A		133		mΩ
		T_A = 25°C, V_{BST} – SW = 5.5 V, TPS563210A		68		
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C, TPS562210A		80		mΩ
		T_A = 25°C, TPS563210A		39		
CURRENT LIMIT						
I_{OCL}	Current limit(1)	DC current, V_{OUT} = 1.05 V , L1 = 2.2 µH, TPS562210A	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V , L1 = 1.5 µH, TPS563210A	3.5	4.2	5.3	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		155		°C
		Hysteresis		35		
SOFT START						
I_{SS}	SS charge current	V_{SS} = 1.2 V	4.2	6	7.8	µA
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (Good)	85%	90%	95%	
		V_{FB} falling (Fault)		85%		
I_{PG}	PG sink current	PG = 0.5 V	0.5	1		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP Detect		125%x Vfbth		
V_{UVP}	Output UVP threshold	Hiccup detect		65%x Vfbth		
$t_{HiccupOn}$	Hiccup Power On Time	Relative to soft start time		1		cycle
$t_{HiccupOff}$	Hiccup Power Off Time	Relative to soft start time		7		cycles
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage	3.45	3.75	4.05	V
		Hysteresis VIN voltage	0.13	0.32	0.55	

(1) Not production tested.

6.6 Timing Requirements

			MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.5 V		260	310	ns

Copyright © 2016, Texas Instruments Incorporated

6.7 Typical Characteristics

6.7.1 TPS562210A Characteristics

V_{IN} = 12 V (unless otherwise noted)

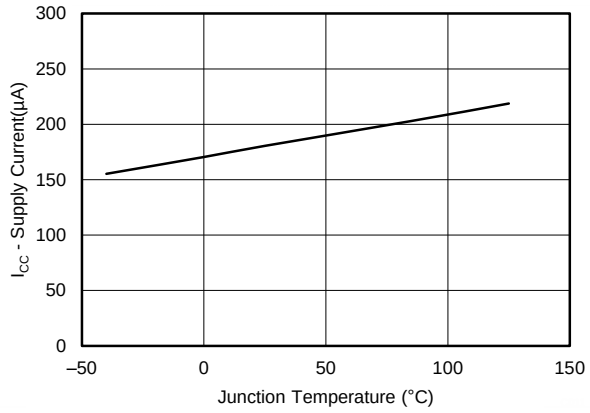


Figure 1. Supply Current vs Junction Temperature

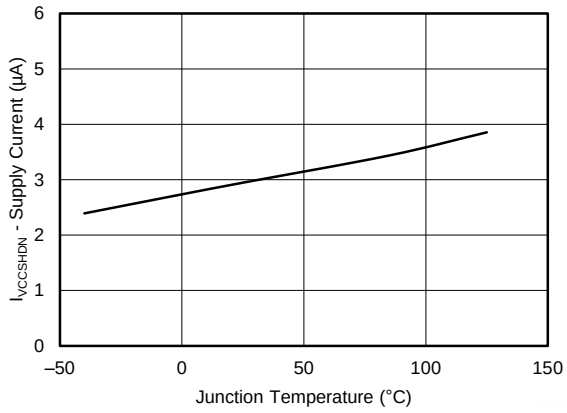


Figure 2. VIN Shutdown Current vs Junction Temperature

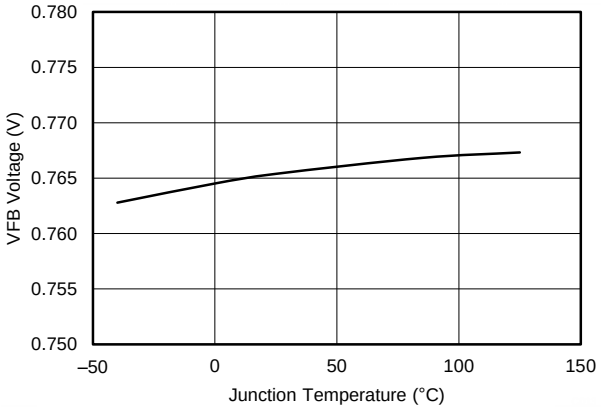


Figure 3. VFB Voltage vs Junction Temperature

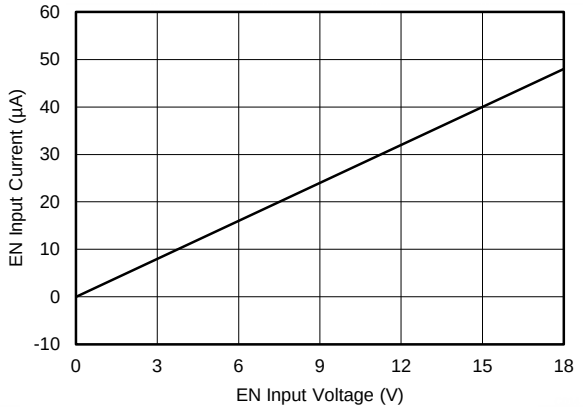


Figure 4. EN Current vs EN Voltage

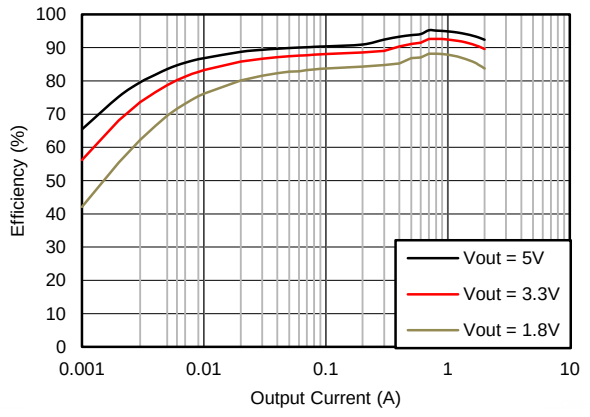
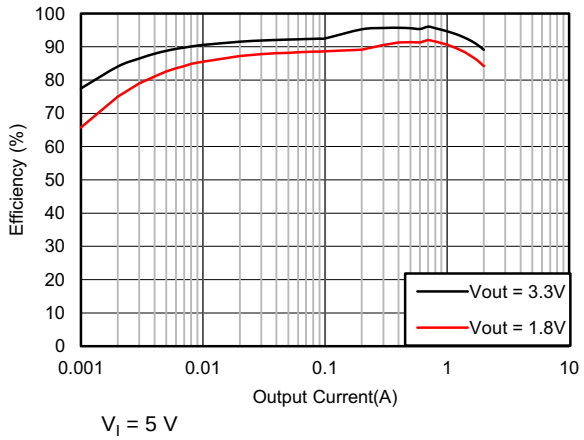


Figure 5. Efficiency vs Output Current



V_I = 5 V

Figure 6. Efficiency vs Output Current

Copyright © 2016, Texas Instruments Incorporated

TPS562210A Characteristics (continued)

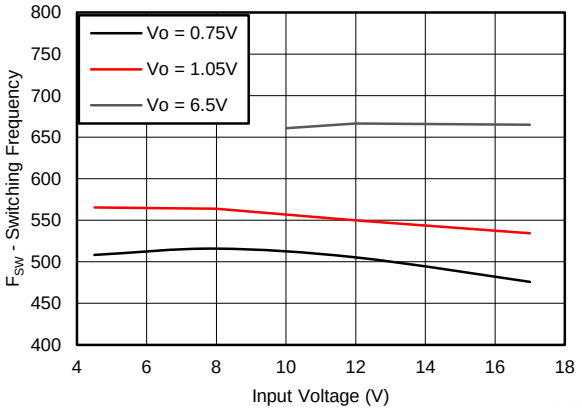


Figure 7. Switching Frequency vs Input Voltage

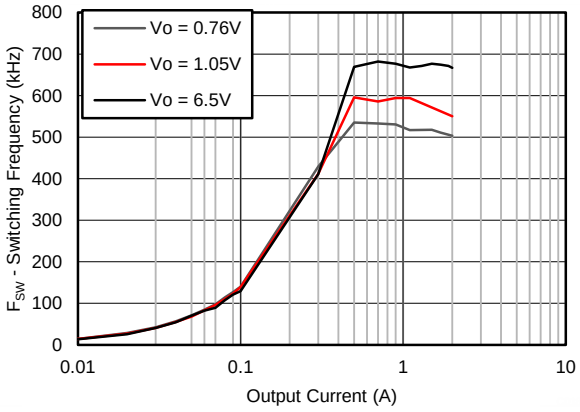


Figure 8. Switching Frequency vs Output Current

Copyright © 2016, Texas Instruments Incorporated

6.7.2 TPS563210A Characteristics

V_{IN} = 12V (unless otherwise noted)

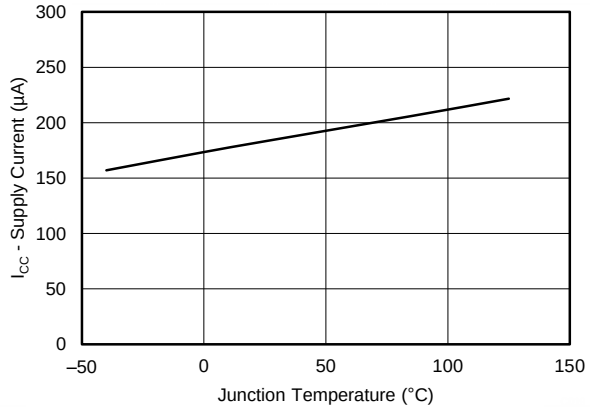


Figure 9. Supply Current vs Junction Temperature

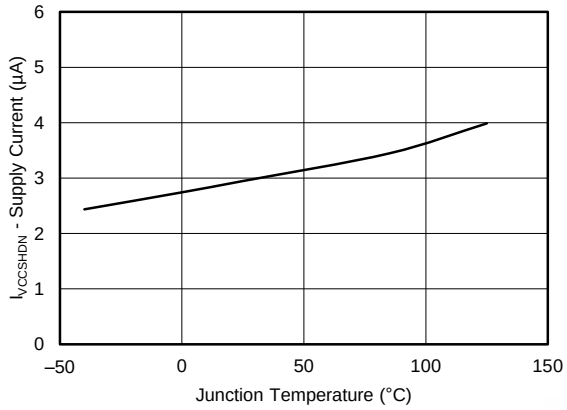


Figure 10. VIN Shutdown Current vs Junction Temperature

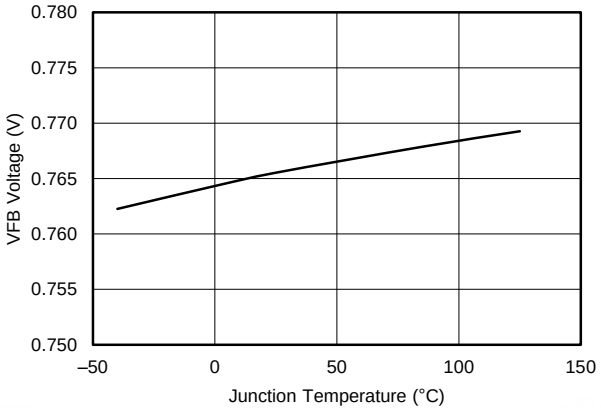


Figure 11. VFB Voltage vs Junction Temperature

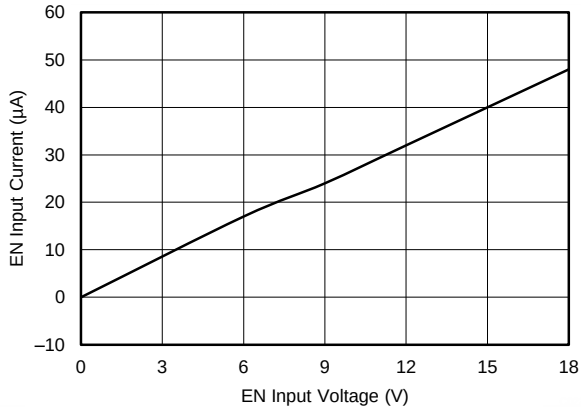


Figure 12. EN Current vs EN Voltage

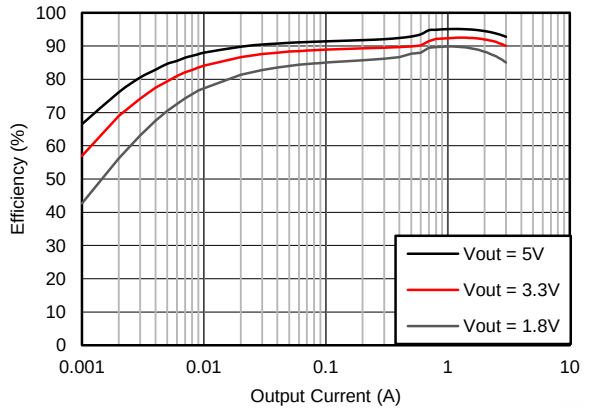
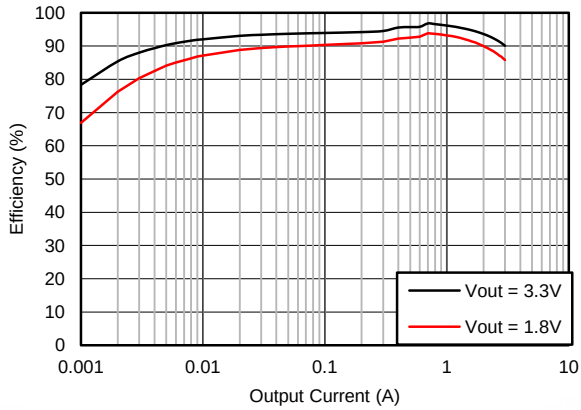


Figure 13. Efficiency vs Output Current



V_I = 5 V

Figure 14. Efficiency vs Output Current

Copyright © 2016, Texas Instruments Incorporated

TPS563210A Characteristics (continued)

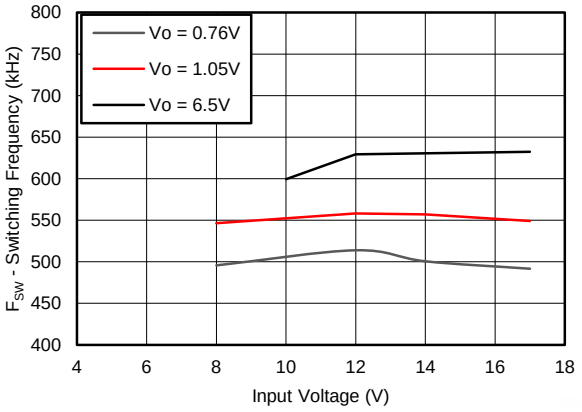


Figure 15. Switching Frequency vs Input Voltage

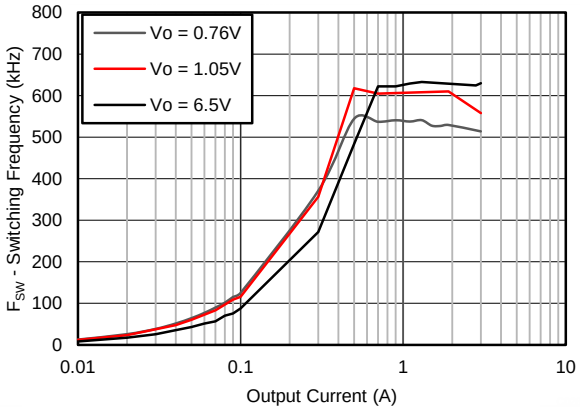


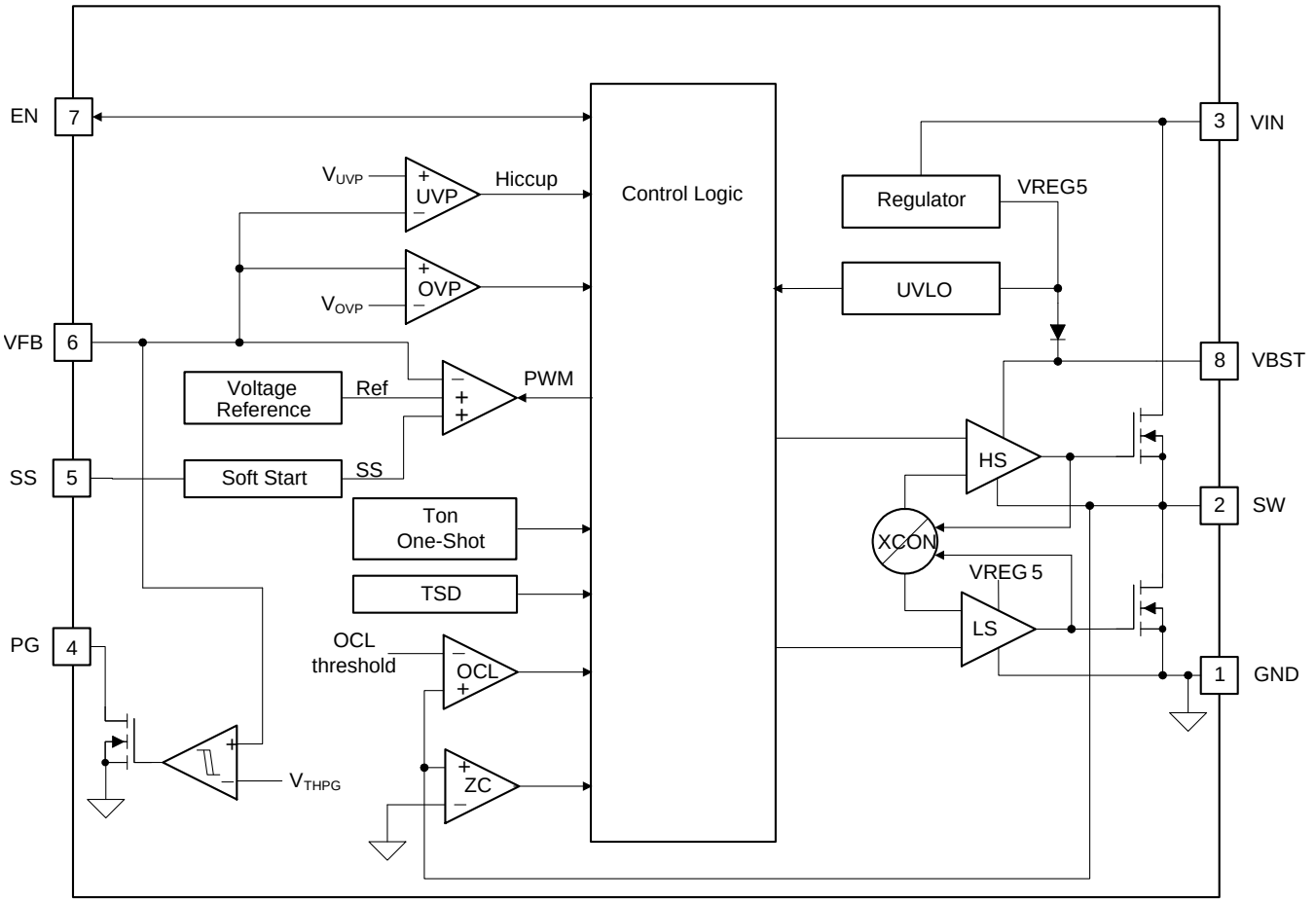
Figure 16. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS562210A and TPS563210A are 2-A, 3-A synchronous step-down converters. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS562210A and TPS563210A are adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, VIN, and inversely proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS562210A and TPS563210A have adjustable soft-start. When the EN pin becomes high, the SS charge current (I_{SS}) begins charging the capacitor which is connected from the SS pin to GND (C_{SS}). Smooth control of the output voltage is maintained during start up. The equation for the soft start time, Tss is shown in Equation 1.

$$Tss(ms) = \frac{Css \times V_{FBTH} \times 0.86}{Iss} \quad (1)$$

where V_{FBTH} is 0.765 V and Iss is 6 µA.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.3 Power Good

The power good output, PG is an open drain output. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

7.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 14 µs) and re-start after the hiccup time.

When the over current condition is removed, the output voltage returns to the regulated value.

Copyright © 2016, Texas Instruments Incorporated

Feature Description (continued)

7.3.5 Over Voltage Protection

TPS562210A and TPS563210A detect over voltage condition by monitoring the feedback voltage (VFB). When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the high-side MOSFET is turns off. This function is non-latch operation.

7.3.6 UVLO Protection

Under voltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.7 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Advanced Eco-Mode™ Control

The TPS562210A and TPS563210A are designed with Advanced Eco-mode™ to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

Copyright © 2016, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS562210A and TPS563210A are typically used as step down converters, which convert a voltage from 4.5 V to 17 V to a lower voltage. Webench software is available to aid in the design and analysis of circuits.

8.2 Typical Application

8.2.1 Typical Application, TPS562210A

4.5-V to 17-V Input, 1.05-V Output Converter.

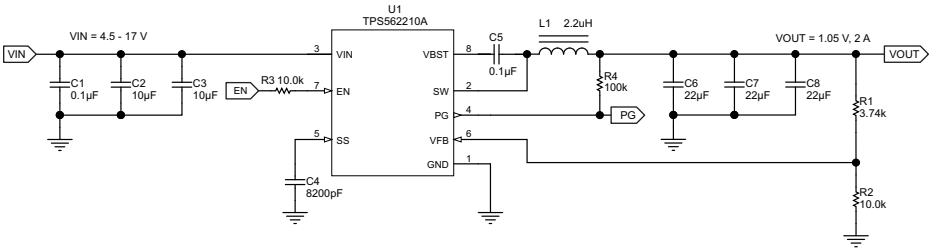


Figure 17. TPS562210A 1.05V/2A Reference Design

8.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 1.

Table 1. Design Parameters

PARAMETER	VALUES
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	2 A
Output voltage ripple	20 mVp-p

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 3 to calculate V_{OUT}.

To improve efficiency at light loads consider using larger value resistors, too high of resistance are more susceptible to noise and voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

8.2.1.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (4)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. TPS562210A Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1 (µH)			C6 + C7 + C8 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 - 68
1.05	3.74	10.0	1.5	2.2	4.7	20 - 68
1.2	5.76	10.0	1.5	2.2	4.7	20 - 68
1.5	9.53	10.0	1.5	2.2	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	2.2	3.3	4.7	20 - 68
3.3	33.2	10.0	2.2	3.3	4.7	20 - 68
5	54.9	10.0	3.3	4.7	4.7	20 - 68
6.5	75	10.0	3.3	4.7	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6 and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 6 and the RMS current of Equation 7.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (5)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (6)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (7)$$

For this design example, the calculated peak current is 2.34 A and the calculated RMS current is 2.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5 A and an RMS current rating of 4.3 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562210A and TPS563210A are intended for use with ceramic or other low ESR capacitors. Recommended values range from 20µF to 68µF. Use Equation 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (8)$$

For this design, two TDK C3216X5R0J226M 22 µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

8.2.1.2.3 Input Capacitor Selection

The TPS562210A and TPS563210A require an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Copyright © 2016, Texas Instruments Incorporated

8.2.1.2.4 Bootstrap capacitor Selection

A 0.1µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.1.3 Application Curves

The following application curves were generated using the application circuit of Figure 17.

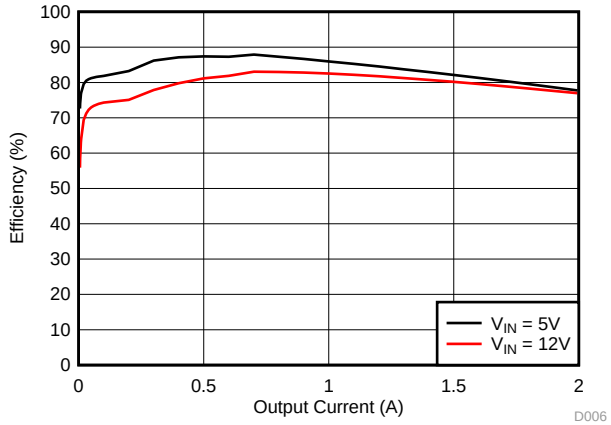


Figure 18. TPS562210A Efficiency

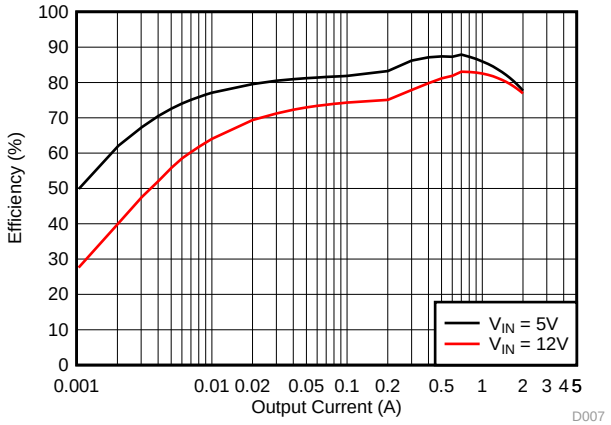


Figure 19. TPS562210A Light Load Efficiency

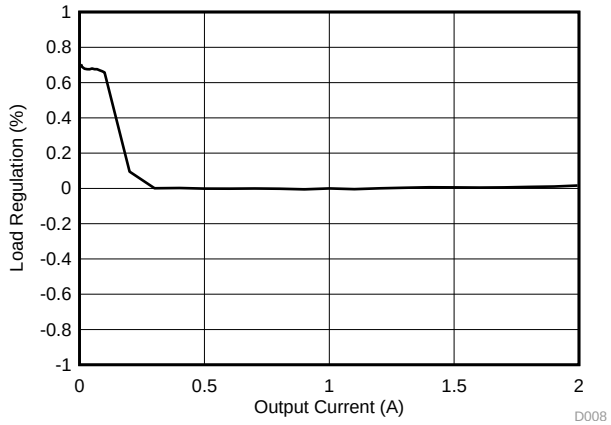


Figure 20. TPS562210A Load Regulation, V_I = 5 V

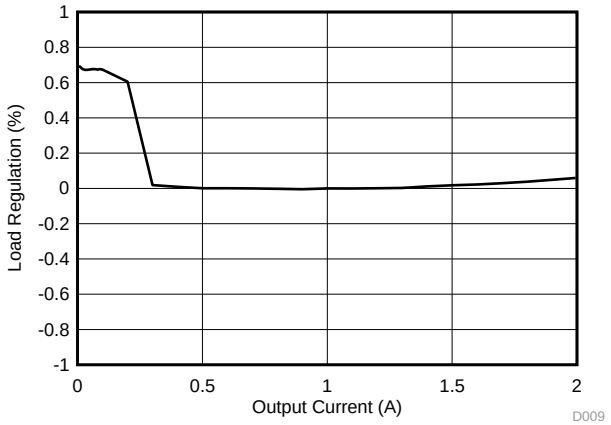


Figure 21. TPS562210A Load Regulation, V_I = 12 V

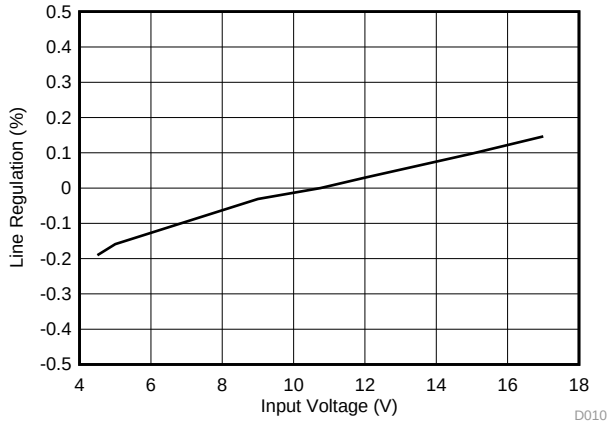


Figure 22. TPS562210A Line Regulation

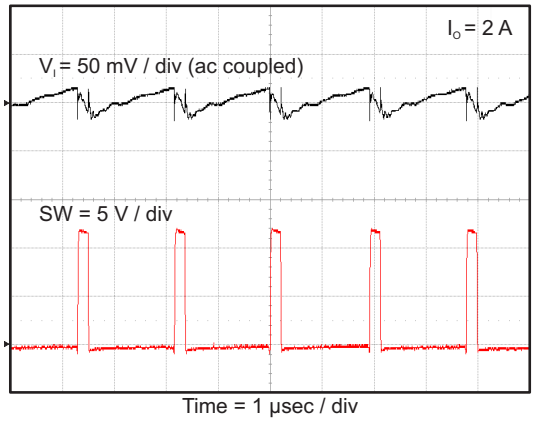


Figure 23. TPS562210A Input Voltage Ripple

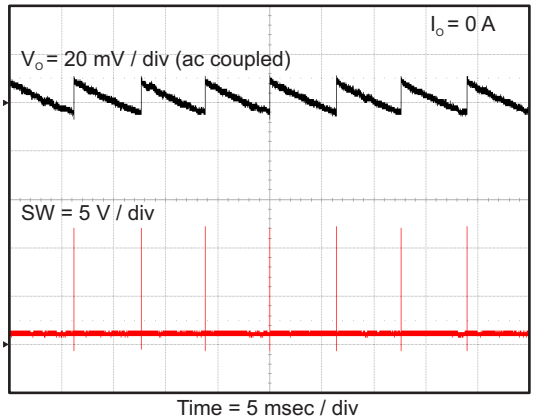


Figure 24. TPS562210A Output Voltage Ripple

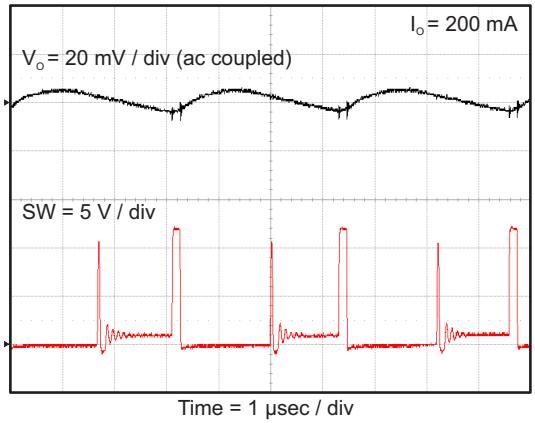


Figure 25. TPS562210A Output Voltage Ripple

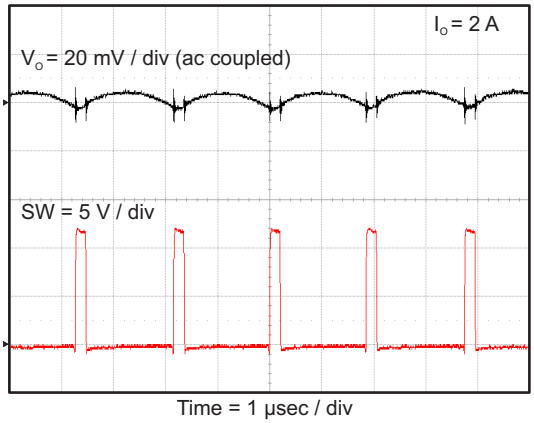


Figure 26. TPS562210A Output Voltage Ripple

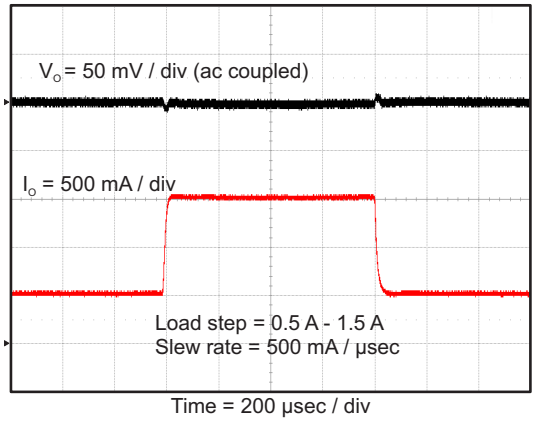


Figure 27. TPS562210A Transient Response

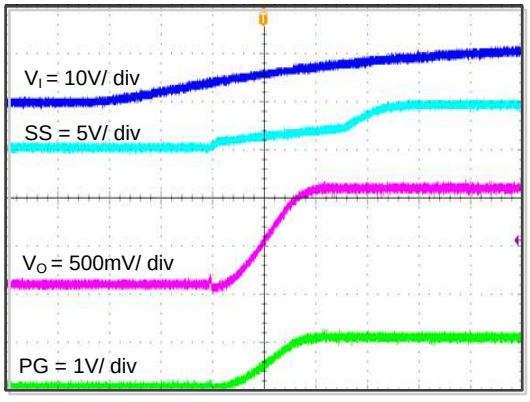


Figure 28. TPS562210A Start Up Relative To V_I

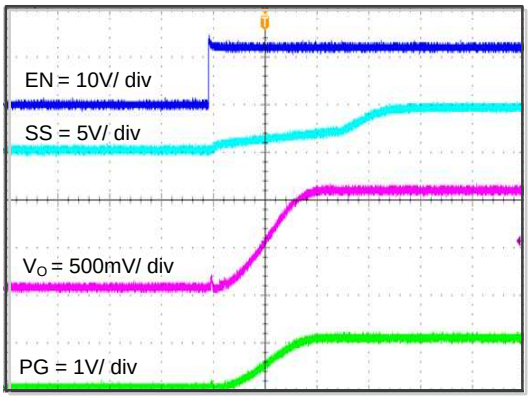


Figure 29. TPS562210A Start Up Relative To En

Copyright © 2016, Texas Instruments Incorporated

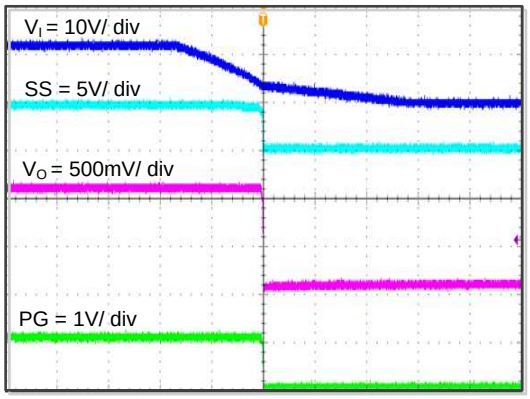


Figure 30. TPS562210A Shut Down Relative To V_I

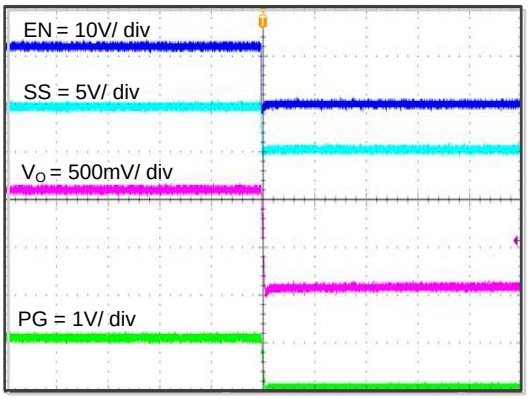


Figure 31. TPS562210A Shut Down Relative To EN

8.2.2 Typical Application, TPS563210A

4.5-V To 17-V Input, 1.05-V Output Converter.

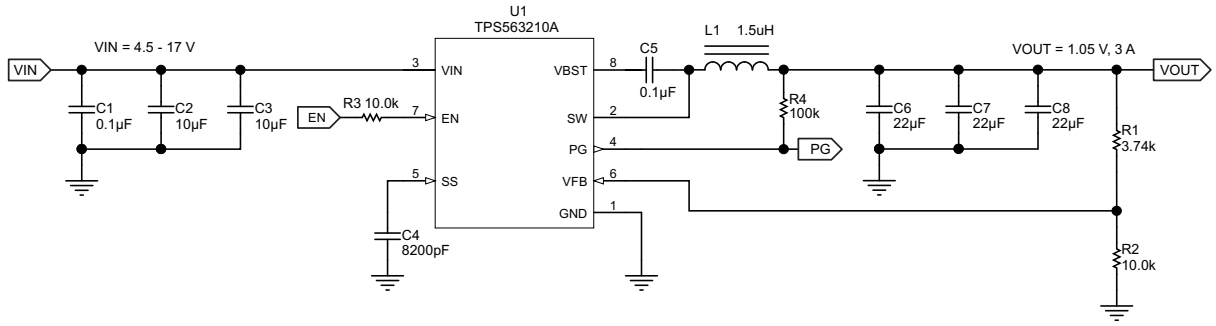


Figure 32. TPS563210A 1.05 V / 3A Reference Design

8.2.2.1 Design Requirements

For this design example, use the parameters shown in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	3 A
Output voltage ripple	20 mVpp

8.2.2.2 Detailed Design Procedures

The detailed design procedure for TPS563210A is the same as for TPS562210A except for inductor selection.

8.2.2.2.1 Output Filter Selection

Table 4. TPS563210A Recommended Component Values

Output Voltage (V)	R2 (kΩ)	R3 (kΩ)	L1 (µH)			C6 + C7 + C8 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.0	1.5	4.7	20 - 68
1.05	3.74	10.0	1.0	1.5	4.7	20 - 68
1.2	5.76	10.0	1.0	1.5	4.7	20 - 68
1.5	9.53	10.0	1.0	1.5	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	1.5	2.2	4.7	20 - 68
3.3	33.2	10.0	1.5	2.2	4.7	20 - 68
5	54.9	10.0	2.2	3.3	4.7	20 - 68
6.5	75	10.0	2.2	3.3	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 9, Equation 10 and Equation 11. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 10 and the RMS current of Equation 11.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (9)$$

Copyright © 2016, Texas Instruments Incorporated

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (10)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (11)$$

For this design example, the calculated peak current is 3.505 A and the calculated RMS current is 3.014 A. The inductor used is a TDK CLF7045T-1R5N with a peak current rating of 7.3-A and an RMS current rating of 4.9-A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563209 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor. For this design three TDK C3216X5R0J226M 22 µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.292A and each output capacitor is rated for 4 A.

8.2.2.3 Application Curves

The following application curves were generated using the application circuit of Figure 32.

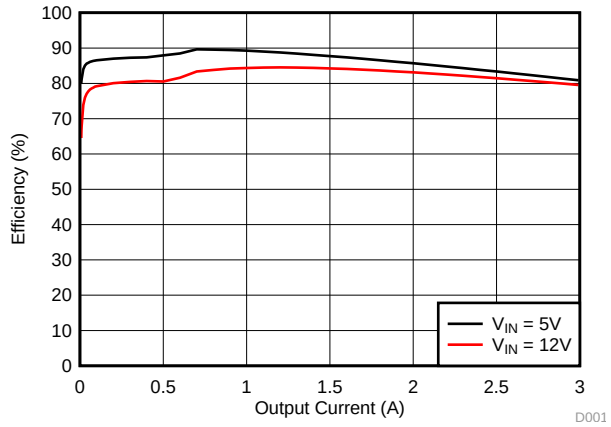


Figure 33. TPS563210A Efficiency

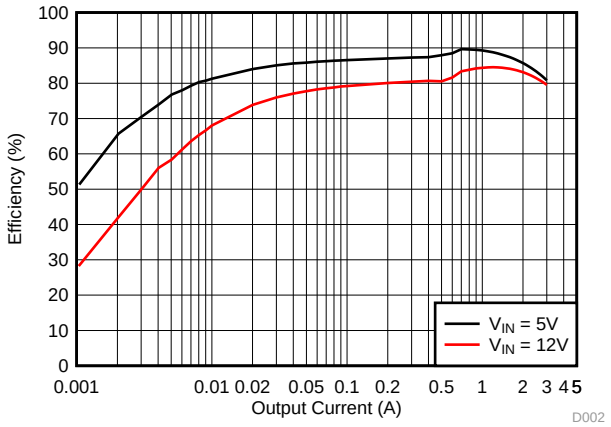


Figure 34. TPS563210A Light Load Efficiency

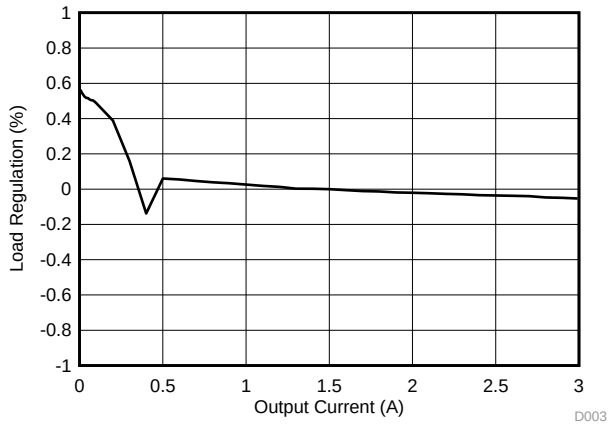


Figure 35. TPS563210A Load Regulation, V_I = 5 V

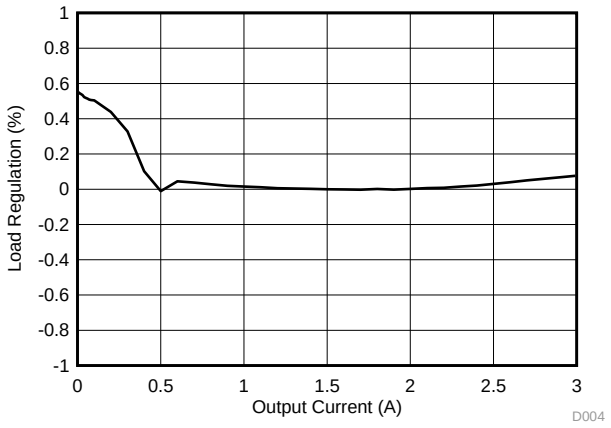


Figure 36. TPS563210A Load Regulation, V_I = 12 V

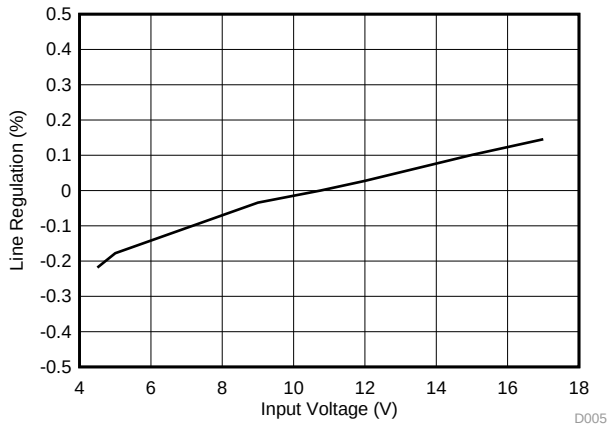


Figure 37. TPS563210A Line Regulation

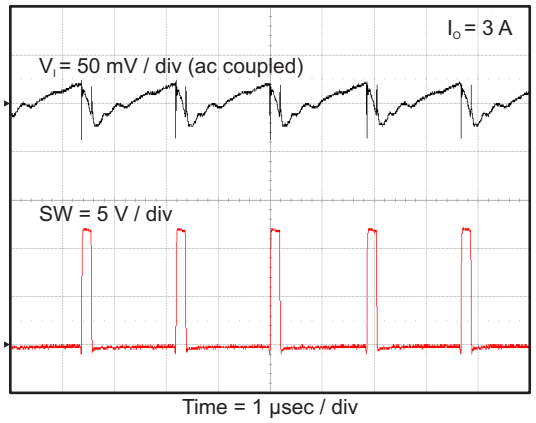


Figure 38. TPS563210A Input Voltage Ripple

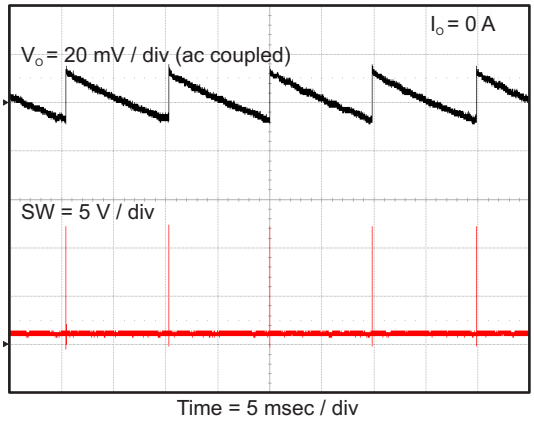


Figure 39. TPS563210A Output Voltage Ripple

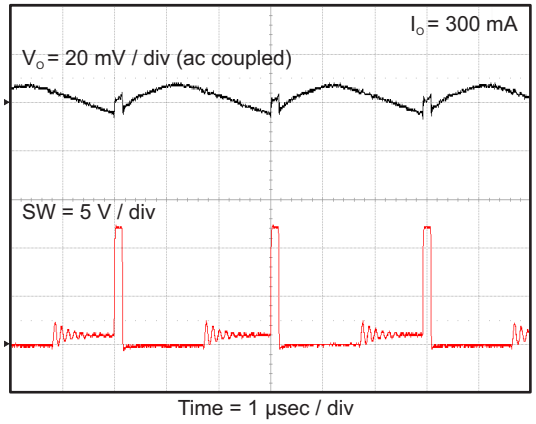


Figure 40. TPS563210A Output Voltage Ripple

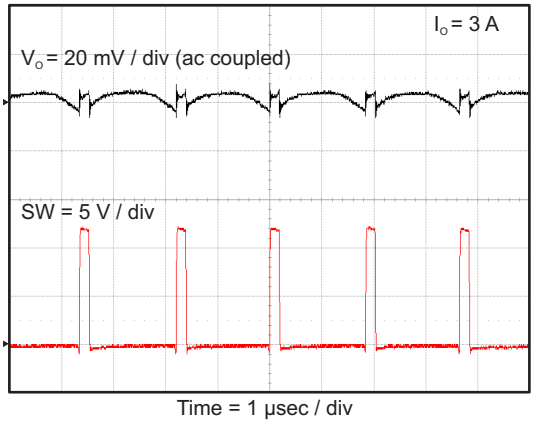


Figure 41. TPS563210A Output Voltage Ripple

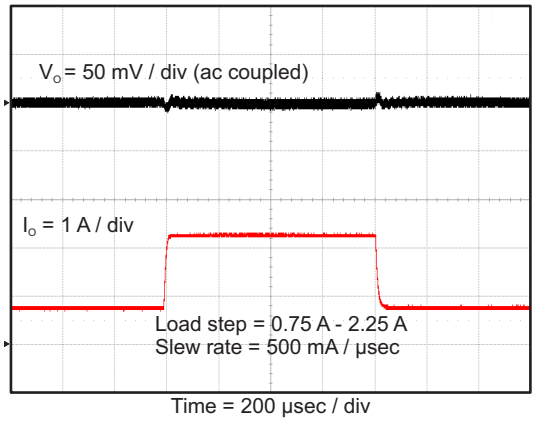
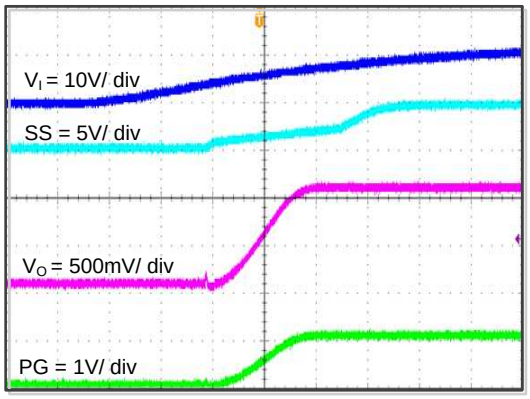


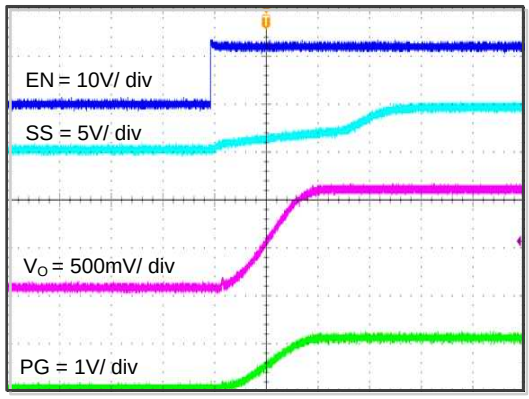
Figure 42. TPS563210A Transient Response

Copyright © 2016, Texas Instruments Incorporated



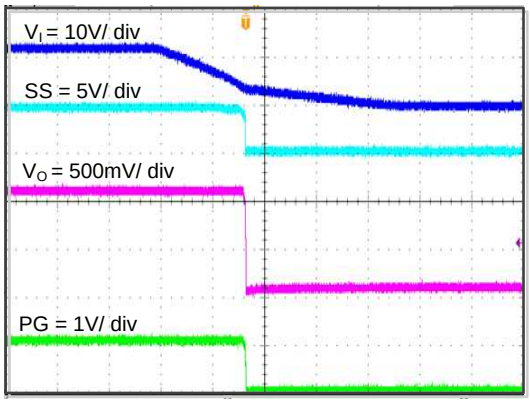
Time = 1 msec / div

Figure 43. TPS563210A Start Up Relative To V_I



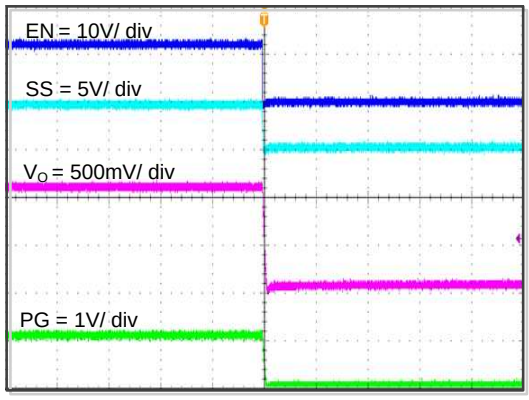
Time = 1 msec / div

Figure 44. TPS563210A Start Up Relative To EN



Time = 5 msec / div

Figure 45. TPS563210A Shut Down Relative To V_I



Time = 5 msec / div

Figure 46. TPS563210A Shut Down Relative To EN

9 Power Supply Recommendations

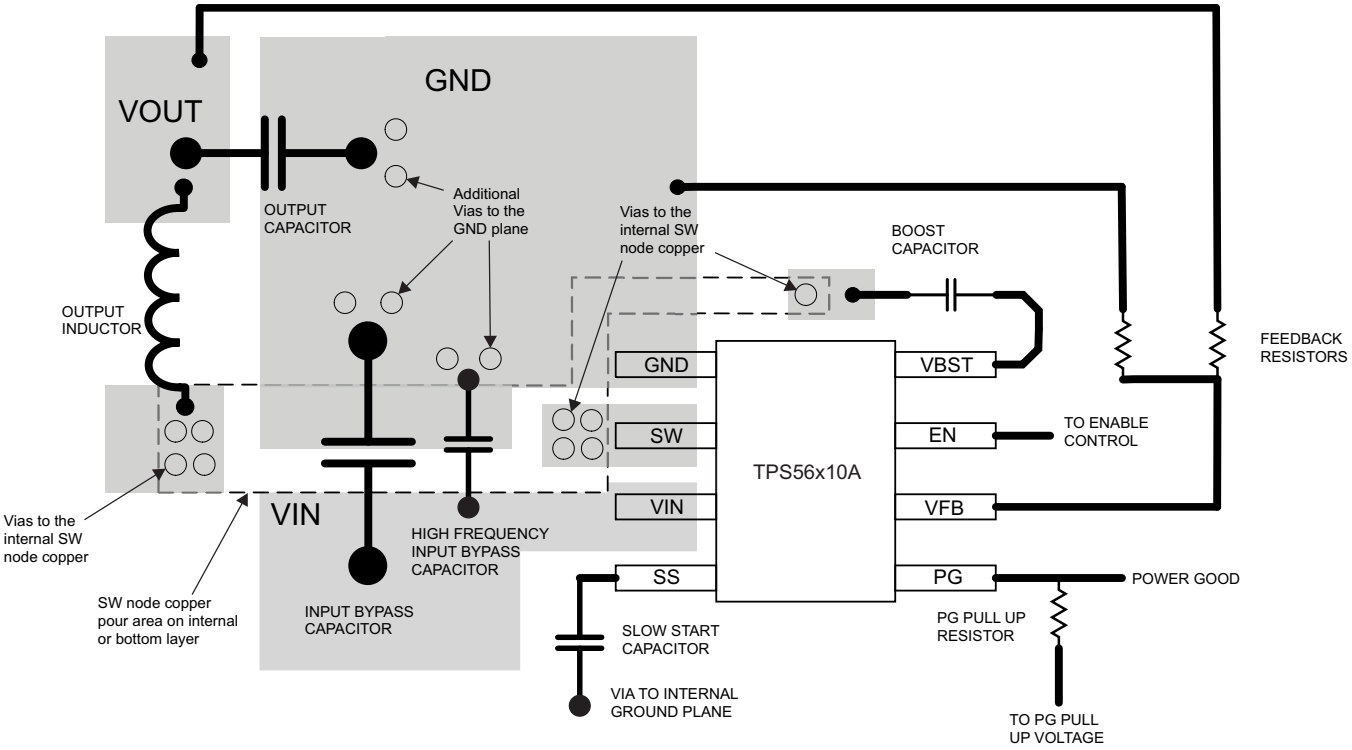
The TPS562210A and TPS563210A are designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is V_O / 0.65.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example



Copyright © 2016, Texas Instruments Incorporated

11 Device and Documentation Support

11.1 Device Support

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS562210A	Click here	Click here	Click here	Click here	Click here
TPS563210A	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

D-CAP2, Eco-mode, E2E are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS562210ADDFR	ACTIVE	SOT	DDF	8	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	2210A	Samples
TPS562210ADDFT	ACTIVE	SOT	DDF	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	2210A	Samples
TPS563210ADDFR	ACTIVE	SOT	DDF	8	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	3210A	Samples
TPS563210ADDFT	ACTIVE	SOT	DDF	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	3210A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

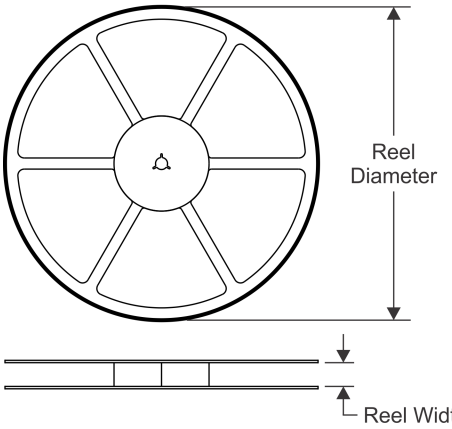
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

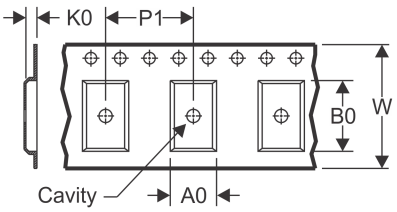
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

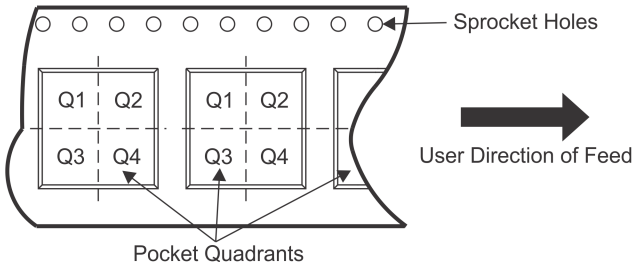


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

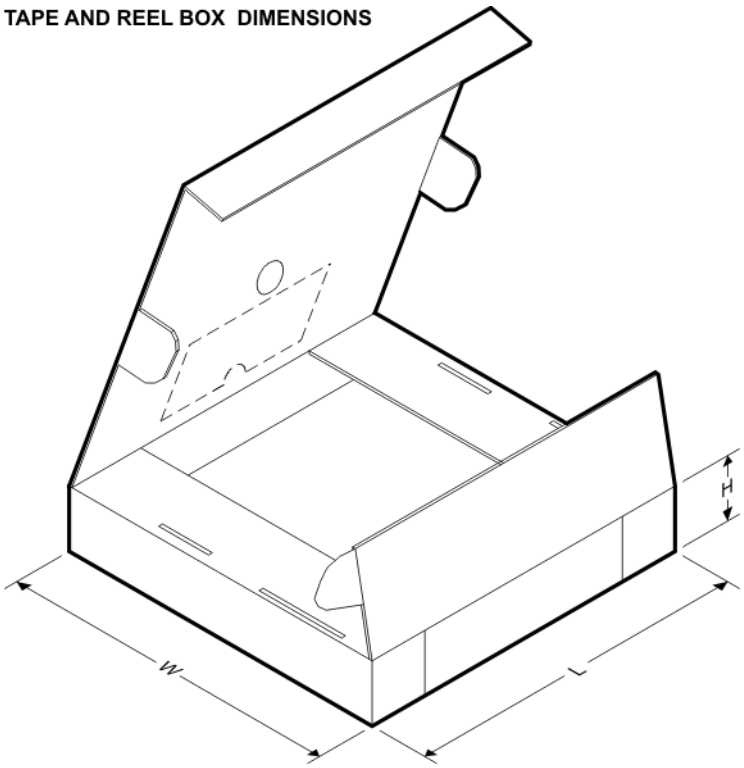
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS562210ADDFR	SOT	DDF	8	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS562210ADDFT	SOT	DDF	8	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS563210ADDFR	SOT	DDF	8	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TPS563210ADDFT	SOT	DDF	8	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

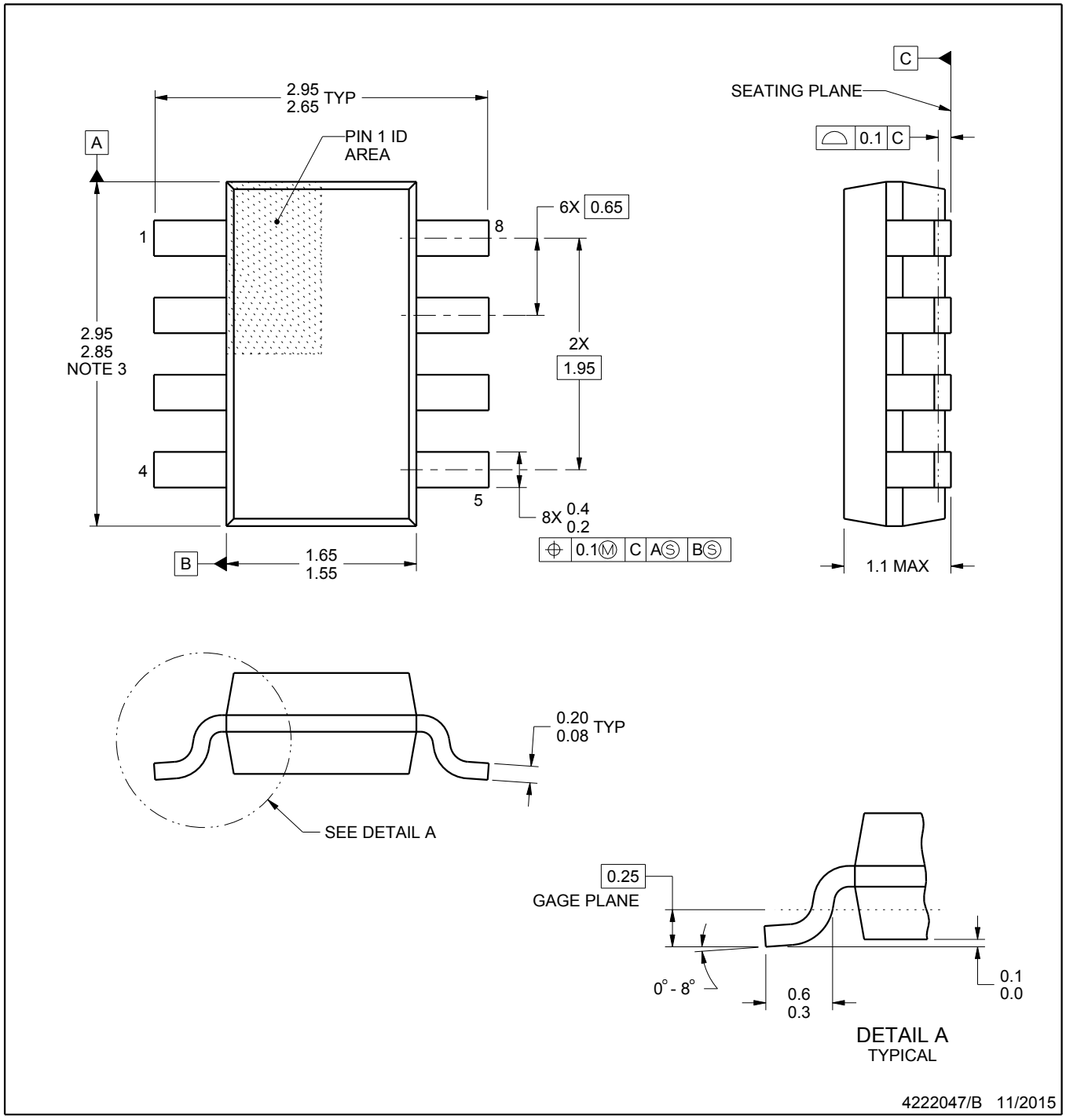
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS562210ADDFR	SOT	DDF	8	3000	184.0	184.0	19.0
TPS562210ADDFT	SOT	DDF	8	250	184.0	184.0	19.0
TPS563210ADDFR	SOT	DDF	8	3000	184.0	184.0	19.0
TPS563210ADDFT	SOT	DDF	8	250	184.0	184.0	19.0

PACKAGE OUTLINE

DDF0008A

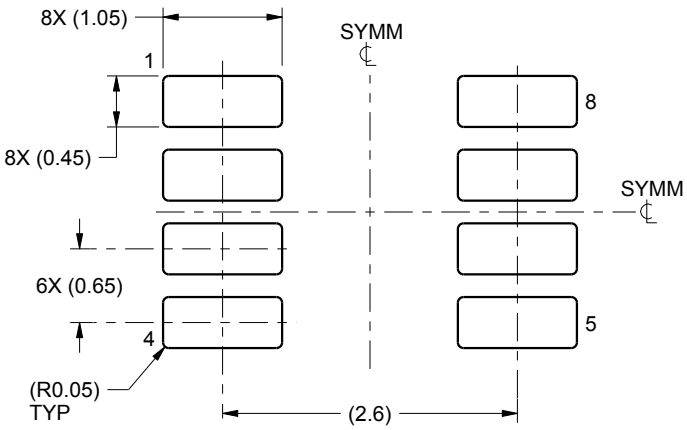
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

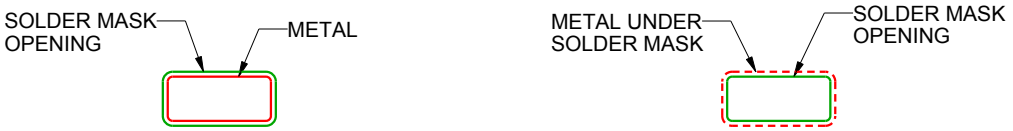


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

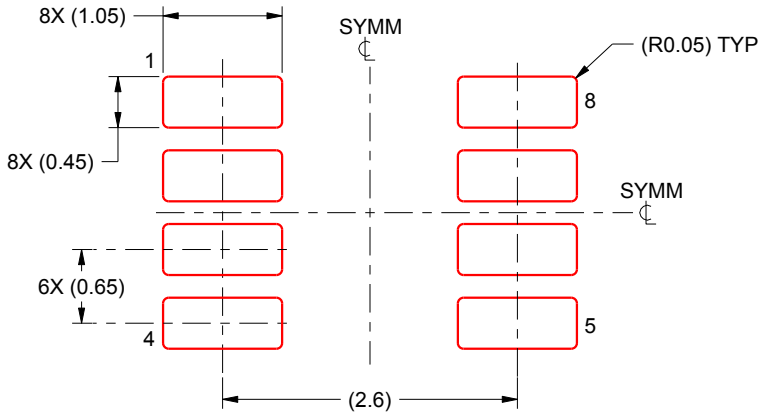
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated