

TPS27S100x 40V 4A 80mΩ 单通道高侧开关

1 特性

- 具有全面诊断功能的 80mΩ 单通道高侧开关
 - TPS27S100A: 开漏状态输出
 - TPS27S100B: 电流监视器模拟输出
- 宽工作电压范围: 3.5V 至 40V
- 超低待机电流, 低于 0.5μA
- 工作结温范围, -40°C 至 150°C
- 输入控制, 兼容 3.3V 和 5V 逻辑
- 高精度电流监控器, 在 1A 时精度为 ±30mA
- 可通过外部电阻器将电流限制调节为 0.5A 至 6A (在 0.5A 时精度为 ±20%)
- 用于对 MCU、模拟或数字接口进行多路复用的诊断使能功能
- 针对 IN 和 OUT 引脚的出色 ESD 保护
 - ±16kV IEC 61000-4-2 ESD 接触放电
 - ±4kV IEC 61000-4-4 电气快速瞬变
 - ±1.0kV/42Ω IEC 61000-4-5 浪涌
- 保护
 - 过载和接地短路保护
 - 电感负载负电压钳位
 - 欠压锁定 (UVLO) 保护
 - 具备自恢复功能的热关断和热振荡
 - 接地失效保护
- 诊断
 - 开启和关闭状态输出开路负载/对电源短路检测
 - 过载和接地短路检测
 - 热关断和热振荡检测
- 热增强型 14 引脚 PWP 或 16 引脚 QFN 封装

2 应用

- 可编程逻辑控制器
- 楼宇自动化
- 电信/网络

3 说明

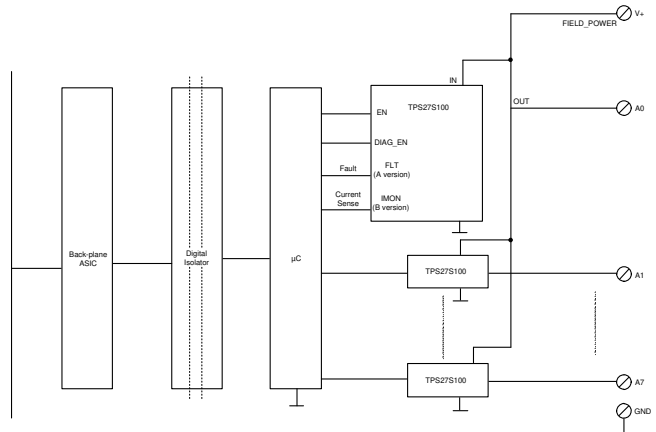
TPS27S100x 是一款受到全面保护的单通道高侧开关, 具有集成式 NMOS 和电荷泵。全面的诊断功能和高精度电流监控器功能, 可对负载进行智能控制。可调节电流限制功能能够极大地提高整个系统的可靠性。器件诊断报告具有两个版本, 以支持数字故障状态和模拟电流监控器输出。精确的电流监控器和可调节电流限制特性使该器件从市场中脱颖而出。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS27S100x	HTSSOP (14)	4.40mm × 5.00mm
	QFN (16)	4.00mm × 3.5mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型应用原理图



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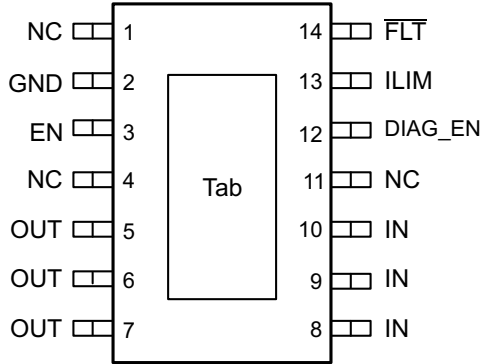
4 修订历史记录

Changes from Revision A (February 2018) to Revision B	Page
• 向特性部分中添加了 QFN 封装	1
• 向设备信息 表中添加了 QFN (16) 封装, 以及 4.00mm × 3.5mm 的封装尺寸	1
• 更新了 典型应用原理图	1
• Added RRK Package to the <i>Pin Out Drawing</i> and <i>Pin Functions</i> table	3
• Updated the Specifications <i>Absolute Maximum Ratings</i> table	4
• Changed the Operation junction temperature range MAX from 150°C to 125°C in the Specifications <i>Recommended Operating Conditions</i> table	4
• Added RRK package to the Specifications <i>Thermal Information</i> table	4
• Updated the Operating Current section in the Specifications <i>Electrical Characteristics</i> table	4

Changes from Original (October 2017) to Revision A	Page
• Added footnote 2 and 3 to the <i>Electrical Characteristics</i> table	4
• Added reverse current protection information to the Reverse Current Protection section	22

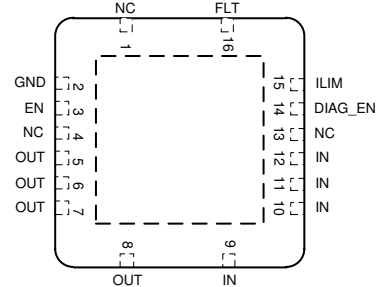
5 Pin Configuration and Functions

TPS27S100A PWP Package
14-Pin HTSSOP With Exposed Thermal Pad
Top View



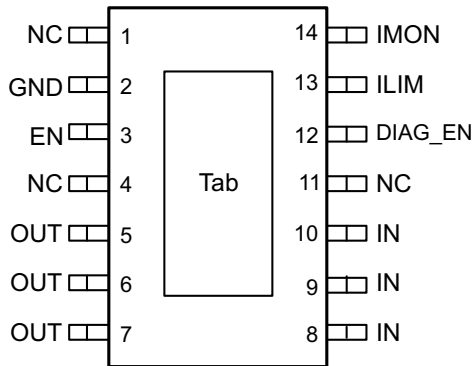
NC – No internal connection

TPS27S100A RRK Package
16-Pin QFN With Exposed Thermal Pad
Top View



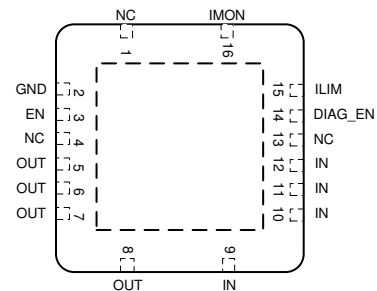
NC – No internal connection

TPS27S100B PWP Package
14-Pin HTSSOP With Exposed Thermal Pad
Top View



NC – No internal connection

TPS27S100B RRK Package
16-Pin QFN With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

NAME	PIN				I/O	DESCRIPTION
	TPS27S100 A PWP	TPS27S100 B PWP	TPS27S100 A RRK	TPS27S100B RRK		
DIAG_EN	12	12	14	14	I	Enable and disable pin for diagnostic functions. Connect to device GND if not used.
EN	3	3	3	3	I	Enable control for channel activation.
FLT	14	—	16	—	O	Open-drain diagnostic status output. Leave floating if not used.
GND	2	2	2	2	—	Ground pin.
ILIM	13	13	15	15	O	adjustable current-limit pin. Connect to device GND if external current limit is not used.
IMON	—	14	—	16	O	Current-monitor output. Leave floating if not used.
IN	8, 9, 10	8, 9, 10	9, 10, 11, 12	9, 10, 11, 12	I	Power supply.
NC	1, 4, 11	1, 4, 11	1, 4, 13	1, 4, 13	—	No-connect pin; leave floating.
OUT	5, 6, 7	5, 6, 7	5, 6, 7, 8	5, 6, 7, 8	O	Output, connected to load.
Thermal pad	—	—	—	—	—	Thermal pad. Connect to device GND or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

	MIN	MAX	UNIT
Supply voltage		40	V
Supply voltage (for transients less than 400 ms)		48	V
Current on GND pin, $t < 2$ minutes	–250	100	mA
Voltage on EN and DIAG_EN pins	–0.3	7	V
Current on EN and DIAG_EN pins	–10		mA
Voltage on $\overline{\text{FLT}}$ pin	–0.3	7	V
Current on $\overline{\text{FLT}}$ pin	–30	10	mA
Voltage on ILIM pin	–0.3	7	V
Voltage on IMON pin	–2.7	6.5	V
Inductive load switch-off energy dissipation, single pulse ⁽³⁾		70	mJ
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Test condition: $V_{\text{IN}} = 13.5$ V, $L = 8$ mH, $R = 0$ Ω , $T_J = 150^\circ\text{C}$. FR4 2s2p board, 2- $\times$ 70- μm Cu, 2- $\times$ 35- μm Cu. 600-mm² board copper area.

6.2 ESD Ratings

			VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge	Human body model (HBM) ⁽¹⁾	IN, OUT, GND	± 5000
		Human body model (HBM) ⁽¹⁾	Other pins	± 4000
		Charged device model (CDM)		± 750
$V_{\text{(ESD)}}$	Electrostatic discharge	Contact/Air discharge, per IEC 61000-4-2 ⁽²⁾	IN, OUT	± 16000
$V_{\text{(ESD)}}$		Electrical fast transient, per IEC 61000-4-4 ⁽²⁾	IN, OUT	± 4000
$V_{\text{(ESD)}}$		Surge protection with 42 Ω , per IEC 61000-4-5; 1.2/50 μs ⁽²⁾	IN, OUT	± 1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) Tested with application circuit shown in [Figure 35](#) with $C_{\text{VIN1}} = 47$ μF , $C_{\text{VIN2}} = 100$ nF, $C_{\text{VOUT}} = 22$ nF and SM15T30A TVS input clamp. Supply voltage of 24 V DC is always ON, EN Inputs are High, so output is High (ON) and floating (no load).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Operating voltage	5	40	V
V_{ENx}	Voltage on EN and DIAG_EN pins	0	5	V
V_{FLT}	Voltage on $\overline{\text{FLT}}$ pin	0	5	V
$I_{\text{L,nom}}$	Nominal dc load current	0	4	A
T_J	Operating junction temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS27S100x		UNIT
		PWP (HTSSOP)	RRK (QFN)	
		14 PINS	16 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	41	42.7	°C/W
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	29.7	31.3	°C/W
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	25.1	16.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		TPS27S100x		UNIT
		PWP (HTSSOP)	RRK (QFN)	
		14 PINS	16 PINS	
ψ_{JT}	Junction-to-top characterization parameter	0.9	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.8	16.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	4.6	°C/W

6.5 Electrical Characteristics

5 V < V_{IN} < 40 V; –40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
V _{IN(nom)}	Nominal operating voltage		4		40	V
V _{IN(uvr)}	Undervoltage restart	V _{IN} rises up	3.5	3.7	4	V
V _{IN(uvf)}	Undervoltage shutdown	V _{IN} falls down	3	3.2	3.5	V
V _(uv,hys)				0.5		V
OPERATING CURRENT						
I _(op)	Nominal operating current	V _{EN} = 5 V, V _{DIAG_EN} = 0 V, 5 V < V _{IN} < 30 V, no load; –40°C T _J < 125°C		2.5	3.2	mA
I _(op)	Nominal operating current	V _{EN} = 5 V, V _{DIAG_EN} = 0 V, 5 V < V _{IN} < 40 V, no load; –40°C T _J < 150°C		2.5	5	mA
I _(op)	Nominal operating current	V _{EN} = 5 V, V _{DIAG_EN} = 0 V, 24-Ω load			10	mA
I _(off)	Standby mode current	V _{IN} = 24 V, V _{EN} = V _{DIAG_EN} = V _{IMON} = V _{ILIM} = V _{OUT} = 0 V, T _J = 25°C			2	μA
I _(off,diag)	Standby current with diagnostic enabled	V _{IN} = 24 V, V _{EN} = 0 V, V _{DIAG_EN} = 5 V			1.2	mA
t _(off,deg)	Standby mode deglitch time ⁽¹⁾	EN from high to low, if deglitch time > t _(off,deg) , the device enters into standby mode.		2		ms
I _{kg(out)}	Off-state output leakage current	V _{IN} = 24 V, V _{EN} = V _{OUT} = 0, T _J = 25°C			0.5	μA
POWER STAGE						
r _{DS(on)}	On-state resistance	V _{IN} > 5 V, T _J = 25°C		80	100	mΩ
		V _{IN} > 5 V, T _J = 150°C			166	mΩ
		V _{IN} = 3.5 V, T _J = 25°C			120	mΩ
I _{ILIM(int)}	Internal current limit	Internal current limit value, ILIM pin connected to GND	7		13	A
I _{ILIM(TSD)}	Current limit during thermal shutdown	Internal current limit value under thermal shutdown		5		A
		External current limit value under thermal shutdown as a percentage of the external current limit setting value		50		%
V _{DS(clamp)}	Drain-to-source internal clamp voltage		50		70	V
OUTPUT DIODE CHARACTERISTICS						
V _F	Drain-to-source diode voltage	V _{EN} = 0, I _{OUT} = –0.2 A		0.7		V
I _(R1)	Continuous reverse current from source to drain	t < 60 s, V _{EN} = 0, T _J = 25°C. Short-to-supply condition.		2		A
I _(R2)	Continuous reverse current from source to drain	t < 60 s, V _{EN} = 0, T _J = 25°C. With GND network, 1-kΩ resistor in parallel with A diode. Reverse-polarity condition.		3		A
LOGIC INPUT (EN AND DIAG_EN)						
V _{IH}	Logic high-level voltage		2			V
V _{IL}	Logic low-level voltage				0.8	V
R _(EN,pd)	EN pulldown resistor			500		kΩ
R _(DIAG,pd)	DIAG_EN pulldown resistor			150		kΩ

(1) Value is specified by design, not subject to production test.

Electrical Characteristics (continued)

5 V < V_{IN} < 40 V; -40°C < T_J < 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIAGNOSTICS						
V _(ol,off)	Open-load detection threshold in off-state	V _{EN} = 0 V, When V _{IN} - V _{OUT} < V _(ol,off) , duration longer than t _{d(ol,off)} . Open load detected.	1.4	1.8	2.6	V
I _(ol,off)	Off-state output sink current with open load	V _{EN} = 0 V, V _{IN} = V _{OUT} = 24 V, T _J = 125°C.	-150			μA
t _{d(ol,off)}	Open-load detection-threshold deglitch time in off state	V _{EN} = 0 V, When V _{IN} - V _{OUT} < V _(ol,off) , duration longer than t _{d(ol,off)} . Open load detected.		600		μs
I _(ol,on)	Open-load detection threshold in on state	V _{EN} = 5 V, when I _{OUT} < I _(ol,on) , duration longer than t _{d(ol,on)} . Open load detected. Version A only	2	6	10	mA
t _{d(ol,on)}	Open-load detection-threshold deglitch time in on-state	V _{EN} = 5 V, when I _{OUT} < I _(ol,on) , duration longer than t _{d(ol,on)} . Open load detected.		700		μs
V _(FLT)	Fault low output voltage	I _{FLT} = 2 mA			0.4	V
T _(SD)	Thermal shutdown threshold			175		°C
T _(SD,rst)	Thermal shutdown status reset			155		°C
T _(SW)	Thermal swing shutdown threshold			60		°C
T _(hys)	Hysteresis for resetting the thermal shutdown and swing			10		°C
CURRENT MONITOR AND CURRENT LIMIT						
K _(IMON)	Current sense current ratio			500		
K _(ILIM)	Current limit current ratio			2000		
dK _{(IMON)/K_(IMON)}	Current-monitor accuracy	I _{load} ≥ 5 mA	-80		80	%
		I _{load} ≥ 25 mA	-12		12	
		I _{load} ≥ 50 mA	-8		8	
		I _{load} ≥ 0.1 A	-5		5	
		I _{load} ≥ 1 A	-3		3	
dK _{(ILIM)/K_(ILIM)}	External current-limit accuracy ⁽²⁾ , ⁽³⁾	I _{limit} ≥ 0.5 A, 25°C < T _J < 150°C	-20		20	%
		I _{limit} ≥ 0.5 A, -40°C < T _J < 25°C	-28		28	%
dK _{(ILIM)/K_(ILIM)}	External current-limit accuracy ⁽²⁾ , ⁽³⁾	I _{limit} ≥ 1.6 A, 25°C < T _J < 150°C	-15		15	%
		I _{limit} ≥ 1.6 A, -40°C < T _J < 25°C	-18		18	%
V _{IMON(lin)}	Current-monitor voltage linear voltage range ⁽¹⁾	V _{IN} ≥ 5 V	0		4	V
I _{OUT(lin)}	Current-monitor voltage linear current range ⁽¹⁾	V _{IN} ≥ 5 V, V _{IMON(lin)} ≤ 4 V	0		4	A
V _{IMON(H)}	IMON pin voltage in Fault mode	V _{IN} ≥ 7 V, fault mode	4.3	4.75	4.9	V
		V _{IN} ≥ 5 V, fault mode	Min(V _{IN} - 0.8, 4.3)		4.9	
I _{IMON(H)}	IMON pin current in Fault mode	V _{IMON} = 4.3 V, V _{IN} > 7 V, fault mode	10			mA
V _{IMON(th)}	Current limit internal threshold voltage ⁽¹⁾			1.233		V

(2) External current limit set is recommended to be higher than 500 mA.

(3) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting.

6.6 Timing Requirements – Current Monitor Characteristics⁽¹⁾

			MIN	NOM	MAX	UNIT
$t_{\text{IMON(off1)}}$	IMON settling time from DIAG_EN disabled	$V_{\text{EN}} = 5 \text{ V}$, $I_{\text{load}} \geq 5 \text{ mA}$. $V_{\text{DIAG_EN}}$ from 5 to 0 V. IMON to 10% of sense value.			10	μs
$t_{\text{IMON(on1)}}$	IMON settling time from DIAG_EN enabled	$V_{\text{EN}} = 5 \text{ V}$, $I_{\text{load}} \geq 5 \text{ mA}$. $V_{\text{DIAG_EN}}$ from 0 to 5 V. IMON to 90% of sense value.			10	μs
$t_{\text{IMON(off2)}}$	IMON settling time from EN falling edge	$V_{\text{DIAG_EN}} = 5 \text{ V}$, $I_{\text{load}} \geq 5 \text{ mA}$. EN from 5 to 0 V. IMON to 10% of sense value.			10	μs
		$V_{\text{DIAG_EN}} = 5 \text{ V}$, $I_{\text{load}} \geq 5 \text{ mA}$. EN from 5 to 0 V. Current limit triggered.			180	μs
$t_{\text{IMON(on2)}}$	IMON settling time from EN rising edge	$V_{\text{IN}} = 24 \text{ V}$, $V_{\text{DIAG_EN}} = 5 \text{ V}$, $I_{\text{load}} \geq 100 \text{ mA}$. V_{EN} from 0 to 5 V. IMON to 90% of sense value.			150	μs

(1) Value specified by design, not subject to production test.

6.7 Switching Characteristics

$V_{IN} = 24\text{ V}$, $R_{load} = 24\ \Omega$, over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time EN rising edge to $V_{OUT} = 10\%$, DIAG_EN high	20		50	μs
$t_{d(off)}$	Turn-off delay time EN falling edge to $V_{OUT} = 90\%$, DIAG_EN high	40		80	μs
$dV/dt_{(on)}$	Slew rate on $V_{OUT} = 10\%$ to 90% , DIAG_EN high	0.1		0.5	$\text{V}/\mu\text{s}$
$dV/dt_{(off)}$	Slew rate off $V_{OUT} = 90\%$ to 10% , DIAG_EN high	0.1		0.5	$\text{V}/\mu\text{s}$

(1) Value specified by design, not subject to production test.

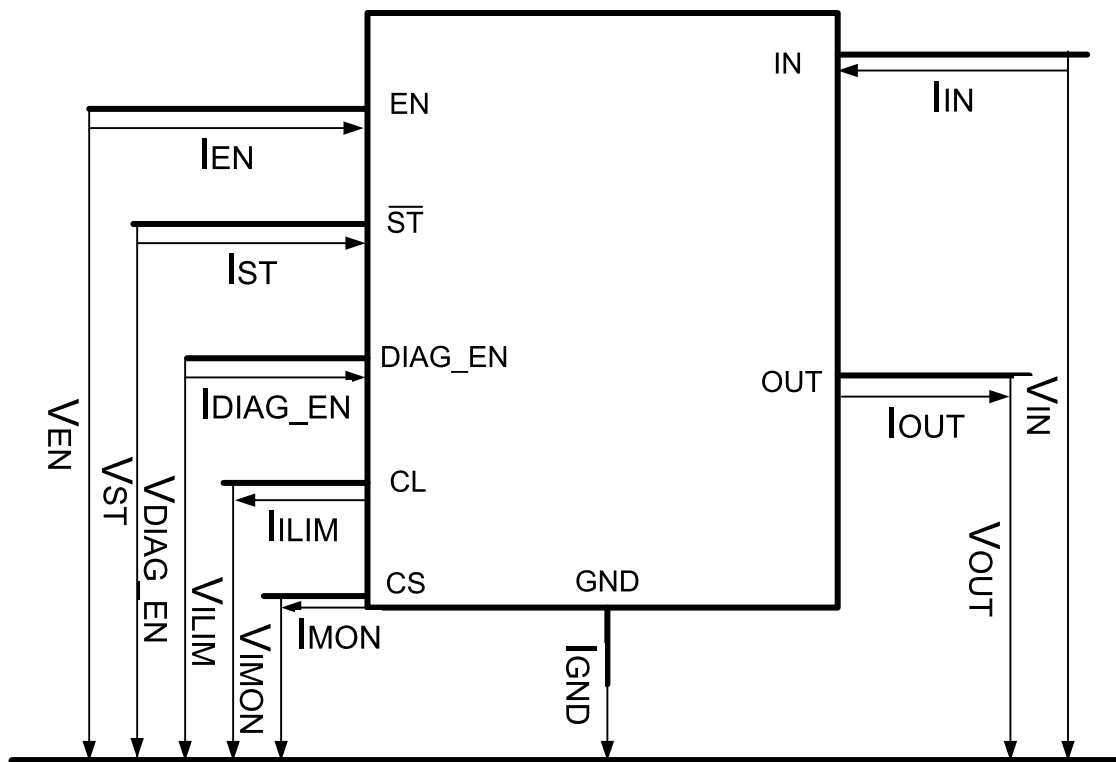


Figure 1. Pin Current and Voltage Conventions

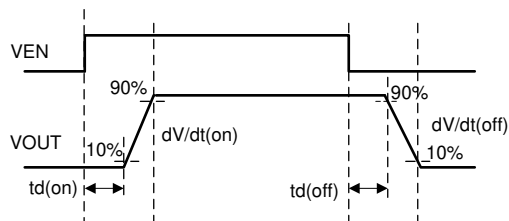


Figure 2. Output Delay Characteristics

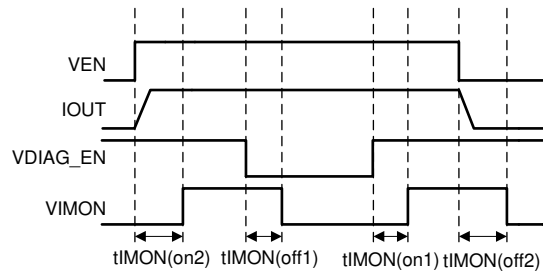


Figure 3. Current sense Delay Characteristics

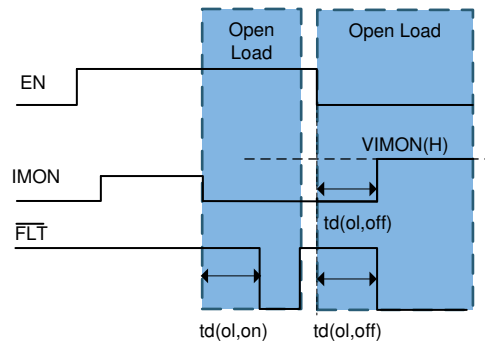


Figure 4. Open Load Blanking Time Characteristics

6.8 Typical Characteristics

All the below data are based on the mean value of the three lots samples, $V_{IN} = 24\text{ V}$ if not specified.

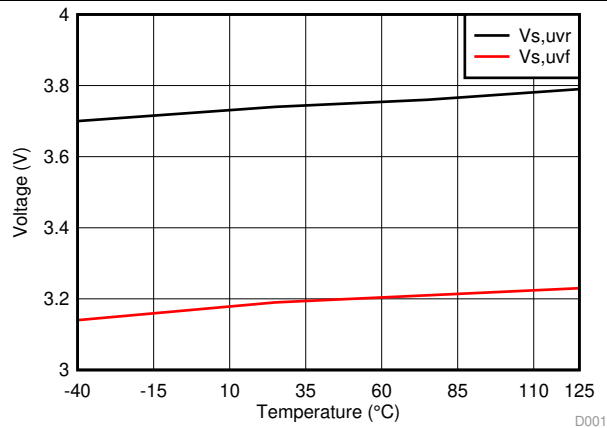


图 5. IN Pin Undervoltage Rising and Falling Thresholds
 $V_{IN,UVR}$ and $V_{IN,UVF}$

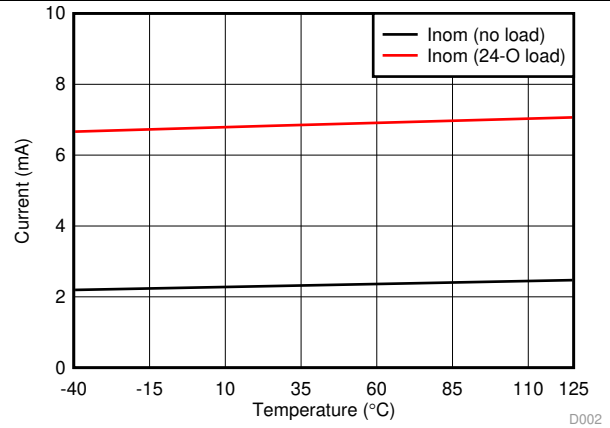


图 6. I_{nom} With No Load and 24-Ω Load

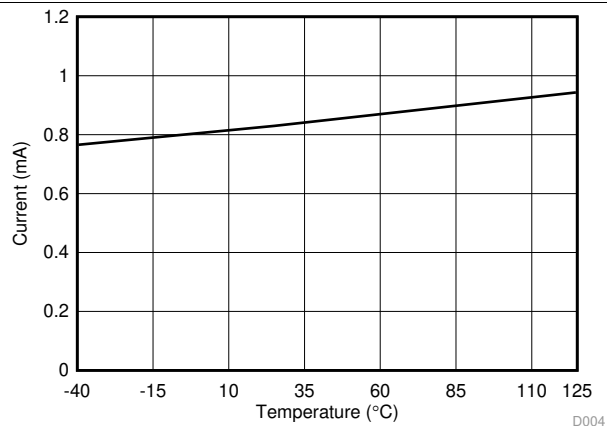


图 7. $I_{off,diag}$ as a Function of Temperature

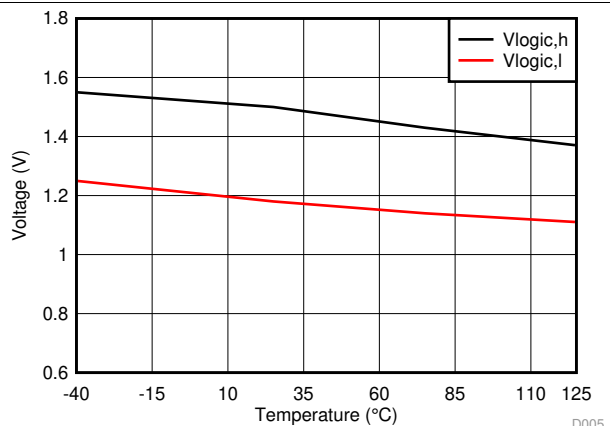


图 8. $V_{logic,h}$ and $V_{logic,l}$

Typical Characteristics (接下页)

All the below data are based on the mean value of the three lots samples, $V_{IN} = 24\text{ V}$ if not specified.

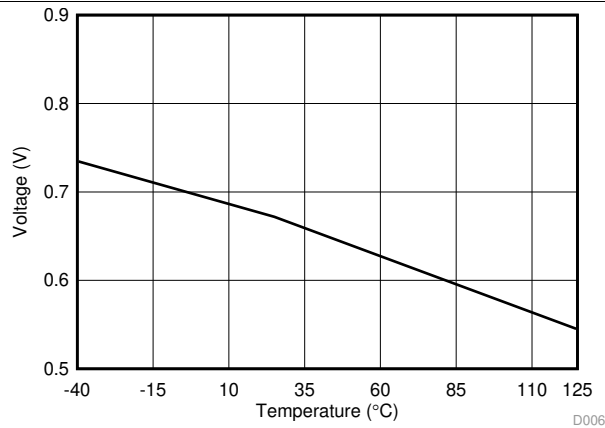


图 9. Drain-to-source Diode Voltage VF

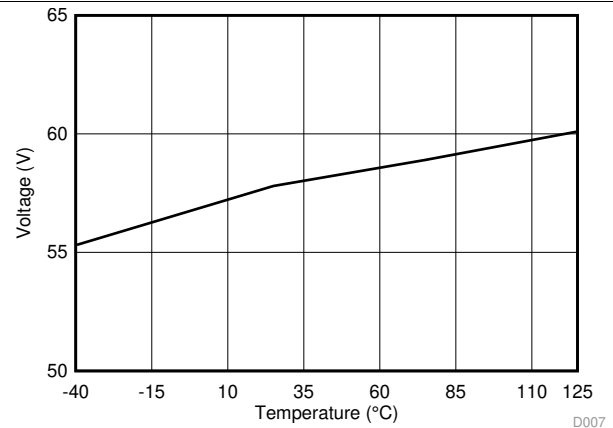


图 10. V_{DS} , Clamp

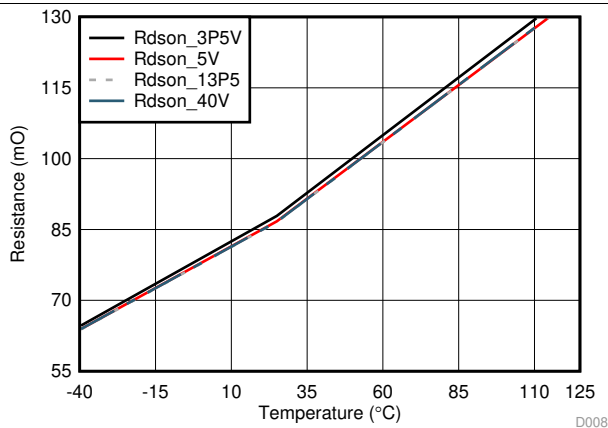


图 11. FET $R_{DS(on)}$

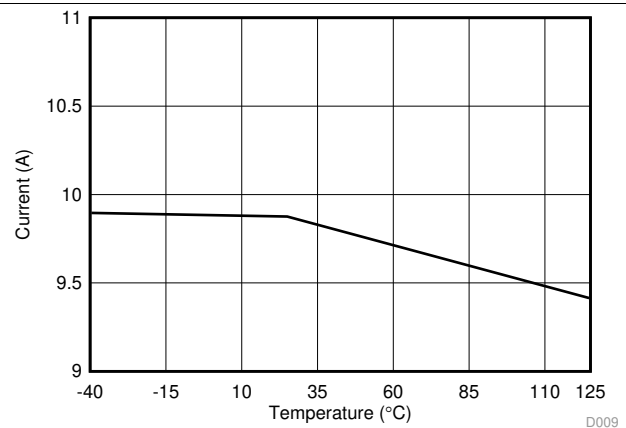


图 12. Current Limit $I_{lim,nom}$

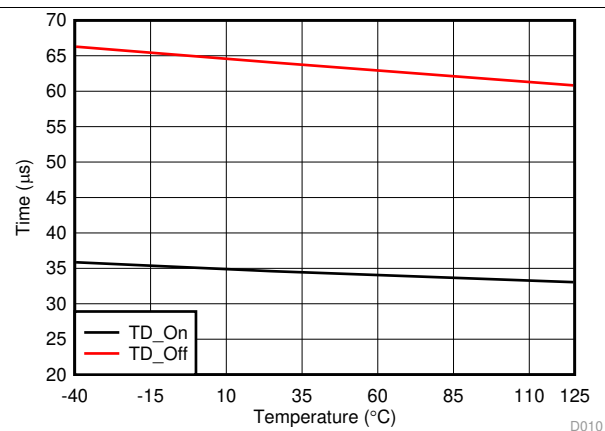


图 13. TDon and TDOff

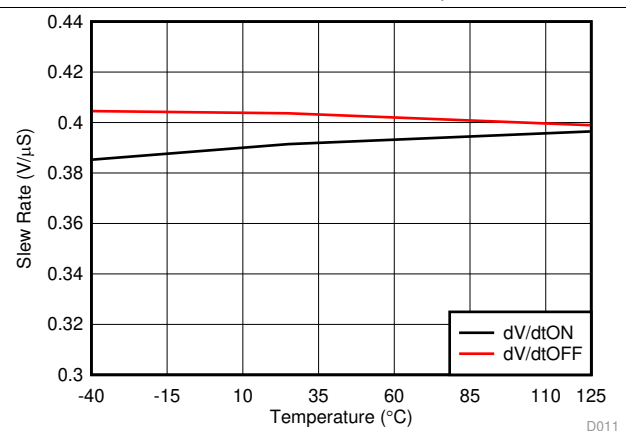


图 14. dV/dt_{ON} and dV/dt_{OFF}

Typical Characteristics (接下页)

All the below data are based on the mean value of the three lots samples, $V_{IN} = 24\text{ V}$ if not specified.

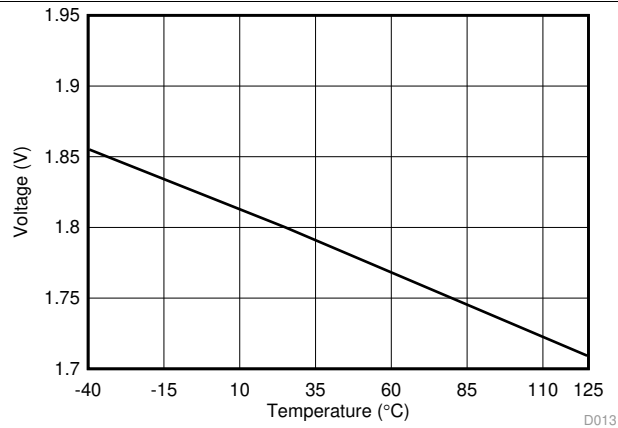


图 15. $V_{OL,off}$

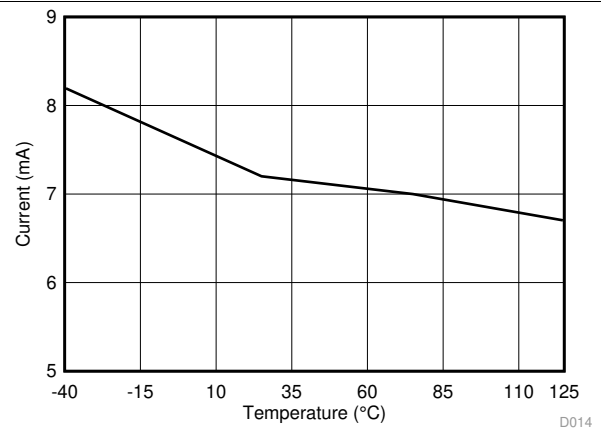


图 16. $I_{OL,on}$

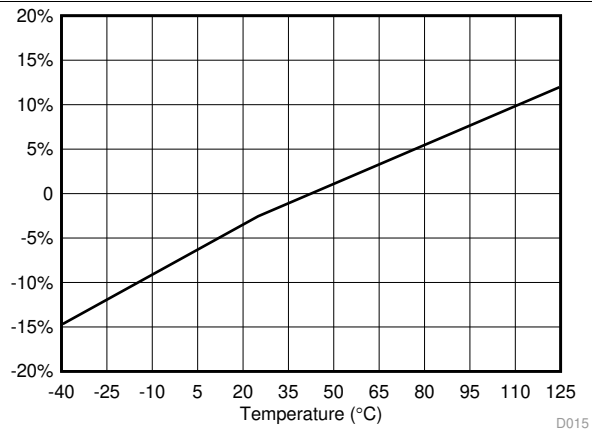


图 17. $K_{(IMON)}$ at $I_{OUT} = 5\text{ mA}$, $V_{IN} = 24\text{ V}$

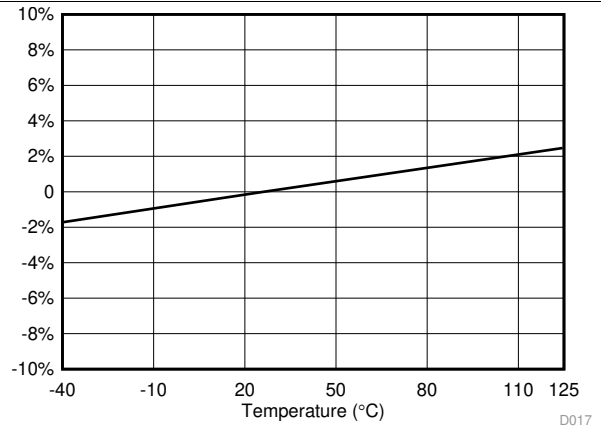


图 18. $K_{(IMON)}$ at $I_{OUT} = 25\text{ mA}$, $V_{IN} = 24\text{ V}$

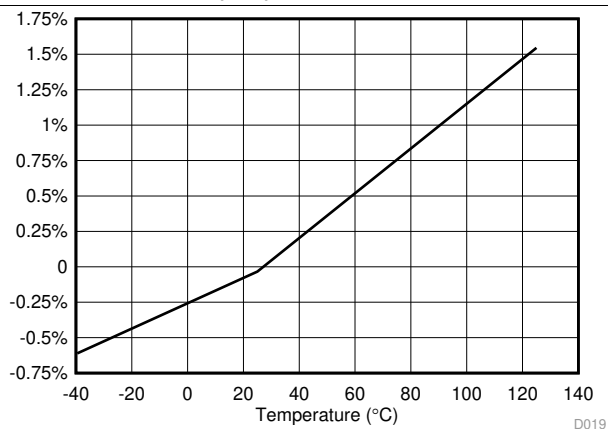


图 19. $K_{(IMON)}$ at $I_{OUT} = 50\text{ mA}$, $V_{IN} = 24\text{ V}$

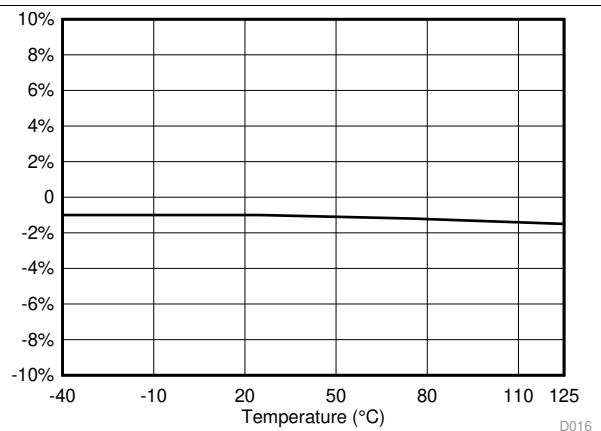


图 20. $K_{(IMON)}$ at $I_{OUT} = 100\text{ mA}$, $V_{IN} = 24\text{ V}$

Typical Characteristics (接下页)

All the below data are based on the mean value of the three lots samples, $V_{IN} = 24\text{ V}$ if not specified.

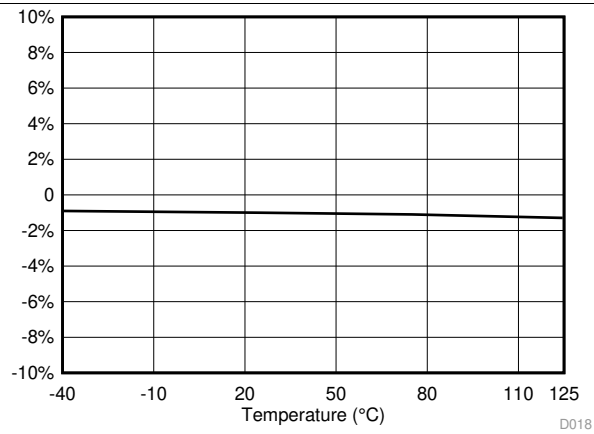


图 21. $K_{(IMON)}$ at $I_{OUT} = 1\text{ A}$, $V_{IN} = 24\text{ V}$

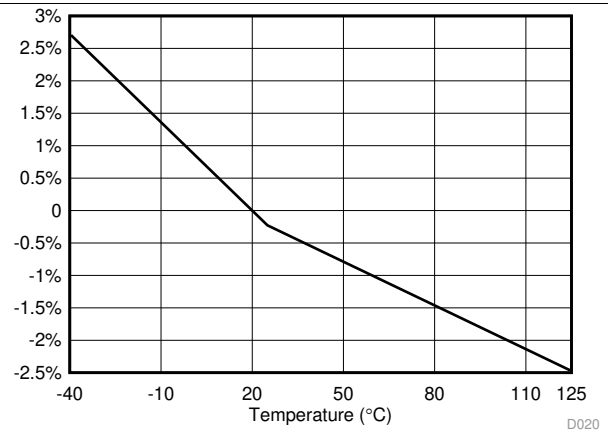


图 22. $K_{(ILIM)}$ at $I_{ILIM} = 0.5\text{ A}$, $V_{IN} = 24\text{ V}$

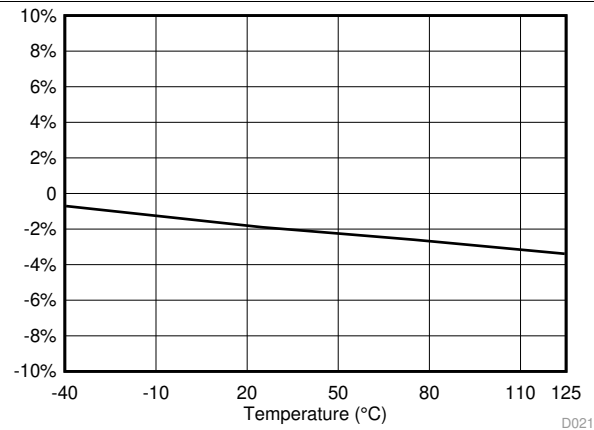


图 23. $K_{(ILIM)}$ at $I_{ILIM} = 1.6\text{ A}$, $V_{IN} = 24\text{ V}$

Feature Description (接下页)

K_{IMON} is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage range. Each part is factory calibrated during production test, so user-calibration is not required in most cases.

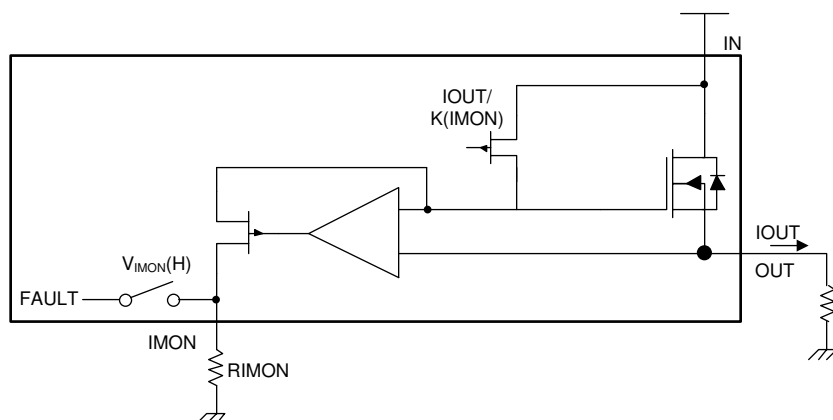


图 24. Current-monitor Block Diagram

When a fault occurs, the IMON pin also works as a fault report with a pullup voltage, $V_{IMON(H)}$.

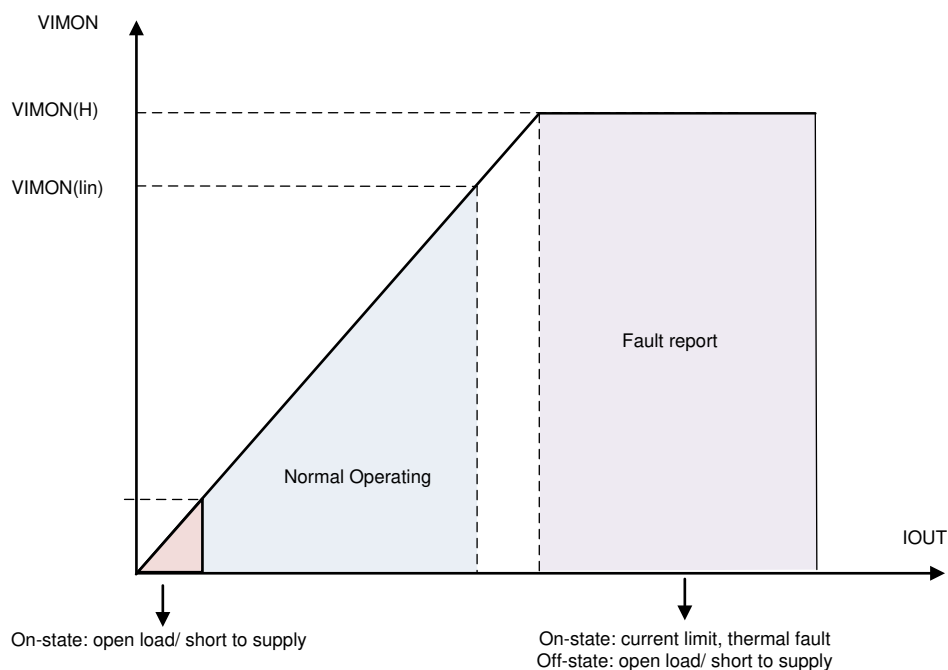


图 25. IMON Output-Voltage Curve

Use Equation 1 to calculate R_{IMON} . Also, please ensure V_{IMON} is within the current-sense linear region $V_{IMON(lin)}$ across the full range of the load current.

$$R_{IMON} = \frac{V_{IMON}}{I_{IMON}} = \frac{V_{IMON} \times K_{(IMON)}}{I_{OUT}} \quad (1)$$

Feature Description (接下页)

7.3.2 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from over-stressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When the current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{ILIM(TSD)}$ to reduce the power dissipation on the power FET.

The device has two current-limit thresholds.

Internal current limit – The internal current limit is fixed at $I_{ILIM(int)}$. Tie the ILIM pin directly to the device GND for large-transient-current applications.

External adjustable current limit – An external resistor is used to set the current-limit threshold. Use Equation 2 below to calculate the R_{ILIM} . $V_{ILIM(th)}$ is the internal band-gap voltage. $K_{(ILIM)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

$$R_{ILIM} = \frac{V_{ILIM(th)} \cdot K_{(ILIM)}}{I_{OUT}} \quad (2)$$

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must be connected with device GND.

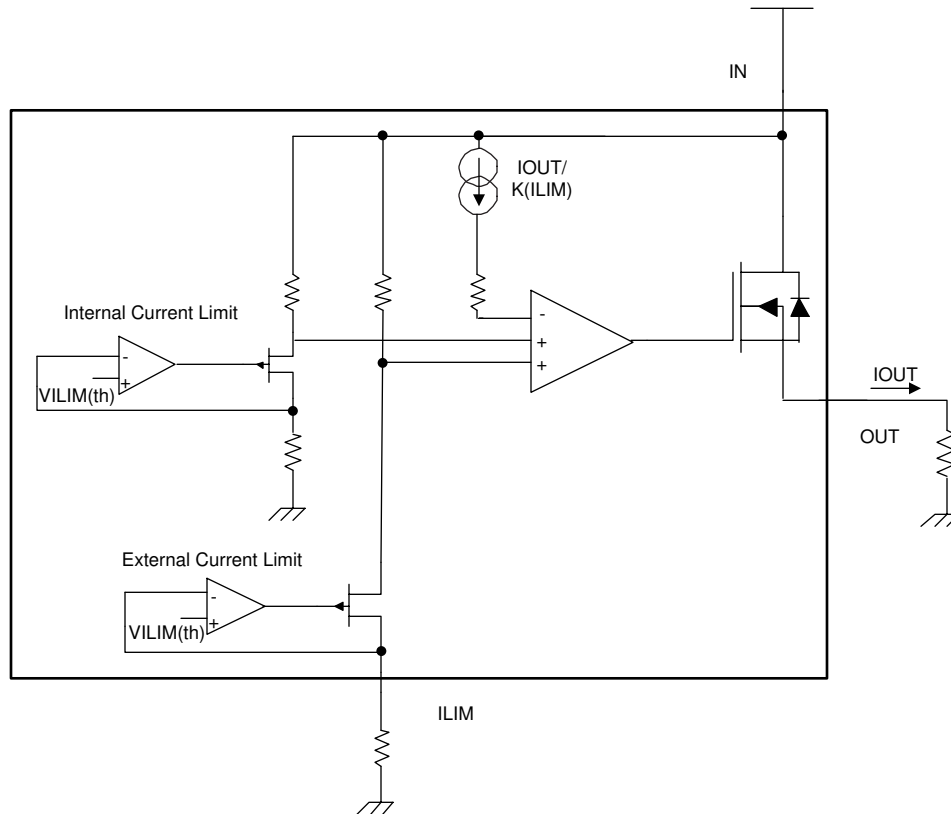


图 26. Current-Limit Block Diagram

For better protection from a hard short-to-GND condition (when the EN pin is enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 μ s, typically. With this fast response, the device can achieve better inrush current-suppression performance.

Feature Description (接下页)

7.3.3 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

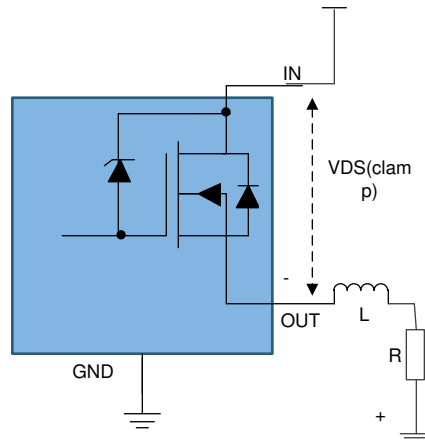


图 27. Drain-to-Source Clamping Structure

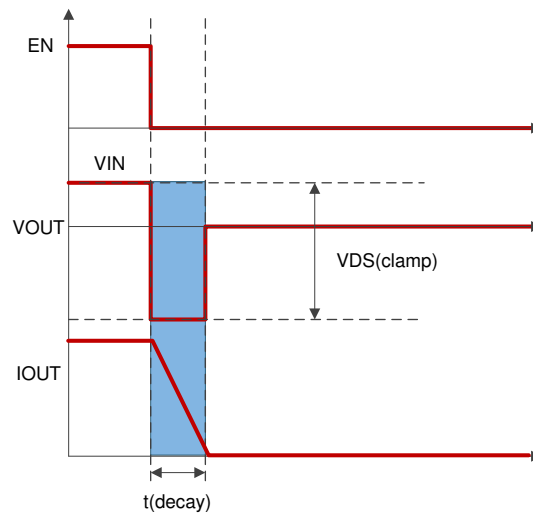


图 28. Inductive-Load Switching-Off Diagram

7.3.4 Full Protections and Diagnostics

表 1 is when DIAG_EN enabled. When DIAG_EN is low, all the diagnostics is disabled accordingly. The output is in high-impedance mode. Refer to 表 2 for details.

表 1. Fault Table

CONDITIONS	IN	OUT	CRITERION	$\overline{\text{FLT}}$ (TPS27S100A)	IMON (TPS27S100B)	FAULT RECOVERY
Normal	L	L		H	0	
	H	H		H	In linear region	
Short to GND	H	L	Current limit triggered.	L	$V_{IMON(H)}$	AUTO

Feature Description (接下页)

表 1. Fault Table (接下页)

CONDITIONS	IN	OUT	CRITERION	FLT (TPS27S100A)	IMON (TPS27S100B)	FAULT RECOVERY
Open load ⁽¹⁾ Short to supply	H	H	TPS27S100A: $I_{OUT} < I_{(ol,on)}$ TPS27S100B: Judged by users	L	Almost 0	AUTO
	L	H	$V_{IN} - V_{OUT} < V_{(ol,off)}$	L	$V_{IMON(H)}$	AUTO
Thermal shutdown	H		T_{SD} triggered	L	$V_{IMON(H)}$	Recovery when $T_J < T_{(SD,rst)}$ or when EN toggles.
Thermal swing	H		T_{SW} triggered	L	$V_{IMON(H)}$	AUTO

(1) Need external pull-up resistor during off-state

表 2. DIAG_EN Logic Table

DIAG_EN	EN	PROTECTIONS AND DIAGNOSTICS
HIGH	ON	See 表 1
	OFF	See 表 1
LOW	ON	Diagnostics disabled, protection normal IMON or FLT is high Impedance
	OFF	Diagnostics disabled, no protections IMON or FLT is high impedance

7.3.4.1 Short-to-GND and Overload Detection

When the switch is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{LIM(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

7.3.4.2 Open-Load Detection

When the channel is on, for TPS27S100A, if the current flowing through the output is less than $I_{(ol,on)}$, the device recognizes an open-load fault. For TPS27S100B, if an open-load event occurs, it can be detected as an ultra-low V_{IMON} and handled by the microcontroller.

When the channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{IN} - V_{OUT} < V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 15 kΩ.

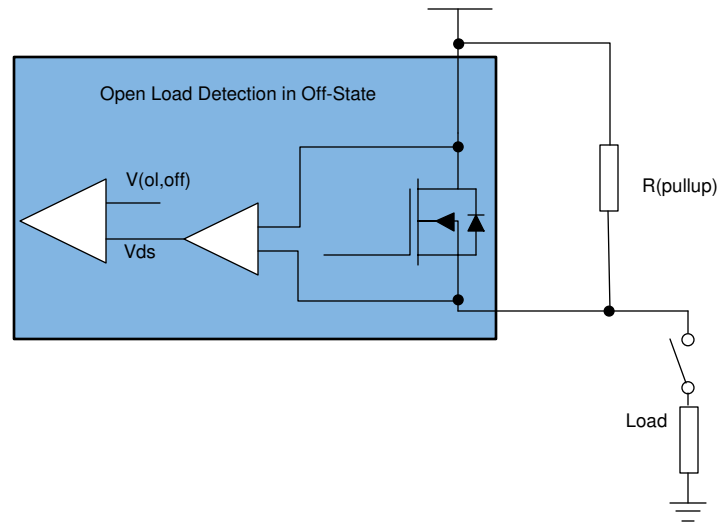


图 29. Open-Load Detection Circuit in Off-State

7.3.4.3 Short-to-Supply Detection

Short-to-Supply has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See [表 1](#) for more details.

7.3.4.4 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thermal shutdown occurs, the respective output turns off.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation.

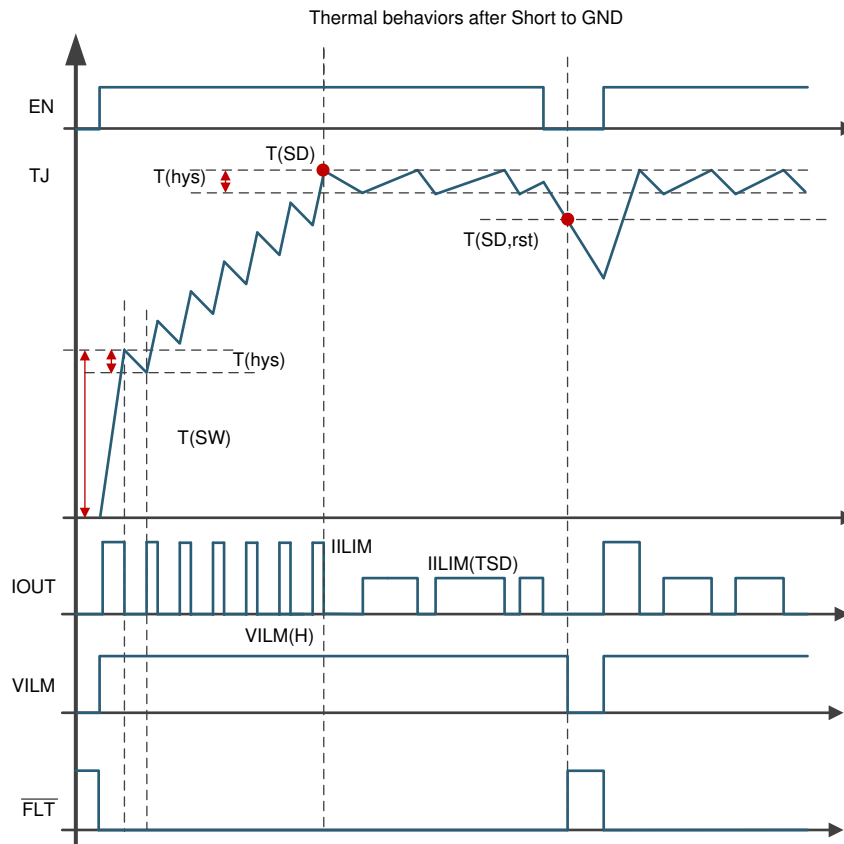


图 30. Thermal Behavior Diagram

7.3.4.5 UVLO Protection

The device monitors the supply voltage V_{IN} , to prevent unpredicted behaviors when V_{IN} is too low. When V_{IN} falls down to $V_{IN(uvf)}$, the device shuts down. When V_{IN} rises up to $V_{IN(uvr)}$, the device turns on.

7.3.4.6 Loss of GND Protection

When loss of GND occurs, output is shut down regardless of whether the EN pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

7.3.4.7 Reverse Current Protection

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

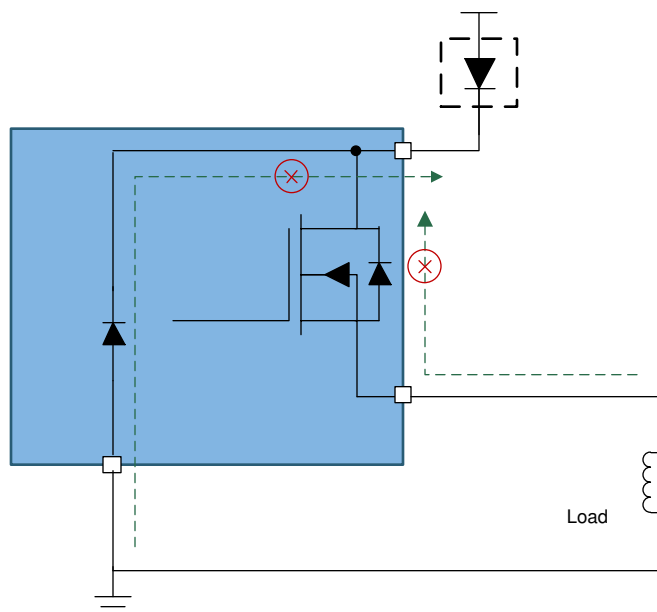


图 31. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-k Ω resistor in parallel with an >100-mA diode. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

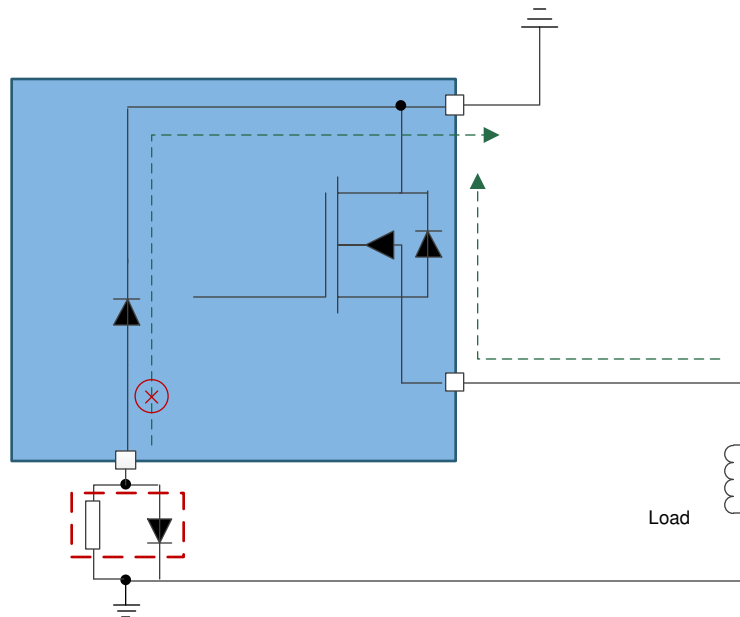


图 32. Reverse-Current External Protection, Method 2

7.3.4.8 Protection for MCU I/Os

TI recommends serial resistors to protect the microcontroller, for example, 4.7-k Ω when using a 3.3-V microcontroller and 10-k Ω for a 5-V microcontroller.

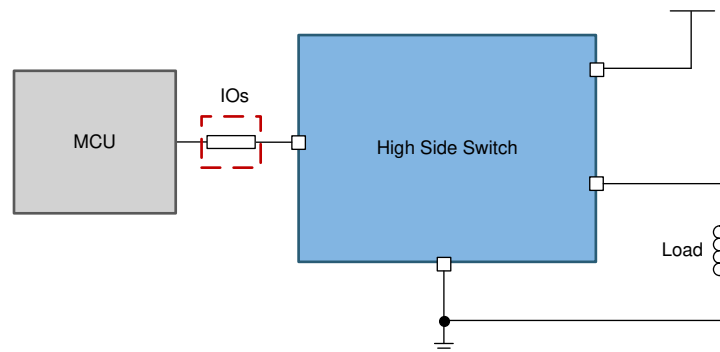


图 33. MCU I/O External Protection

7.4 Device Functional Modes

7.4.1 Working Mode

The device has three working modes: the normal mode, the standby mode, and the standby mode with diagnostics.

Device Functional Modes (接下页)

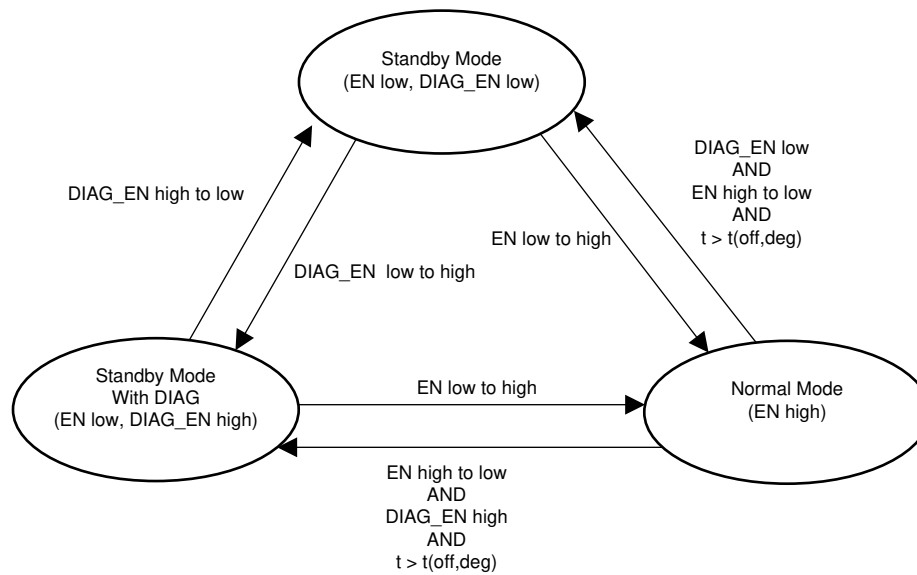


图 34. Working Modes

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is capable of driving a wide variety of resistive, inductive, and capacitive loads. Full diagnostics and high accuracy current-monitor features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

8.2 Typical Application

图 35 shows an example of how to design the external circuitry parameters.

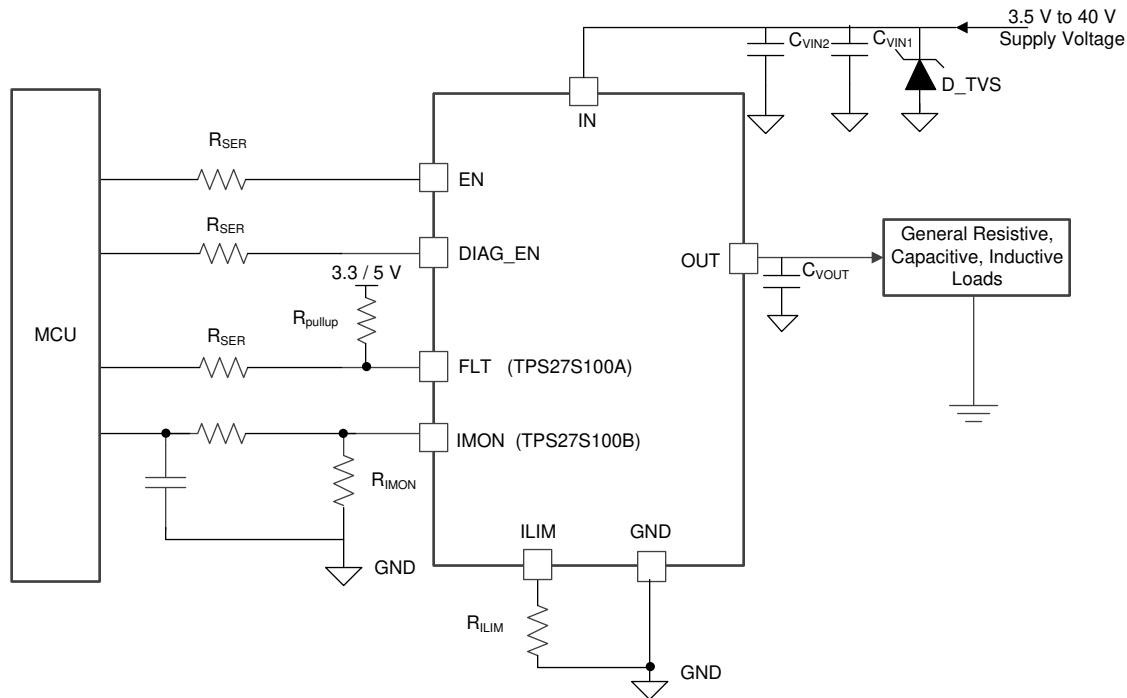


图 35. Typical Application Circuitry

表 3. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{SER}	15 k Ω	Protect microcontroller and device I/O pins
R_{IMON}	1 k Ω	Translate the sense current into sense voltage
C_{SNS}	100 pF - 10 nF	Low-pass filter for the ADC input
R_{ILIM}	0.82 k Ω	Set current limit threshold
$C_{VIN1/2}$	4.7 nF to Device GND	Filtering of high frequency noise
	220 nF to Module GND	Stabilize the input supply and voltage spike suppression for surge transient immunity.
C_{OUT}	22 nF	Immunity to ESD
D_{TVS}	36V TVS diode	Transient voltage clamp for surge transient immunity

8.2.1 Design Requirements

- V_{IN} range from 9 V to 30 V
- Nominal current of 2 A
- Current Monitor for fault monitoring
- Expected current limit value of 5 A
- Full diagnostics with 5-V MCU

8.2.2 Detailed Design Procedure

To keep the 2-A nominal current in the 0 to 4-V current-sense range, calculate the R_{IMON} resistor using Equation 3. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{IMON} = \frac{V_{IMON} \times K_{(IMON)}}{I_{OUT}} = \frac{4 \times 500}{2} = 1000 \, \Omega \quad (3)$$

To set the adjustable current limit value at 5-A, calculate R_{ILIM} using Equation 4.

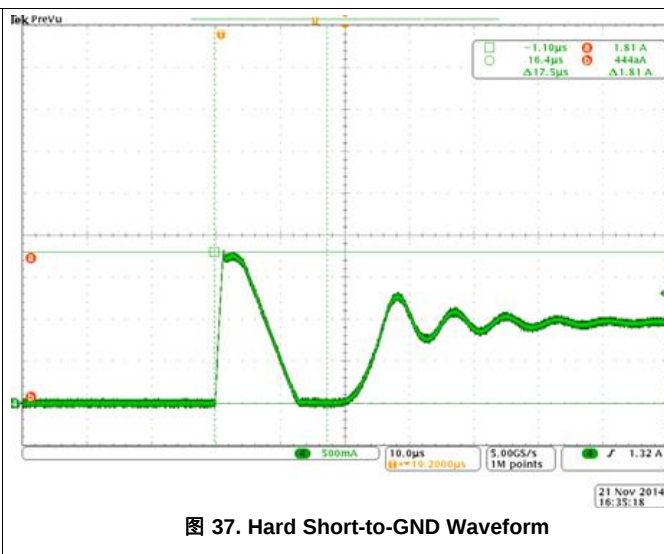
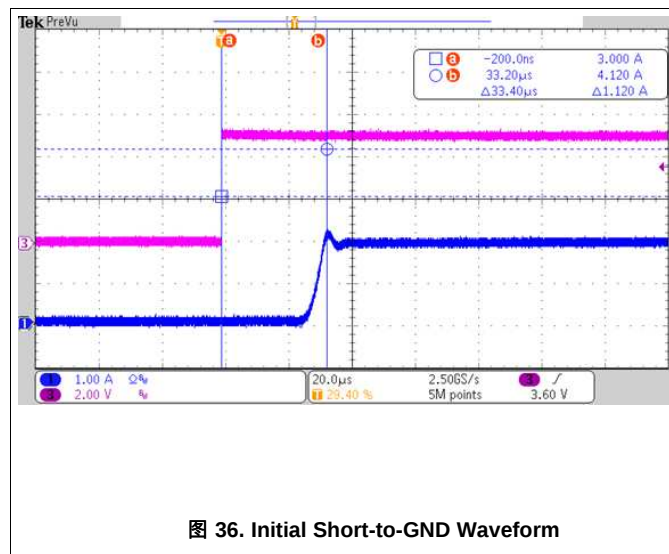
$$R_{ILIM} = \frac{V_{LIM(th)} \cdot K_{(ILIM)}}{I_{OUT}} = \frac{1.233 \cdot 2000}{5} = 493.2 \, \Omega \quad (4)$$

TI recommends $R_{SER} = 10 \, k\Omega$ for 5-V MCU, and $R_{pullup} = 10 \, k\Omega$ as the pull-up resistor.

8.2.3 Application Curves

图 36 shows a an example of initial inrush or short-circuit current limit. Test conditions: EN is from low to high, load is resistive short-to-GND or with a 470- μ F capacitive load, external current limit is 2 A. CH1 is the output current. CH3 is the EN step.

图 37 shows an example of current limit during hard short-circuit. Test conditions: EN is high, load is (5 μ H + 100 m Ω), external current limit is 1 A. A short to GND suddenly happens.



9 Power Supply Recommendations

The device is qualified for both 12-V and 24-V applications. The typical power input is a 12-V or 24-V industrial power supply.

10 Layout

10.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation may be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

10.2 Layout Example

10.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

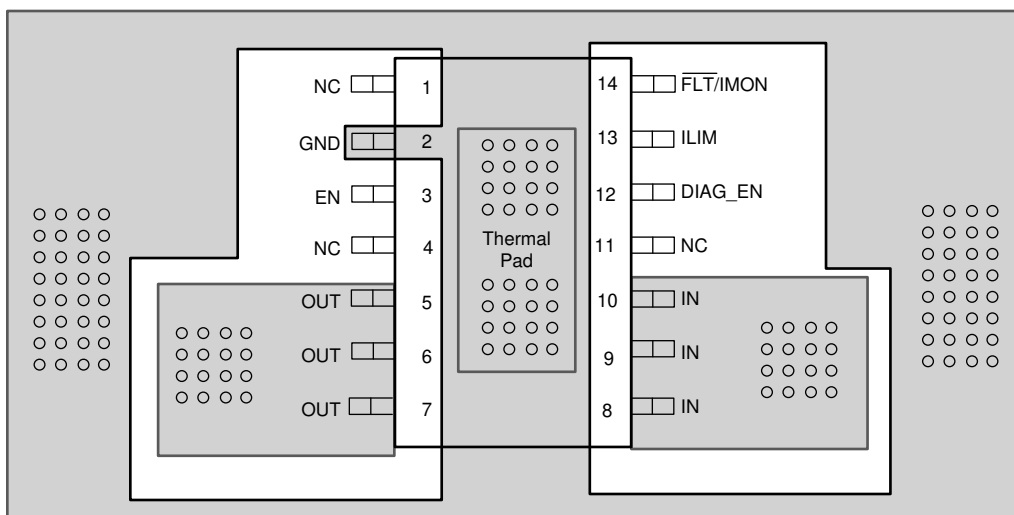


图 38. Layout Without a GND Network

Layout Example (接下页)

10.2.2 With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

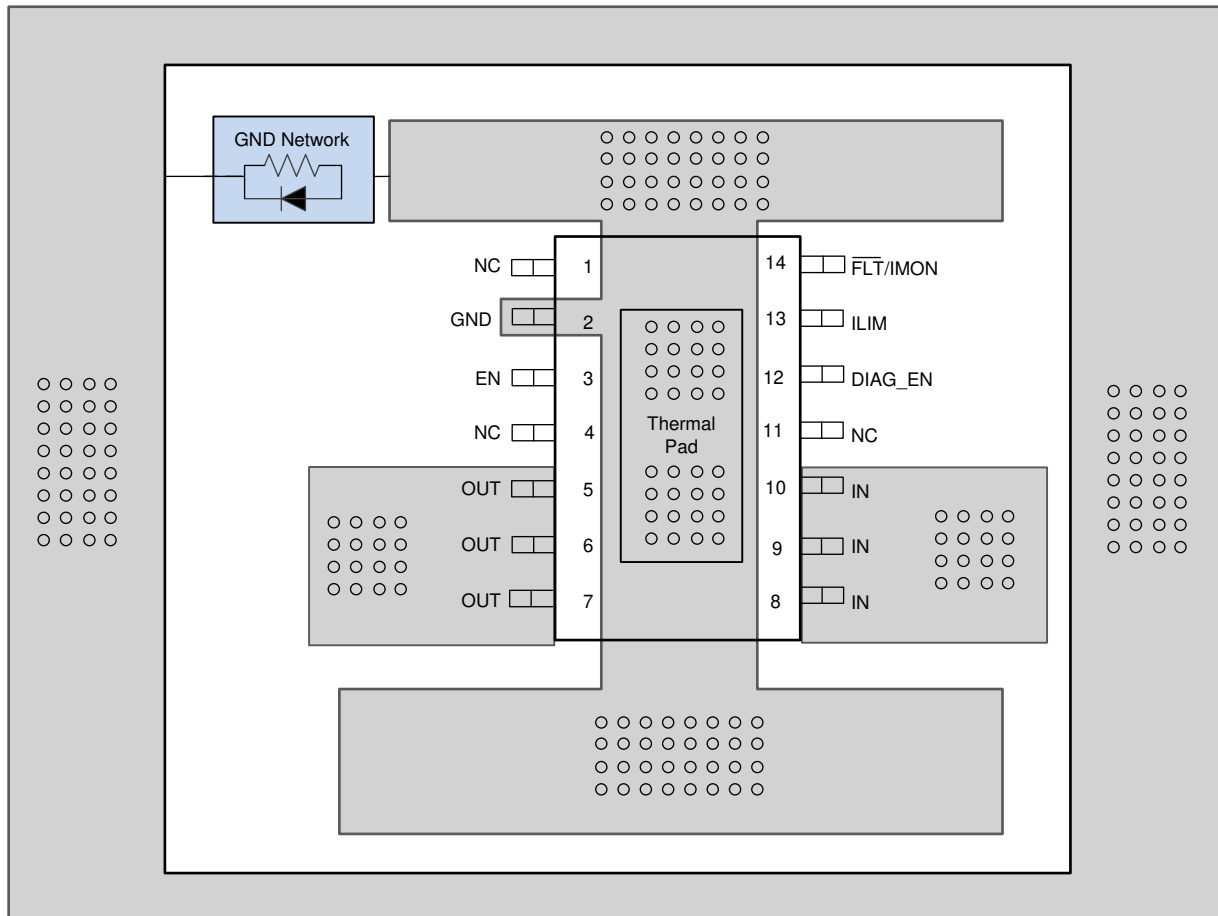


图 39. Layout With a GND Network

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.3 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS27S100APWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A	Samples
TPS27S100APWPT	ACTIVE	HTSSOP	PWP	14	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1A	Samples
TPS27S100ARRKR	ACTIVE	WQFN	RRK	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100A	Samples
TPS27S100ARRKT	ACTIVE	WQFN	RRK	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100A	Samples
TPS27S100BPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B	Samples
TPS27S100BPWPT	ACTIVE	HTSSOP	PWP	14	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	27S1B	Samples
TPS27S100BRRKR	ACTIVE	WQFN	RRK	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27S100B	Samples
TPS27S100BRRKT	ACTIVE	WQFN	RRK	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	27S100B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27S100APWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100ARRKR	WQFN	RRK	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100ARRKT	WQFN	RRK	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100BPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS27S100BRRKR	WQFN	RRK	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS27S100BRRKT	WQFN	RRK	16	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27S100APWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS27S100ARRKR	WQFN	RRK	16	3000	367.0	367.0	35.0
TPS27S100ARRKT	WQFN	RRK	16	250	210.0	185.0	35.0
TPS27S100BPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
TPS27S100BRRKR	WQFN	RRK	16	3000	367.0	367.0	35.0
TPS27S100BRRKT	WQFN	RRK	16	250	210.0	185.0	35.0

PLASTIC QUAD FLATPACK- NO LEAD



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

WQFN - 0.8 mm max height

Mechanical drawing of a 16-pin package. The drawing shows the package outline, pin locations, and dimensions. The package is rectangular with a central square area. The dimensions are as follows:

- Overall width: (3.3)
- Overall height: (3.8)
- Pin 1 to Pin 16 distance: (2.05)
- Pin 1 to Pin 16 distance (center-to-center): $2X(1.5)$
- Pin 1 to Pin 16 distance (edge-to-edge): $16X(0.6)$
- Pin 1 to Pin 16 distance (center-to-center): $16X(0.24)$
- Pin 1 to Pin 16 distance (edge-to-edge): $10X(0.5)$
- Pin 1 to Pin 16 distance (center-to-center): PKG $\varnothing$
- Pin 1 to Pin 16 distance (edge-to-edge): (0.775)
- Pin 1 to Pin 16 distance (center-to-center): (1.025)
- Pin 1 to Pin 16 distance (edge-to-edge): (2.55)
- Pin 1 to Pin 16 distance (center-to-center): (3.8)

The drawing also includes the following labels:

- 16X (0.6)
- 16X (0.24)
- 10X (0.5)
- PKG $\varnothing$
- (Ø0.2) VIA (TYP)
- (R0.05) TYP
- 1
- 2
- 7
- 8
- 9
- 10
- 15
- 16
- 17

The diagram illustrates two PCB manufacturing processes:

- NON- SOLDER MASK DEFINED:** This process shows a central **EXPOSED METAL** pad (black dot) surrounded by a **METAL** layer (blue outline). This is further enclosed by a **SOLDER MASK OPENING** (green outline). The distance between the metal layer and the solder mask opening is specified as **0.07 MAX ALL AROUND**.
- SOLDER MASK DEFINED:** This process shows a central **EXPOSED METAL** pad (black dot) surrounded by **METAL UNDER SOLDER MASK** (blue dashed outline). This is further enclosed by a **SOLDER MASK OPENING** (green outline). The distance between the metal under solder mask and the solder mask opening is specified as **0.07 MIN ALL AROUND**.

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3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PLASTIC QUAD FLATPACK- NO LEAD

GENERIC PACKAGE VIEW

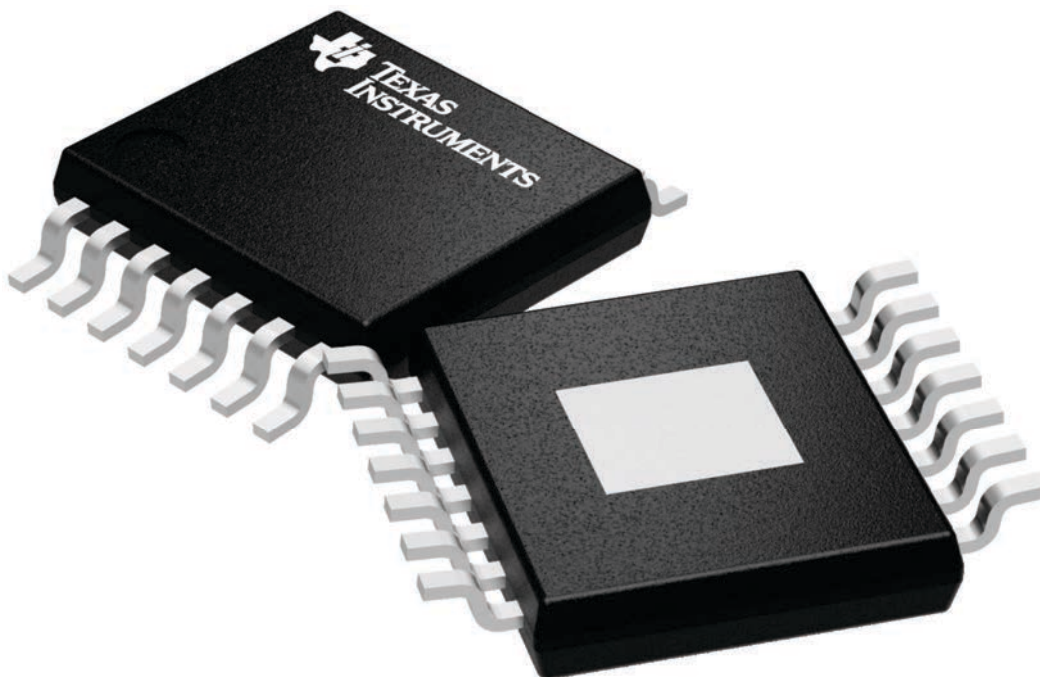
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

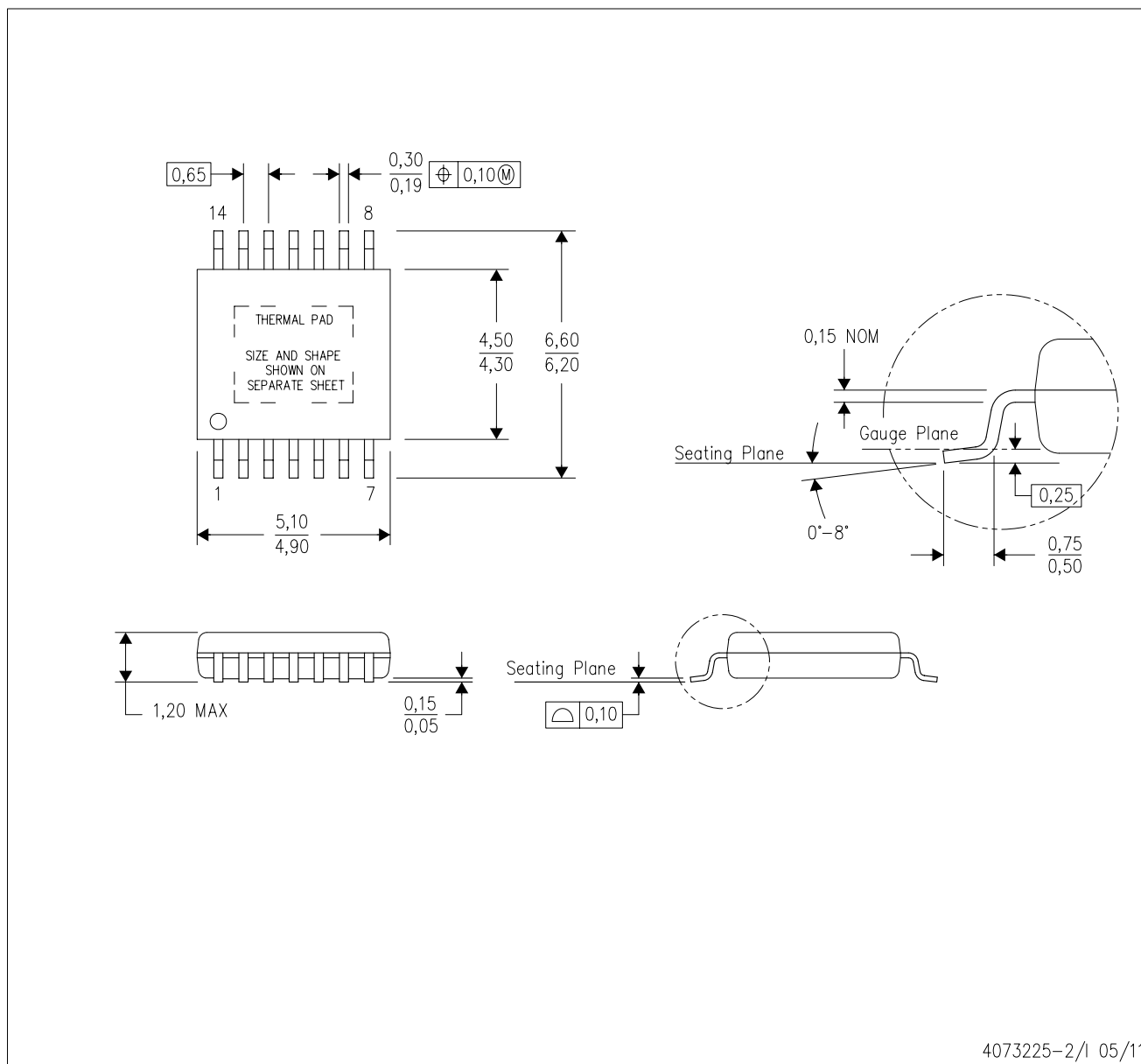
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

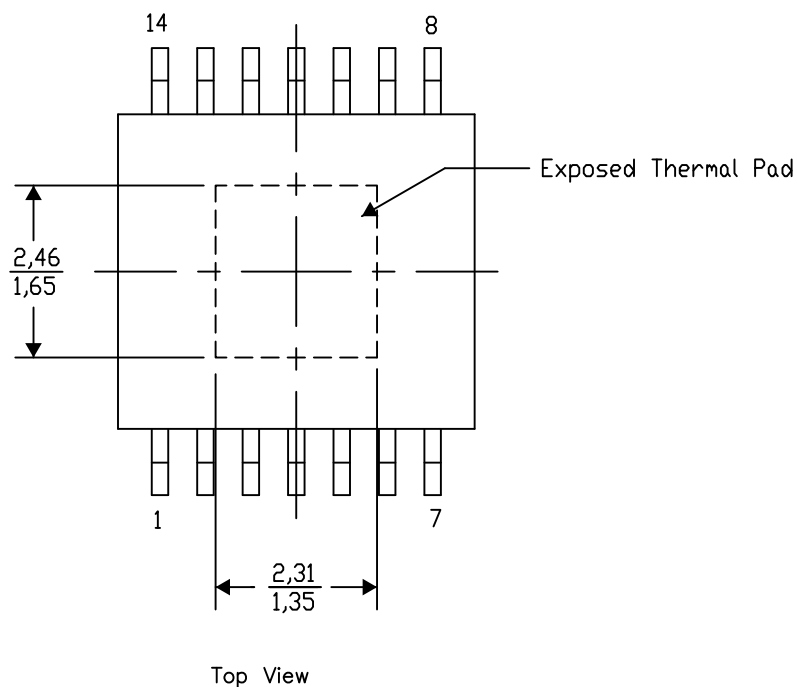
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



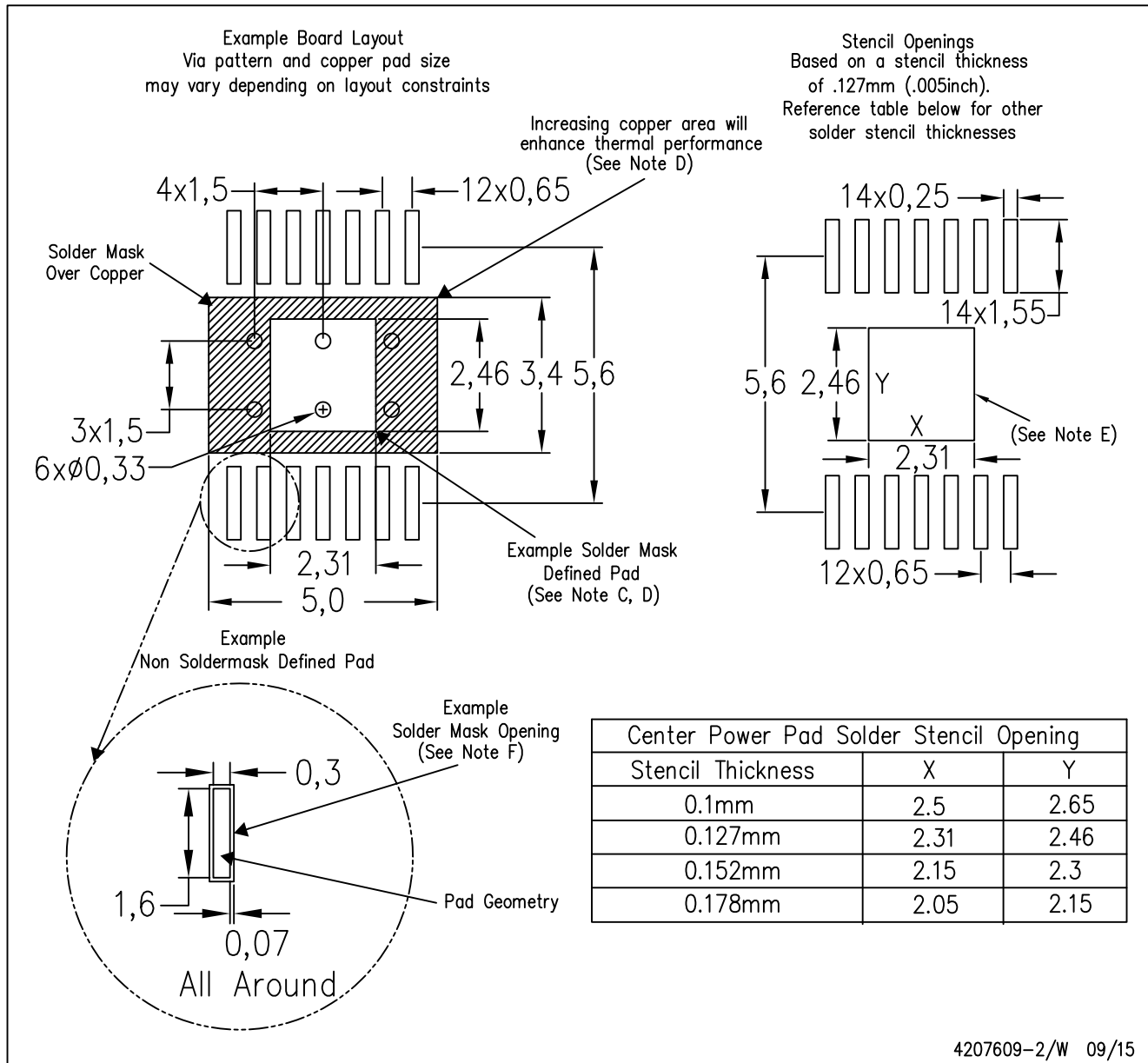
Exposed Thermal Pad Dimensions

4206332-2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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