PRELIMINARY DATA SHEET

SD1200

Analog-Interface XGA/SXGA TFT

LCD Display Controller

September 1998

SmartASIC, Inc.

SD1200 PRELIMINARY DATA SHEET

PRSD-1200-A

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SD1200

Analog-Interface XGA/SXGA TFT LCD Display Controller

Features

- Highly integrated analog interface XGA/SXGA TFT LCD Display Controller
- Handle both 24-bit and 48-bit sampled RGB input up to SXGA (1280x1024) @ 85Hz
- Support various PC graphics cards
- Drive 48-bit digital RGB output up to SXGA (1280x1024) @ 75Hz
- Support various TFT LCD panels
- Truly "Plug and Display" no special driver running on PC
- Implement proprietary ***SmartDisplay*** technology for
  - input mode detection and auto calibration
  - output image scaling and interpolation
  - 16.7 million true color support for 6 bit panel
  - robust detection and handling of invalid input modes
- Advanced input mode detection and auto calibration
  - input refresh rate detection
  - input format detection
  - input sync polarity detection
  - image expansion
  - input frequency detection
  - optimal sampling clock phase calibration
- Advanced image scaling and interpolation with
  - automatic image centering
  - automatic image expansion in both horizontal and vertical directions
  - programmable horizontal and vertical expansion ratio
  - programmable horizontal and vertical interpolation algorithm
- True color support for 6 bit panel
  - Proprietary dithering based on both intensity and spatial information
  - Optional frame modulation
- Robust handling of invalid input conditions
  - detect no input signal
  - detect input signal beyond specified acceptable range
  - output status indicators
  - generate output signal even when no input signal
- Support multiple TFT LCD panels
  - programmable output timing parameters to match specifications of various TFT LCD panels
  - support power On/Off sequence
  - Output signal is synchronized with the input signal with the same frame rate
- Low-cost system solution
  - no external frame buffer required
  - 2-wire I^2C serial interface for EEPROM and CPU
  - programmable OSD mixer
  - direct interface to external ADC's and PLL's
  - 160 pin PQFP Package
  - 5.0V and 3.3V supply



1. OVERVIEW

The SD1200 is an IC designed for analog-interface XGA/SXGA TFT LCD monitors. An analog-interface LCD monitor takes analog RGB signals from a graphic card of a personal computer, the exact same input interface as a conventional CRT monitor. This feature makes analog-interface LCD monitor a true replacement of a conventional CRT monitor.

The analog input RGB signals are first sampled by six channels of 8-bit A/D converters, and the 48-bit RGB data are then fed into the SD1200. The SD1200 is capable of performing automatic detection of the display resolution and timing of input signals generated from various PC graphic cards. No special driver is required for the timing detection, nor does any manual adjustment. The SD1200 then automatically scales the input image to fill the full screen of the LCD monitor. The SD1200 can interface with TFT LCD panels from various manufacturers by generating 48-bit RGB signal to the LCD panel based upon the timing parameters saved in the EEPROM.

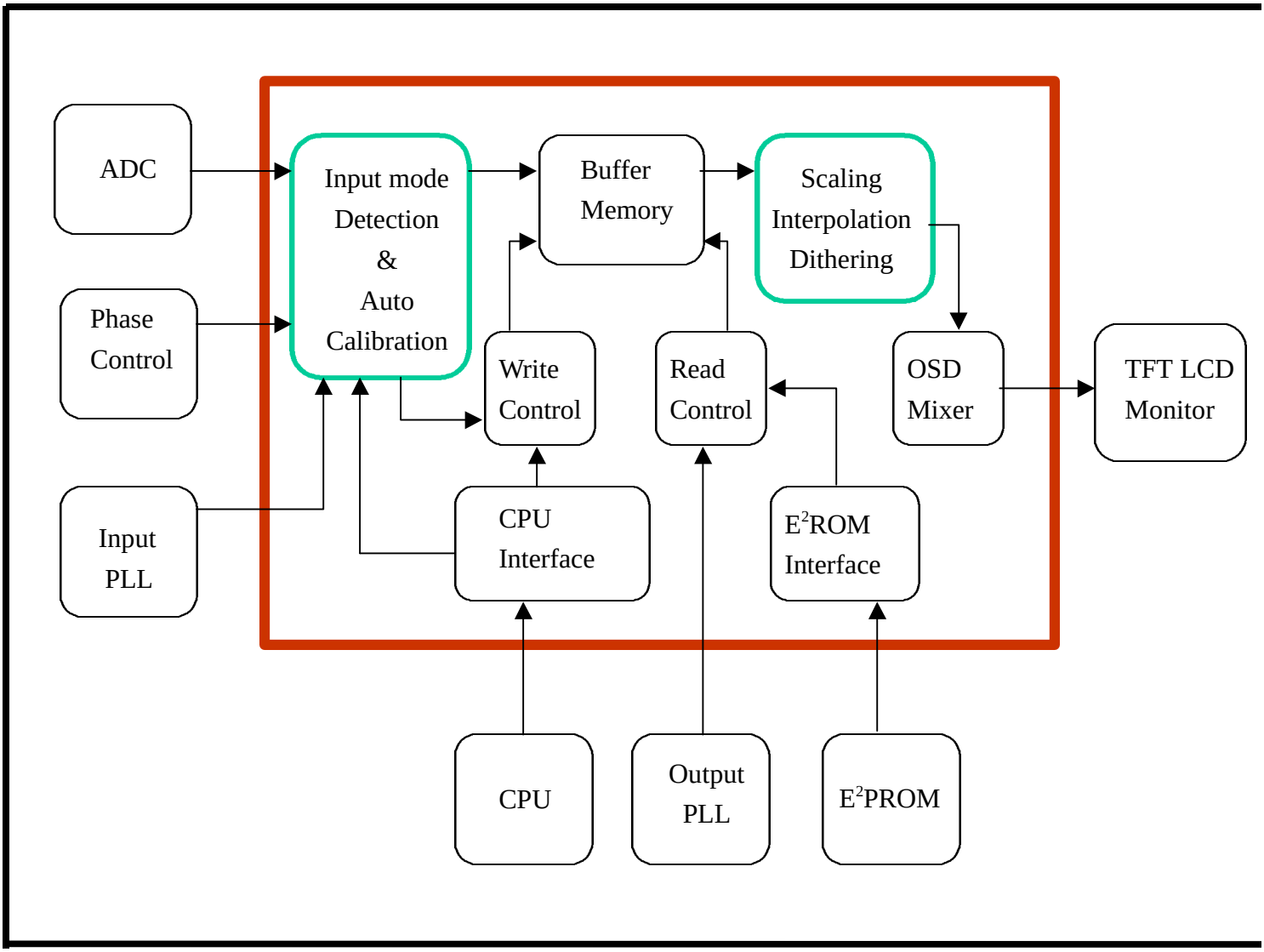
The SD1200 provides two distinguished features to the TFT LCD monitor solution. The first one is “plug-and-play”, and the second one is “cost-effective system solution”. To be truly plug-and-display, the SD1200 performs automatic input mode detection and auto phase calibration, so that the LCD monitor can ensure the A/D converters’ sample clock to be precisely synchronized with the input video data, and to preserve the highest image bandwidth for the highest image quality. Furthermore, the SD1200 can generate output video even when the input signal is beyond the specifications, or no input signal is fed.

For “cost-effective system solution”, the SD1200 implements many system support features such as OSD mixer, error status indicators, 2-wire I^2C serial interface for both EEPROM and host CPU interface, and low-cost IC package. Another important contributing factor is that SD1200 does not require external frame buffer memory for the automatic image scaling and synchronization.

The SD1200 can handle input signal up to SXGA (1280x1024) resolution at 75Hz refresh rate, and produce output signal at SXGA resolution at 75Hz refresh rate (subject to the limitation of LCD panel).

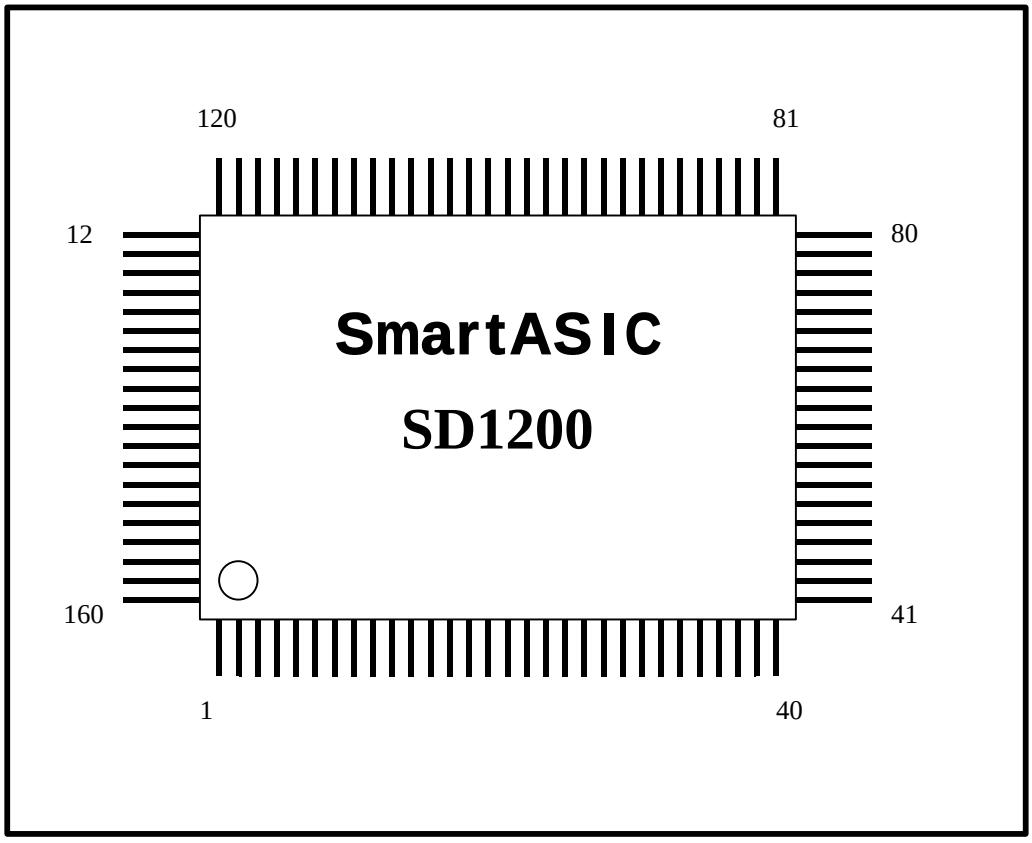
Figure 1 shows the block diagram of the SD1200 as well as the connections of important system components around the SD1200.

Figure 1: SD1200 Functional Block Diagram



2. PIN DESCRIPTION

Figure 2: SD1200 package diagram



able 1: SD1200 pin description (sorted by pin number)

Symbol	PIN Number	Voltage	I/O	Description
B_IN06	1	5	I	Input Color Blue
B_IN07	2	5	I	Input Color Blue
B_IN10	3	5	I	Input Color Blue
B_IN11	4	5	I	Input Color Blue
B_IN12	5	5	I	Input Color Blue
B_IN13	6	5	I	Input Color Blue
DATA_SEL	7	5	I	Select Input Odd/Even Data
B_IN14	8	5	I	Input Color Blue
B_IN15	9	5	I	Input Color Blue
B_IN16	10	5	I	Input Color Blue
B_IN17	11	5	I	Input Color Blue
GND	12			Ground
HSYNC_I	13	5	I	Input HSYNC (active LOW)
VSYNC_I	14	5	I	Input VSYNC (active LOW)
MODE_IN0	15	5	I	Input Mode Select 1: double 24 bit RGB 0: single 24 bit RGB
MODE_IN1	16	5	I	Device ID bit 4 for CPU Interface (Pull High Internally)
VDD_5V	17	5		+5V Power Supply
MODE_IN2	18	5	I	Device ID bit 5 for CPU Interface (Pull High Internally)
MODE_IN3	19	5	I	Device ID bit 6 for CPU Interface (Pull High Internally)
ROM_SCL	20	5	O	SCL in I^2C for EEPROM interface
ROM_SDA	21	5	I/O	SDA in I^2C for EEPROM interface
GND	22			Ground
CPU_SCL	23	5	I	SCL in I^2C for CPU interface
CPU_SDA	24	5	I/O	SDA in I^2C for CPU interface
PWM_CTL	25	5	O	PWM control signal (Detail description in PWM Operation Section)
CLK_1M	26	5	I	Free Running Clock (default: 1MHz)
VDD_5V	27	5		+5V Power Supply
CLK_1M_O	28	5	O	Feedback of free Running Clock
RESET_B	29	5	I	System Reset (active LOW)
R_OSD	30	5	I	OSD Color Red
G_OSD	31	5	I	OSD Color Green
B_OSD	32	5	I	OSD Color Blue
EN_OSD	33	5	I	OSD Mixer Enable =0, No OSD output =1,R_OUT[7:0]= {R_OSD repeat 8 times} G_OUT[7:0]= {G_OSD repeat 8 times } B_OUT[7:0]= {B_OSD repeat 8 times }
SCAN_EN	34	5	1	Manufacturing test pin (NC)
TEST_EN	35	5	I	Manufacturing test pin (NC)
TEST_H	36	5	I	Manufacturing test pin (NC)
TST_DONE	37	5	O	Manufacturing test pin (NC)
FAIL_H	38	5	O	Manufacturing test pin (NC)
HSYNC_X	39	5	O	Default HSYNC generated by ASIC (active

				LOW)
VSYNC_X	40	5	O	Default VSYNC generated by ASIC (active LOW)
GND	41			Ground
FCLK0	42	5	O	Input PLL Feedback Clock
VCLK0	43	5	I	Input PLL Output Clock
FCLK1	44	5	O	Output PLL Feedback Clock
VCLK1	45	5	I	Output PLL Output Clock
HSYNC_O	46	3.3	O	Output HSYNC
VSYNC_O	47	3.3	O	Output VSYNC
DCLK_OUT	48	3.3	O	Output Clock to Control Panel
DE_OUT	49	3.3	O	Output Display Enable for Panel (active HIGH)
VDD_5V	50	5		+5V Power Supply
R_OUT0_E	51	3.3	O	Output Color Red Even Pixel
R_OUT1_E	52	3.3	O	Output Color Red Even Pixel
R_OUT2_E	53	3.3	O	Output Color Red Even Pixel
R_OUT3_E	54	3.3	O	Output Color Red Even Pixel
VDD_3.3V	55	3.3		+3.3V Power Supply
R_OUT4_E	56	3.3	O	Output Color Red Even Pixel
R_OUT5_E	57	3.3	O	Output Color Red Even Pixel
R_OUT6_E	58	3.3	O	Output Color Red Even Pixel
R_OUT7_E	59	3.3	O	Output Color Red Even Pixel
GND	60			Ground
R_OUT0_O	61	3.3	O	Output Color Red Odd Pixel
R_OUT1_O	62	3.3	O	Output Color Red Odd Pixel
R_OUT2_O	63	3.3	O	Output Color Red Odd Pixel
R_OUT3_O	64	3.3	O	Output Color Red Odd Pixel
VDD_5V	65	5		+5V Power Supply
R_OUT4_O	66	3.3	O	Output Color Red Odd Pixel
R_OUT5_O	67	3.3	O	Output Color Red Odd Pixel
R_OUT6_O	68	3.3	O	Output Color Red Odd Pixel
R_OUT7_O	69	3.3	O	Output Color Red Odd Pixel
GND	70			Ground
G_OUT0_E	71	3.3	O	Output Color Green Even Pixel
G_OUT1_E	72	3.3	O	Output Color Green Even Pixel
G_OUT2_E	73	3.3	O	Output Color Green Even Pixel
G_OUT3_E	74	3.3	O	Output Color Green Even Pixel
G_OUT4_E	75	3.3	O	Output Color Green Even Pixel
VDD_3.3V	76	3.3		+3.3V Power Supply
G_OUT5_E	77	3.3	O	Output Color Green Even Pixel
G_OUT6_E	78	3.3	O	Output Color Green Even Pixel
G_OUT7_E	79	3.3	O	Output Color Green Even Pixel
GND	80			Ground
G_OUT0_O	81	3.3	O	Output Color Green Odd Pixel
G_OUT1_O	82	3.3	O	Output Color Green Odd Pixel
G_OUT2_O	83	3.3	O	Output Color Green Odd Pixel
G_OUT3_O	84	3.3	O	Output Color Green Odd Pixel
VDD_5V	85	5		+5V Power Supply
G_OUT4_O	86	3.3	O	Output Color Green Odd Pixel
G_OUT5_O	87	3.3	O	Output Color Green Odd Pixel
G_OUT6_O	88	3.3	O	Output Color Green Odd Pixel
G_OUT7_O	89	3.3	O	Output Color Green Odd Pixel

GND	90			Ground
B_OUT0_E	91	3.3	O	Output Color Blue Even Pixel
B_OUT1_E	92	3.3	O	Output Color Blue Even Pixel
B_OUT2_E	93	3.3	O	Output Color Blue Even Pixel
B_OUT3_E	94	3.3	O	Output Color Blue Even Pixel
B_OUT4_E	95	3.3	O	Output Color Blue Even Pixel
B_OUT5_E	96	3.3	O	Output Color Blue Even Pixel
B_OUT6_E	97	3.3	O	Output Color Blue Even Pixel
VDD_3.3V	98	3.3		+3.3V Power Supply
B_OUT7_E	99	3.3	O	Output Color Blue Even Pixel
GND	100			Ground
B_OUT0_O	101	3.3	O	Output Color Blue Odd Pixel
B_OUT1_O	102	3.3	O	Output Color Blue Odd Pixel
B_OUT2_O	103	3.3	O	Output Color Blue Odd Pixel
B_OUT3_O	104	3.3	O	Output Color Blue Odd Pixel
VDD_5V	105	5		+5V Power Supply
B_OUT4_O	106	3.3	O	Output Color Blue Odd Pixel
B_OUT5_O	107	3.3	O	Output Color Blue Odd Pixel
B_OUT6_O	108	3.3	O	Output Color Blue Odd Pixel
B_OUT7_O	109	3.3	O	Output Color Blue Odd Pixel
GND	110			Ground
R_IN00	111	5	I	Input Color Red
R_IN01	112	5	I	Input Color Red
R_IN02	113	5	I	Input Color Red
R_IN03	114	5	I	Input Color Red
VDD_5V	115	5		+5V Power Supply
R_IN04	116	5	I	Input Color Red
R_IN05	117	5	I	Input Color Red
R_IN06	118	5	I	Input Color Red
R_IN07	119	5	I	Input Color Red
GND	120			Ground
R_IN10	121	5	I	Input Color Red
R_IN11	122	5	I	Input Color Red
R_IN12	123	5	I	Input Color Red
R_IN13	124	5	I	Input Color Red
VDD_5V	125	5		+5V Power Supply
R_IN14	126	5	I	Input Color Red
R_IN15	127	5	I	Input Color Red
R_IN16	128	5	I	Input Color Red
R_IN17	129	5	I	Input Color Red
GND	130			Ground
G_IN00	131	5	I	Input Color Green
G_IN01	132	5	I	Input Color Green
G_IN02	133	5	I	Input Color Green
G_IN03	134	5	I	Input Color Green
VDD_5V	135	5		+5V Power Supply
G_IN04	136	5	I	Input Color Green
G_IN05	137	5	I	Input Color Green
ADC_CLK0	138	5	O	Sample Clock for ADC 0
G_IN06	139	5	I	Input Color Green
G_IN07	140	5	I	Input Color Green
GND	141			Ground

G_IN10	142	5	I	Input Color Green
G_IN11	143	5	I	Input Color Green
ADC_CLK1	144	5	O	Sample Clock for ADC 1
G_IN12	145	5	I	Input Color Green
G_IN13	146	5	I	Input Color Green
VDD_5V	147	5		+5V Power Supply
G_IN14	148	5	I	Input Color Green
G_IN15	149	5	I	Input Color Green
G_IN16	150	5	I	Input Color Green
G_IN17	151	5	I	Input Color Green
GND	152			Ground
B_IN00	153	5	I	Input Color Blue
B_IN01	154	5	I	Input Color Blue
B_IN02	155	5	I	Input Color Blue
B_IN03	156	5	I	Input Color Blue
VDD_5V	157	5		+5V Power Supply
B_IN04	158	5	I	Input Color Blue
B_IN05	159	5	I	Input Color Blue
GND	160			Ground

Table 2: SD1200 pin description (sorted by function)

Symbol	PIN Number	Voltage	I/O	Description
R_IN00	111	5	I	Input Color Red
R_IN01	112	5	I	Input Color Red
R_IN02	113	5	I	Input Color Red
R_IN03	114	5	I	Input Color Red
R_IN04	116	5	I	Input Color Red
R_IN05	117	5	I	Input Color Red
R_IN06	118	5	I	Input Color Red
R_IN07	119	5	I	Input Color Red
R_IN10	121	5	I	Input Color Red
R_IN11	122	5	I	Input Color Red
R_IN12	123	5	I	Input Color Red
R_IN13	124	5	I	Input Color Red
R_IN14	126	5	I	Input Color Red
R_IN15	127	5	I	Input Color Red
R_IN16	128	5	I	Input Color Red
R_IN17	129	5	I	Input Color Red
G_IN00	131	5	I	Input Color Green
G_IN01	132	5	I	Input Color Green
G_IN02	133	5	I	Input Color Green
G_IN03	134	5	I	Input Color Green
G_IN04	136	5	I	Input Color Green
G_IN05	137	5	I	Input Color Green
G_IN06	139	5	I	Input Color Green
G_IN07	140	5	I	Input Color Green
G_IN10	142	5	I	Input Color Green
G_IN11	143	5	I	Input Color Green
G_IN12	145	5	I	Input Color Green
G_IN13	146	5	I	Input Color Green
G_IN14	148	5	I	Input Color Green
G_IN15	149	5	I	Input Color Green
G_IN16	150	5	I	Input Color Green
G_IN17	151	5	I	Input Color Green
B_IN00	153	5	I	Input Color Blue
B_IN01	154	5	I	Input Color Blue
B_IN02	155	5	I	Input Color Blue
B_IN03	156	5	I	Input Color Blue
B_IN04	158	5	I	Input Color Blue
B_IN05	159	5	I	Input Color Blue
B_IN06	1	5	I	Input Color Blue
B_IN07	2	5	I	Input Color Blue
B_IN10	3	5	I	Input Color Blue
B_IN11	4	5	I	Input Color Blue
B_IN12	5	5	I	Input Color Blue
B_IN13	6	5	I	Input Color Blue
B_IN14	8	5	I	Input Color Blue
B_IN15	9	5	I	Input Color Blue
B_IN16	10	5	I	Input Color Blue
B_IN17	11	5	I	Input Color Blue

HSYNC_I	13	5	I	Input HSYNC (active LOW)
VSYNC_I	14	5	I	Input VSYNC (active LOW)
MODE_IN0	15	5	I	Input Mode Select 1: double 24 bit RGB 0: single 24 bit RGB
MODE_IN1	16	5	I	Device ID bit 4 for CPU Interface (Pull High Internally)
MODE_IN2	18	5	I	Device ID bit 5 for CPU Interface (Pull High Internally)
MODE_IN3	19	5	I	Device ID bit 6 for CPU Interface (Pull High Internally)
ADC_CLK0	138	5	O	Sample Clock for ADC 0
ADC_CLK1	144	5	O	Sample Clock for ADC 1
R_OUT0_E	51	3.3	O	Output Color Red Even Pixel
R_OUT1_E	52	3.3	O	Output Color Red Even Pixel
R_OUT2_E	53	3.3	O	Output Color Red Even Pixel
R_OUT3_E	54	3.3	O	Output Color Red Even Pixel
R_OUT4_E	56	3.3	O	Output Color Red Even Pixel
R_OUT5_E	57	3.3	O	Output Color Red Even Pixel
R_OUT6_E	58	3.3	O	Output Color Red Even Pixel
R_OUT7_E	59	3.3	O	Output Color Red Even Pixel
R_OUT0_O	61	3.3	O	Output Color Red Odd Pixel
R_OUT1_O	62	3.3	O	Output Color Red Odd Pixel
R_OUT2_O	63	3.3	O	Output Color Red Odd Pixel
R_OUT3_O	64	3.3	O	Output Color Red Odd Pixel
R_OUT4_O	66	3.3	O	Output Color Red Odd Pixel
R_OUT5_O	67	3.3	O	Output Color Red Odd Pixel
R_OUT6_O	68	3.3	O	Output Color Red Odd Pixel
R_OUT7_O	69	3.3	O	Output Color Red Odd Pixel
G_OUT0_E	71	3.3	O	Output Color Green Even Pixel
G_OUT1_E	72	3.3	O	Output Color Green Even Pixel
G_OUT2_E	73	3.3	O	Output Color Green Even Pixel
G_OUT3_E	74	3.3	O	Output Color Green Even Pixel
G_OUT4_E	75	3.3	O	Output Color Green Even Pixel
G_OUT5_E	77	3.3	O	Output Color Green Even Pixel
G_OUT6_E	78	3.3	O	Output Color Green Even Pixel
G_OUT7_E	79	3.3	O	Output Color Green Even Pixel
G_OUT0_O	81	3.3	O	Output Color Green Odd Pixel
G_OUT1_O	82	3.3	O	Output Color Green Odd Pixel
G_OUT2_O	83	3.3	O	Output Color Green Odd Pixel
G_OUT3_O	84	3.3	O	Output Color Green Odd Pixel
G_OUT4_O	86	3.3	O	Output Color Green Odd Pixel
G_OUT5_O	87	3.3	O	Output Color Green Odd Pixel
G_OUT6_O	88	3.3	O	Output Color Green Odd Pixel
G_OUT7_O	89	3.3	O	Output Color Green Odd Pixel
B_OUT0_E	91	3.3	O	Output Color Blue Even Pixel
B_OUT1_E	92	3.3	O	Output Color Blue Even Pixel
B_OUT2_E	93	3.3	O	Output Color Blue Even Pixel

B_OUT3_E	94	3.3	O	Output Color Blue Even Pixel
B_OUT4_E	95	3.3	O	Output Color Blue Even Pixel
B_OUT5_E	96	3.3	O	Output Color Blue Even Pixel
B_OUT6_E	97	3.3	O	Output Color Blue Even Pixel
B_OUT7_E	99	3.3	O	Output Color Blue Even Pixel
B_OUT0_O	101	3.3	O	Output Color Blue Odd Pixel
B_OUT1_O	102	3.3	O	Output Color Blue Odd Pixel
B_OUT2_O	103	3.3	O	Output Color Blue Odd Pixel
B_OUT3_O	104	3.3	O	Output Color Blue Odd Pixel
B_OUT4_O	106	3.3	O	Output Color Blue Odd Pixel
B_OUT5_O	107	3.3	O	Output Color Blue Odd Pixel
B_OUT6_O	108	3.3	O	Output Color Blue Odd Pixel
B_OUT7_O	109	3.3	O	Output Color Blue Odd Pixel
HSYNC_O	46	3.3	O	Output HSYNC
VSYNC_O	47	3.3	O	Output VSYNC
DCLK_OUT	48	3.3	O	Output Clock to Control Panel
DE_OUT	49	3.3	O	Output Display Enable for Panel (active HIGH)
FCLK0	42	5	O	Input PLL Feedback Clock
VCLK0	43	5	I	Input PLL Output Clock
FCLK1	44	5	O	Output PLL Feedback Clock
VCLK1	45	5	I	Output PLL Output Clock
ROM_SCL	20	5	O	SCL in I^2C for EEPROM interface
ROM_SDA	21	5	I/O	SDA in I^2C for EEPROM interface
CPU_SCL	23	5	I	SCL in I^2C for CPU interface
CPU_SDA	24	5	I/O	SDA in I^2C for CPU interface
PWM_CTL	25	5	O	PWM control signal (Detail description in PWM Operation Section)
CLK_1M	26	5	I	Free Running Clock (default: 1MHz)
CLK_1M_O	28	5	O	Feedback of free Running Clock
RESET_B	29	5	I	System Reset (active LOW)
HSYNC_X	39	5	O	Default HSYNC generated by ASIC (active LOW)
VSYNC_X	40	5	O	Default VSYNC generated by ASIC (active LOW)
R_OSD	30	5	I	OSD Color Red
G_OSD	31	5	I	OSD Color Green
B_OSD	32	5	I	OSD Color Blue
EN_OSD	33	5	I	OSD Mixer Enable =0, No OSD output =1,R_OUT[7:0]= {R_OSD repeat 8 times} G_OUT[7:0]= {G_OSD repeat 8 times } B_OUT[7:0]= {B_OSD repeat 8 times }
SCAN_EN	34	5	1	Manufacturing test pin (NC)
TEST_H	36	5	I	Manufacturing test pin (NC)

FAIL_H	38	5	O	Manufacturing test pin (NC)
TST_DONE	37	5	O	Manufacturing test pin (NC)
TEST_EN	35	5	I	Manufacturing test pin (NC)
DATA_SEL	7	5	I	Select Input Odd/Even Data
VDD_5V	17	5		+5V Power Supply
VDD_5V	27	5		+5V Power Supply
VDD_5V	50	5		+5V Power Supply
VDD_5V	65	5		+5V Power Supply
VDD_5V	85	5		+5V Power Supply
VDD_5V	105	5		+5V Power Supply
VDD_5V	115	5		+5V Power Supply
VDD_5V	125	5		+5V Power Supply
VDD_5V	135	5		+5V Power Supply
VDD_5V	147	5		+5V Power Supply
VDD_5V	157	5		+5V Power Supply
VDD_3.3V	55	3.3		+3.3V Power Supply
VDD_3.3V	76	3.3		+3.3V Power Supply
VDD_3.3V	98	3.3		+3.3V Power Supply
GND	12			Ground
GND	22			Ground
GND	41			Ground
GND	60			Ground
GND	70			Ground
GND	80			Ground
GND	90			Ground
GND	100			Ground
GND	110			Ground
GND	120			Ground
GND	130			Ground
GND	141			Ground
GND	152			Ground
GND	160			Ground

3. FUNCTIONAL DESCRIPTION

The SD1200 has the following major function blocks:

1. Input mode detection & auto calibration block
2. Buffer memory and read/write control block
3. Image scaling, interpolation and dithering block
4. OSD mixer and LCD interface block
5. EEPROM interface block
6. CPU interface block

The following sections will describe the functionality of these blocks.

3.1. Input mode detection & auto calibration block

3.1.1. Supported input modes

The SD1200 accepts seven different input video modes:

- 640 x 350
- 640 x 400
- 720 x 400
- 640 x 480 (VGA)
- 800 x 600 (SVGA)
- 1024 x 768 (XGA)
- 1280 x 1024 (SXGA)

There is no frame rate restriction on the input modes. However, since the output signal is synchronized with the input signal at the same refresh rate. The input refresh rate has to be within the acceptable range of the LCD panel.

3.1.2. Input mode detection

The SD1200 can automatically detect the mode of the input signal without any user adjustment or driver running on the PC host or external CPU. This block

automatically detects polarity of input synchronization and the sizes of back porch, valid data window and the synchronization pulse width in both vertical and horizontal directions. The size information is then used not only to decide the input resolution, to generate the frequency divider for the input PLL, to lock the PLL output clock with HSYNC, but also to automatically scale the image to full screen, and to synchronize the output signal with the input signal.

The detection logic is always active to automatically detect any changes to the input mode. Users can manually change the input mode information at run time through the CPU interface. Detail operation of the CPU interface is described in Section. “CPU Interface”.

3.1.3. Auto calibration

The SD1200 can automatically calibrate the phase of the sample clock in order to preserve the bandwidth of input signal and get the best quality. The SD1200 implements a proprietary image quality function. During auto-calibration process, the SD1200 continues search for the best phase to optimize the image quality.

The output image may display some jitter and blurring during the auto-calibration process, and the image will become crisp and sharp once the optimum phase is found. User can change the sampling clock phase value by the external CPU. Detail operation of the CPU interface is described in Section. “CPU Interface”.

The auto calibration process can be delayed and even disabled by the external CPU if system designer wants to have his/her own implementation.

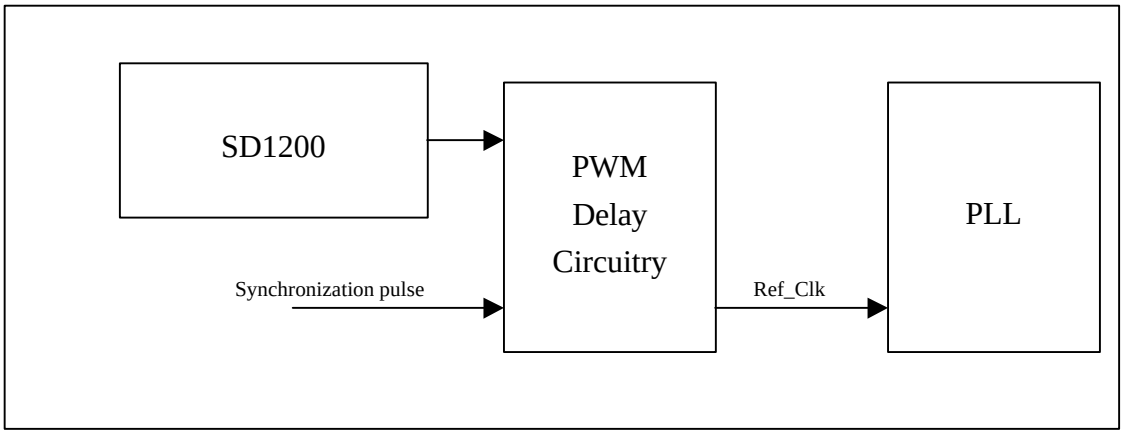
3.1.4. PWM operation

The SD1200 implements a very unique algorithm to adjust the phase of the A/D converter’s sampling clock. An external delay circuitry is required to compliment the SD1200 for the auto-calibration process. The SD1200 generates a Pulse-Width Modulated (PWM) signal to the external delay circuitry. The delay circuitry should insert a certain amount of time delay synchronization pulse based upon the width of the PWM signal. A brief circuit diagram for the PWM is shown in Figure 3.

The PWM signal from the SD1200 is a periodical signal with a period that is 511

times of the period of the free-running clock connected to the pin “CLK_1M”. System manufacturers may select any frequency for the free running clock. The default clock frequency is 1MHz. System manufacturers also decide the unit delay for the external delay circuitry. The delay information is stored in the EEPROM. When the SD1200 wants to delay the synchronization pulse for N units of delay, it will output the PWM with the high time equal to (N * the period of the free-running clock), and with low time equal to (511-N)* the period of the free-running clock. When N=511, the PWM signal stays high all the time, and when N=0, the PWM signal is always low.

Figure 3: SD1200 PWM circuitry block diagram



3.1.5. Free Running Clock

As described in previous section, a free-running clock is needed for the SD1200. This clock is used for many of the SD1200’s internal operations. PWM operation is one of them. System manufacturers can select the frequency of the free-running clock, and the default clock frequency is 1MHz. System manufacturer can use an oscillator to generate the free-running clock, and feed that clock directly to the pin “CLK_1M”, or use a crystal connecting to “CLK_1M” and “CLK_1M_O”.

3.2. Buffer memory and read/write control block

The SD1200 uses internal buffer memory to store a portion of the input image for image scaling and output synchronization. No external memory buffer is needed for the SD1200. The write control logic ensures the input data are stored into the right area of the buffer memory, and the read control logic is responsible to fetch the data from the buffer memory from the correct area and at the correct timing sequence. With the precise timing control of the write and read logic, the output image is appropriately scaled to the full screen, and the output signal is perfectly synchronized with the input signals.

3.3. Image scaling, interpolation and dithering block

The SD1200 supports both automatic image scaling and interpolation.

3.3.1. Image scaling

The SD1200 supports several different input modes, and the input image may have different sizes. It is essential to support automatic image scaling so that the input image is always displayed to the full screen regardless the input mode. The SD1200 scale the images in both horizontal and vertical directions. It calculates the correct scaling ratio for both directions based upon the LCD panel resolution, and the input mode and timing information produced by the “Input mode detection & auto calibration” block. The scaling ratio is re-adjusted whenever a different input mode is detected. The ratio is then fed to the buffer memory read control logic to fetch the image data with the right sequence and timing. Some of the image data may be read more than once to achieve scaling effect.

3.3.2. Image interpolation

The SD1200 supports image interpolation to achieve better image quality. A basic image scaling algorithm replicates the input images to achieve the scaling effect. The replication scheme usually results in a poor image quality. The SD1200 implements both linear interpolation and a proprietary interpolation algorithm. Through external micro-controller, users can chose among different interpolation algorithm.

3.3.3. Dithering

The SD1200 supports 16.7 million true colors for 6-bit panel. Two dithering algorithms are implemented and again users can chose between them through the external micro-controller.

3.4. OSD mixer and LCD interface

At the output stage, the SD1200 performs the OSD mixer function, and then generates 24-bit RGB signal to the LCD panel with the correct timing.

3.4.1. OSD mixer

In the OSD mixer block, the SD1200 mixes the normal output RGB signal with the OSD signal. The OSD output data is generated based on the “R_OSD”, “G_OSD” and “B_OSD” pins as well as the “OSD Intensity” data in EEPROM entry. When the “EN_OSD” is active high, the OSD is active, and the SD1200 will send the OSD data to the LCD panel. The OSD has 16 different color schemes based on the combinations of the three OSD color pins and the “OSD Intensity” data. When R_OSD=1, and OSD_Intensity=0, the SD1200 will output 128 to the output red channel, R_OUT. When R_OSD=1, and OSD_Intensity=1, the SD1200 will output 255. The same scheme is used for G_OSD to G_OUT and for B_OSD to B_OUT.

3.4.2. LCD interface

The SD1200 support 48-bit RGB interface with XGA/SXGA LCD panels from various panel manufacturers. The LCD panel resolution and timing information is stored in the external EEPROM. The information in the EEPROM includes timing related to the output back porch, synchronization pulse width and valid data window. The timing information is used to generate the frequency divider for the output PLL, to lock the PLL output clock with HSYNC for the LCD data clock, and to synchronized the output VSYNC and input VSYNC.

3.5. EEPROM interface

As mentioned in previous sections, the external EEPROM stores much crucial information for the SD1200 internal operations. The SD1200 interfaces with the EEPROM through a 2-wire I^2C serial interface. The suggested EEPROM device is an industry standard serial-interface EEPROM (24x08). The I^2C interface scheme is briefly described here and detail description can be found in many public literatures.

3.5.1. I^2C serial interface

The I^2C serial interface used 2 wires, SCL and SDA. The SCL is driven by the SD1200, and used mainly as the sampling clock and the SDA is a bi-directional signal and used mainly for data signal. Figure 4 shows the basic bit definitions of I^2C serial interface.

The I^2C serial interface supports random read and sequential read operations. Figure 5 and 6 shows the data sequences for random read and sequential read operations.

Figure 4: START, STOP AND DATA Definitions in I^2C serial interface

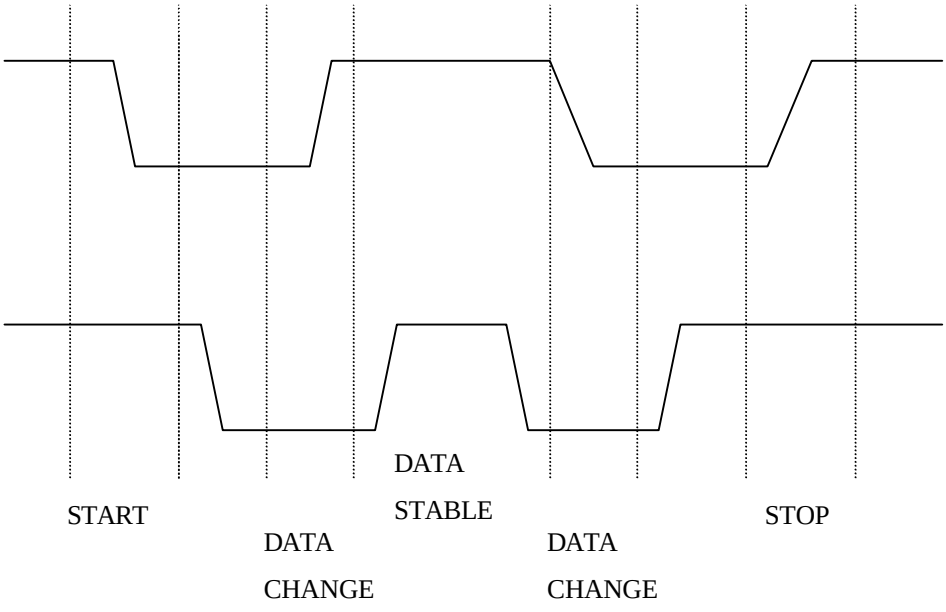


Figure 5: Data sequence for single byte random access

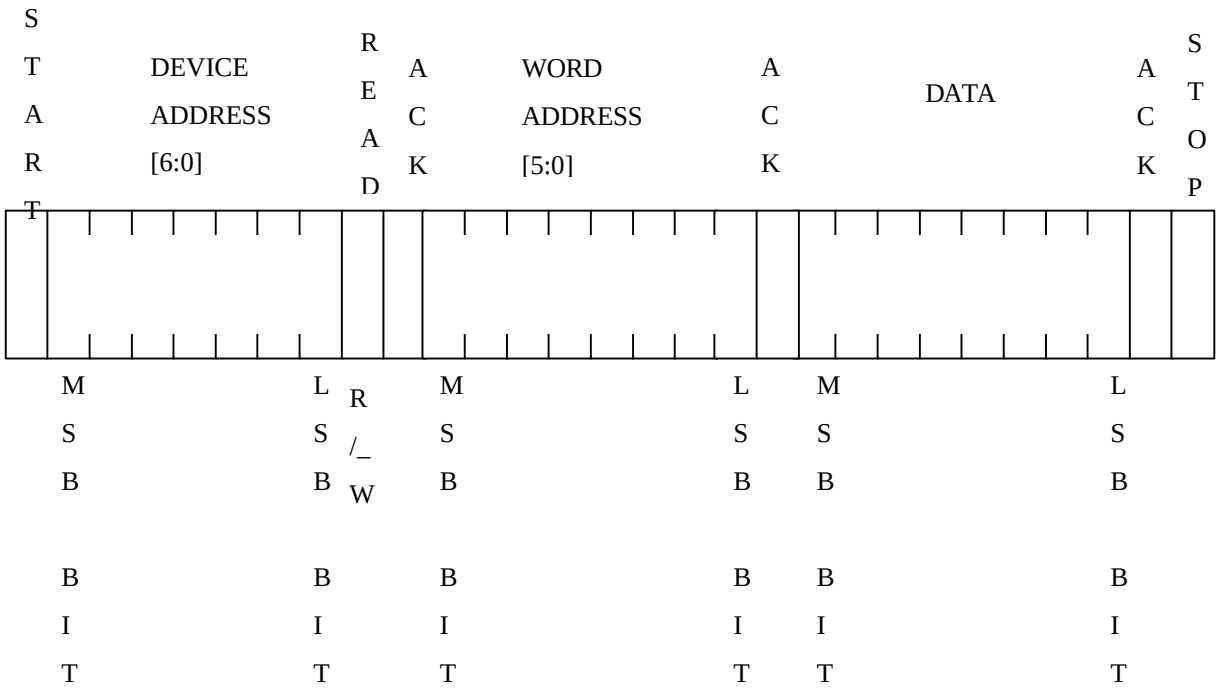
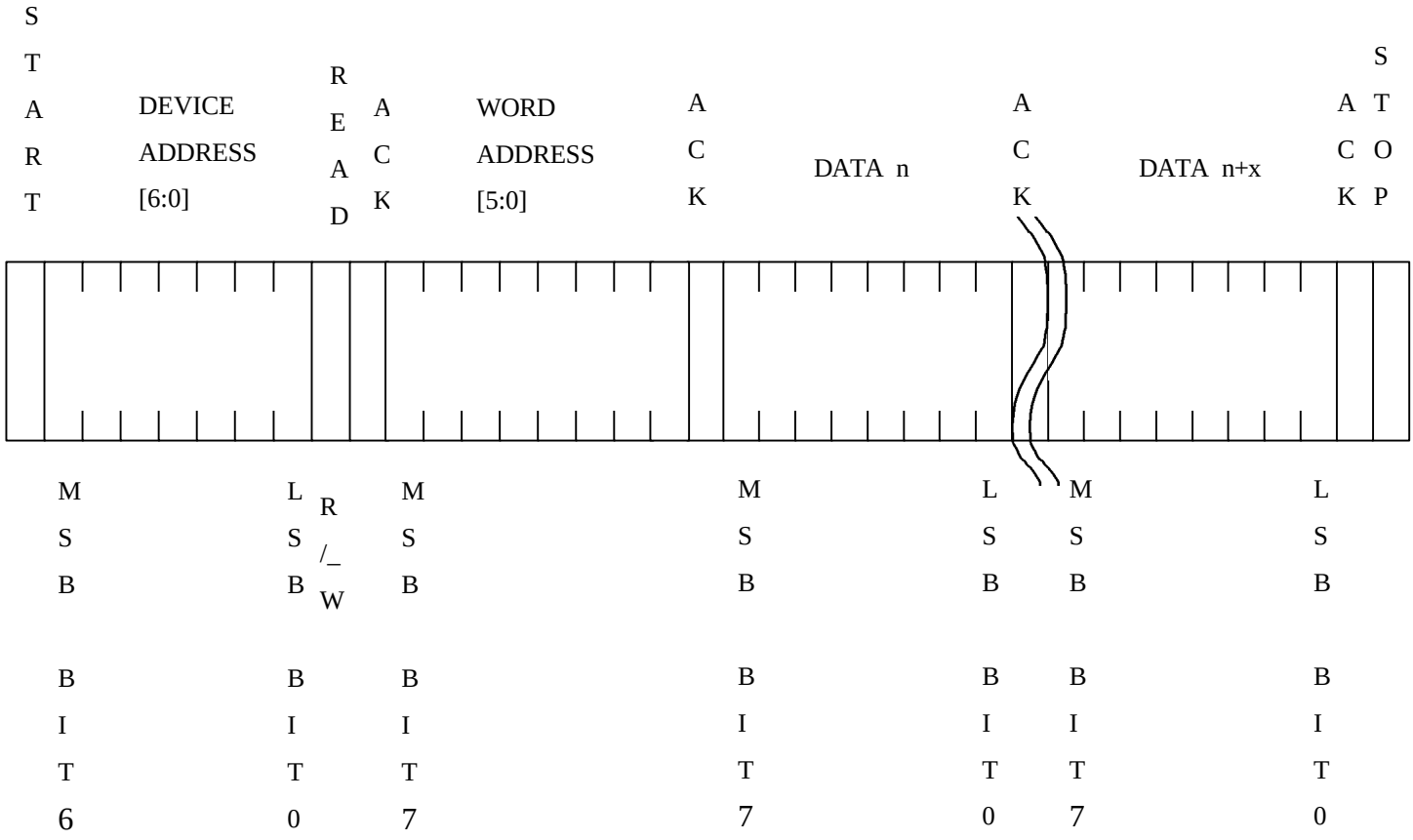


Figure 6: Data sequence for multiple byte sequential access



3.5.2. EEPROM Contents

The contents of EEPROM are primarily dependent on the specifications of the LCD panel. SmartASIC provides suggested EEPROM contents for LCD panels from various panel manufacturers. The section presents all the entries in the EEPROM, and briefly describes their definitions. That allows the system manufacturers to have their own EEPROM contents to distinguish their monitors.

The EEPROM contents can be partitioned into 11 parts. The first 8 parts are input mode dependent. When the SD1200 detects the input mode, it will then load the information related to the detected mode from the EEPROM. The information in the 9^{th} part is mainly for input mode detection as well as some threshold values for error status indicators. The 10^{th} and 11^{th} parts are look up table for interpolation parameters. The 9^{th}, 10^{th} and 11^{th} parts are loaded in the SD1200 during the reset time.

- Part 1: 640x350 mode,
- Part 2: 640x400 mode,
- Part 3: 720x400 mode,
- Part 4: 640x480 mode,
- Part 5: 800x600 mode,
- Part 6: 1024x768 mode,
- Part 7: 1280x1024 mode, and
- Part 8: user defined mode
- Part 9: input mode detection and scaling related parameters
- Part 10: lookup table for horizontal interpolation
- Part 11: lookup table for vertical interpolation

Part 1-8: Input Mode Dependent Data

Symbol	W	640 x 350	640 x 400	720 x 400	640 x 480	800 x 600	1024 x 768	1280 x 1024	INV ALID	Description
VPW	11	00H 01H	20H 21H	40H 41H	60H 61H	80H 81H	A0H A1H	C0H C1H	E0H E1H	LCD VSYNC pulse width
VBP	11	02H 03H	22H 23H	42H 43H	62H 63H	82H 83H	A2H A3H	C2H C3H	E2H E3H	LCD VSYNC back porch (including VPW)
VBP Source	11	04H 05H	24H 25H	44H 45H	64H 65H	84H 85H	A4H A5H	C4H C5H	E4H E5H	LCD VSYNC back porch (source equivalent) = VBP * Line Expansion and round up
Target Skip Pixel	11	06H 07H	26H 27H	46H 47H	66H 67H	86H 87H	A6H A7H	C6H C7H	E6H E7H	If VBP can not be converted into source evenly, the leftover is converted into number of pixels
VSIZE	11	08H 09H	28H 29H	48H 49H	68H 69H	88H 89H	A8H A9H	C8H C9H	E8H E9H	LCD number of lines
HPW	11	0AH 0BH	2AH 2BH	4AH 4BH	6AH 6BH	8AH 8BH	AAH ABH	CAH CBH	EAH EBH	LCD HSYNC pulse width
HBP	11	0CH 0DH	2CH 2DH	4CH 4DH	6CH 6DH	8CH 8DH	ACH ADH	CCH CDH	ECH EDH	LCD HSYNC back porch(including HPW)
HSIZE	11	0EH 0FH	2EH 2FH	4EH 4FH	6EH 6FH	8EH 8FH	AEH AFH	CEH CFH	EEH EFH	LCD number of columns
HTOTAL	11	10H 11H	30H 31H	50H 51H	70H 71H	90H 91H	B0H B1H	D0H D1H	F0H F1H	LCD total number of pixels per line including all porches
HTOTAL Source	12	12H 13H	32H 33H	52H 53H	72H 73H	92H 93H	B2H B3H	D2H D3H	F2H F3H	LCD total number of clocks per line (source equivalent) = HTOTAL/Line Expansion
Line Expansion	4	14H [6:3]	34H [6:3]	54H [6:3]	74H [6:3]	94H [6:3]	B4H [6:3]	D4H [6:3]	F4H [6:3]	Vertical source to destination scaling factor 0: 1 to 1 1: 2 to 3 2: 3 to 4 3: 5 to 8 4: 15 to 32 5: 25 to 32 6: 25 to 48 7: 25 to 64 8: 75 to 128 9: 175 to 384 10: 175 to 512
Pixel Expansion	3	14H [2:0]	34H [2:0]	54H [2:0]	74H [2:0]	94H [2:0]	B4H [2:0]	D4H [2:0]	F4H [2:0]	Horizontal source to destination scaling factor 0: 1 to 1 1: 2 to 4 2: 4 to 5 3: 25 to 36 4: 5 to 8 5: 9 to 10 6: 45 to 64 7: 9 to 16

Fog Factor Horizontal	8	15H	35H	55H	75H	95H	B5H	D5H	F5H	Horizontal fogging factor
Fog Factor 2X	8	16H	36H	56H	76H	96H	B6H	D6H	F6H	Double of Horizontal fogging factor
Fog Factor Vertical	8	17H	37H	57H	77H	97H	B7H	D7H	F7H	Vertical fogging factor
Minimum input lines	11	18H 19H	38H 39H	58H 59H	78H 79H	98H 99H	B8H B9H	D8H D9H	F8H F9H	Minimum input lines = (VSIZE + VBP)* Line Expansion When the input has fewer lines than this value, it is considered as an ERROR, and INPUT_X status bit will be HIGH.
Maximum input pixels	11	1AH 1BH	3AH 3BH	5AH 1BH	7AH 7BH	9AH 9BH	BAH BBH	DAH DBH	FAH FBH	Maximum input pixels per line. Auto clock recovery will not set input PLL divisor larger than this value.
Source HSIZE[11:8]	3	1CH [6:4]	3CH [6:4]	5CH [6:4]	7CH [6:4]	9CH [6:4]	BCH [6:4]	DCH [6:4]	FCH [6:4]	Source horizontal size upper 3 bits
Source VSIZE[11:8]	3	1CH [2:0]	3CH [2:0]	5CH [2:0]	7CH [2:0]	9CH [2:0]	BCH [2:0]	DCH [2:0]	FCH [2:0]	Source vertical size upper 3 bits
Source HSIZE[7:0]	8	1DH	3DH	5DH	7DH	9DH	BDH	DDH	FDH	Source horizontal size lower 8 bits
Source VSIZE[7:0]	8	1EH	3EH	5EH	7EH	9EH	BEH	DEH	FEH	Source vertical size lower 8 bits
Check sum	8	1FH	3FH	5FH	7FH	9FH	BFH	DFH	FFH	Sum of above 31 bytes (keep lower 8 bits only)

Part 9: Input Mode Detection Data

Symbol	Width (bits)	Address	Description
Data low threshold	8	120H	Low water mark for valid data If the data is smaller than this threshold, it is considered LOW internally
Data high threshold	8	121H	High water mark for valid data If the data is larger than this threshold, it is considered HIGH internally
Edge threshold	8	122H	Minimum difference between the data value of two adjacent pixels to be considered as an edge
Calibration mode	2	123H [1:0]	This is to select different operation modes of internal phase calibration. The selection criterion is as follow: 0: when input video signal has large overshot, it results in longest calibration time 1: when input video signal has median overshot, it results in long calibration time 2: when input video signal has normal overshot, it results in normal calibration time (recommended) 3: when input video signal has no overshot, it results in shortest calibration time
Res0 threshold	10	124H-125H	Upper bound of the line number for 640x350 mode, and lower bound for 640x400
Res1 threshold	10	126H-127H	Upper bound of the line number for 640x400 mode,

			and lower bound for 720x400
Res2 threshold	10	128H-129H	Upper bound of the line number for 720x400 mode, and lower bound for 640x480
Res3 threshold	10	12AH-12BH	Upper bound of the line number for 640x480 mode, and lower bound for 800x600
Res4 threshold	10	12CH-12DH	Upper bound of the line number for 800x600 mode, and lower bound for 1024x768
Res5 threshold	10	12EH-12FH	Upper bound of the line number for 1024x768 mode, and lower bound for 1280x1024
Res6 threshold	10	130H-131H	Upper bound of the line number for 1280x1024 mode. If the input has more line than this threshold, it is considered INVALID mode
Mode 640x350 Sync Polarity	2	132H[1:0]	The polarity of input synchronization signals Bit 0 is for VSYNC and bit 1 is for HSYNC
Mode 640x400 Sync Polarity	2	132H[3:2]	The polarity of input synchronization signals Bit 0 is for VSYNC and bit 1 is for HSYNC
Mode 720x400 Sync Polarity	2	132H[5:4]	The polarity of input synchronization signals Bit 0 is for VSYNC and bit 1 is for HSYNC
Mode 640x480 Sync Polarity	2	132H[7:6]	The polarity of input synchronization signals Bit 0 is for VSYNC and bit 1 is for HSYNC
Mode 800x600 Sync Polarity	2	133H[1:0]	The polarity of input synchronization signals Bit 0 is for VSYNC and bit 1 is for HSYNC
Mode 1024x768 Sync Polarity	2	133H[3:2]	The polarity of input synchronization signals Bit 0 is for VSYNC and bit 1 is for HSYNC
Mode 1280x1024 Sync Polarity	2	133H[5:4]	The polarity of input synchronization signals Bit 0 is for VSYNC and bit 1 is for HSYNC
Maximum VBP	8	134H	The maximum vertical back porch for input video
PWM unit delay	13	135H-136H	The unit delay used in the external PWM delay circuitry. If the free-running clock is 1MHz, and the intended unit delay is 0.2 ns (= 5,000MHz), then a value of 5,000MHz/1MHz = 5,000 is used here.
Maximum link off time	22	137H-139H	Maximum time when input VSYNC is off before the LINK_DWN pin turns ON (unit: clock period of the free running clock). If the free-running clock is 1MHz, and the intended maximum time is 1 second, then a value of 1,000,000 us/ 1 us = 1,000,000 is used here.
Maximum refresh rate	16	13AH-13BH	Maximum refresh rate supported by the LCD panel If the intended maximum refresh rate is 75Hz, and the free-running clock is 1MHz, then a value of 1000000/75=133,333 is used here
Maximum input frequency	8	13CH	Maximum source clock rate supported by the SD1200 (unit: frequency of free-running clock) If the intended maximum clock rate is 60MHz, and the free-running clock is 1MHz, then a value of 60 is used here. If the input signal has a higher frequency than this value, the VCLK0_X status bit will turn ON.
Scale factor CE	8	13DH	Scale factor used when generate look up table for current even pixel multiplication
Scale factor CO	8	13EH	Scale factor used when generate look up table for current odd pixel multiplication
Scale factor NE	8	13FH	Scale factor used when generate look up table for next even pixel multiplication

Scale factor NO	8	140H	Scale factor used when generate look up table for next odd pixel multiplication
Offset factor CE	8	141H	Offset factor used when generate look up table for current even pixel multiplication
Offset factor CO	8	142H	Offset factor used when generate look up table for current odd pixel multiplication
Offset factor NE	8	143H	Offset factor used when generate look up table for next even pixel multiplication
Offset factor NO	8	144H	Offset factor used when generate look up table for next odd pixel multiplication
Scale factor V	8	145H	Scale factor used when generate look up table for line multiplication
Offset factor V	8	146H	Offset factor used when generate look up table for line multiplication
Minimum pixels per line for LCD	11	147H-148H	Minimum number of pixels per line for LCD panel
LCD polarity	4	149H[3:0]	Controls the polarity of output VSYNC, HSYNC, clock and display enable Bit0: 0: clock active high, 1: clock active low Bit1: 0: HSYNC active low, 1: HSYNC active high Bit2: 0: VSYNC active low, 1: VSYNC active high Bit4: 0: de active high, 1: de active low
Check sum	8	14AH	Sum of all part 9 bytes (keep only lower 8 bit)

Part 10: Horizontal Interpolation Lookup Table

Symbol	Width (bits)	Address	Description
Mapped value	8	1C0H-2BFH	This is the base table for all four horizontal interpolation lookup tables. Each table is then generated by multiply this value with corresponding scale factor and added with corresponding offset factor.
Check Sum	8	2C0H	Sum of all part 10 entry (only keep lower 8 bits)

Part 11: Vertical Interpolation Lookup Table

Symbol	Width (bits)	Address	Description
Mapped value	8	2E0H-3DFH	This is the base table for vertical interpolation lookup table. The vertical interpolation table is then generated by multiply this value with vertical scale factor and added with vertical offset factor.
Check Sum	8	3E0H	Sum of all part 10 entry (only keep lower 8 bits)

3.6. CPU interface

The SD1200 supports 2-wire I^2C serial interface to external CPU. The interface allows external CPU to access and modify control registers inside the SD1200. The I^2C serial interface is similar to the EEPROM interface, and the CPU is the host that drives the SCL all the time as the clock and for "start" and "stop" bits. The SCL frequency can be as high as 5MHz. The SDA is a bi-directional data wire. This interface supports random and sequential write operations for CPU to modify one or multiple control registers, and random and sequential read operations for CPU to read all or part of the control registers.

The lower 4 bits of device ID for SD1200 are fixed at "1010". The upper 3 bits are programmable through MODE_IN3 (pin 19), MODE_IN2 (pin 18) and MODE_IN1 (pin 15). This avoids any conflict with other I2C devices on the same bus.

The following table briefly describes the SD1200 control registers. External CPU can read these register to know the state of the SD1200 as well as the result of input mode detection and phase calibration. External CPU can modify these control registers to disable several SD1200 features and force the SD1200 into a particular state. When the CPU modifies the control registers, the new data will be first stored in a set of shadow registers, and then are copied into the actual control registers when the "CPU Control Enable" bit is set. When the "CPU Control Enable" bit is set, the external CPU will retain control and the SD1200 will not perform the auto mode detection and auto calibration.

The external CPU is able to adjust the size of the output image and move the output image up and down by simply changing the porch size and pixel and line numbers of the input signal. These adjustments can be tied to the external user control button on the monitor.

A set of four control registers are used to generate output signal when there is no input signal available to the SD1200, or the input signal is beyond the acceptable ranges. This operation mode is called standalone mode, which is very important for the end users when they accidentally select an input mode beyond the acceptable range of the SD1200, or when the input cable connection becomes loose for any reason. System

manufacturers can display appropriate OSD warning messages on the LCD panel to notify the users about the problem.

Table 3: SD1200 Control Registers

Symbol	Width	Mode	Address	Description
VBP Source	11	RW	0H-1H	Input VSYNC back porch (not include pulse width)
VSIZE Source	11	RW	2H-3H	Input image lines per frame
VTOTAL Source	11	RW	4H-5H	Input total number of lines including porches
HBP Source	11	RW	6H-7H	Input HSYNC back porch (not include pulse width)
HSIZE Source	11	RW	8H-9H	Input image pixels per line
HTOTAL Source	11	RW	AH-BH	Input total number of pixels per line including porches
Mode Source	3	RW	CH[2:0]	Input video format 0: 640x350 1: 640x400 2: 720x400 3: 640x480 4: 800x600 5: 1024x768 6: 1280x1024 7: invalid
Clock Phase Source	9	RW	DH-EH	Input sampling clock phase
VPW standalone	10	RW	FH-10H	For standalone mode, the pulse width of VSYNC
VTOTAL standalone	10	RW	11H-12H	For standalone mode, total number of line per frame
HPW standalone	10	RW	13H-14H	For standalone mode, HSYNC active time in us
HTOTAL standalone	10	RW	15H-16H	For standalone mode, HSYNC cycle time in us
Disable auto calibration for mode 640x350	1	RW	17H[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode 640x350	15	RW	17H[6:0]-18H	The number of frames need to be skipped before starting auto calibration for this mode
Disable auto calibration for mode 640x400	1	RW	19H[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode 640x400	15	RW	19H[6:0]-1AH	The number of frames need to be skipped before starting auto calibration for this mode
Disable auto calibration for mode 720x400	1	RW	1BH[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode 720x400	15	RW	1BH[6:0]-1CH	The number of frames need to be skipped before starting auto calibration for this mode
Disable auto calibration for mode 640x480	1	RW	1DH[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode 640x480	15	RW	1DH[6:0]-1EH	The number of frames need to be skipped before starting auto calibration for this mode

Disable auto calibration for mode 800x600	1	RW	1FH[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode 800x600	15	RW	1FH[6:0]-20H	The number of frames need to be skipped before starting auto calibration for this mode
Disable auto calibration for mode 1024x768	1	RW	21H[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode 1024x768	15	RW	21H[6:0]-22H	The number of frames need to be skipped before starting auto calibration for this mode
Disable auto calibration for mode 1280x1024	1	RW	23H[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode 1280x1024	15	RW	23H[6:0]-24H	The number of frames need to be skipped before starting auto calibration for this mode
Disable auto calibration for mode INVALID	1	RW	25H[7]	Disable auto calibration for this mode 1: disable 0: enable
Delay auto calibration for mode INVALID	15	RW	25[6:0]-26H	The number of frames need to be skipped before starting auto calibration for this mode
Bypass Sync Polarity	1	RW	27H[7]	Bypass Input SYNC polarity detection (default 0) 1: bypass input SYNC polarity detection 0: detect input SYNC polarity and make them negative polarity
Enable SYNC Check	7	RW	27H[6:0]	Enable SYNC polarity check during input mode detection (default all 0). 1: enable SYNC polarity based mode detection 0: disable SYNC polarity based mode detection bit 0: 640x350 bit 1: 640x400 bit 2: 720x400 bit 3: 640x480 bit 4: 800x600 bit 5: 1024x768 bit 6: 1280x1024
Dithering Enable	1	RW	28H[7]	Enable dithering for 6 bit panel (default 0) 1: enable dithering 0: disable dithering
Frame Modulation Enable	1	RW	28H[6]	Enable frame modulation for 6 bit panel (default 0) 1: enable frame modulation 0: disable frame modulation
Horizontal Interpolation Enable	1	RW	28H[5]	Enable horizontal interpolation (default 0) 1: enable horizontal interpolation 0: disable horizontal interpolation
Vertical Interpolation Enable	1	RW	28H[4]	Enable vertical interpolation (default 0) 1: enable vertical interpolation 0: disable vertical interpolation
Horizontal Rounding Enable	1	RW	28H[3]	Enable horizontal rounding (default 0) 1: enable horizontal rounding 0: disable horizontal rounding
Vertical Rounding Enable	1	RW	28H[2]	Enable vertical rounding (default 0) 1: enable vertical rounding 0: disable vertical rounding
Horizontal Table	1	RW	28H[1]	Enable horizontal Table Lookup (default 0)

Lookup Enable				1: enable horizontal Table Lookup 0: disable horizontal Table Lookup
Vertical Table Lookup Enable	1	RW	28H[0]	Enable vertical Table Lookup (default 0) 1: enable vertical Table Lookup 0: disable vertical Table Lookup
HSYNC Threshold Enable	1	RW	29H[4]	Enable detection of short lines (IBM panel only, default 0) 1: Enable such detection 0: disable such detection
OSD Intensity	1	RW	29H[3]	OSD intensity selection 0: half intensity 1: full intensity
Load ALL EEPROM	1	RW	29H[2]	Should be kept low most time. A high pulse will force SD1200 to reload all EEPROM entries
Load Mode Dependent EEPROM	1	RW	29H[1]	Should be kept low most time. A high pulse will force SD1200 to reload mode dependent EEPROM entries
CPU control enable	1	RW	29H[0]	External CPU control enable 0: disable external CPU control. SD1200 can write control registers, but CPU only read control registers. 1: enable external CPU control. CPU can read/write control registers. SD1200 cannot write control registers
Status 0	8	R	2AH	Read only internal status registers 1: indicate error status 0: indicate normal status Bit 0: EEPROM vertical lookup table loading Bit 1: EERPOM horizontal lookup table loading Bit 2: EEPROM mode dependent entries loading Bit 3: EEPROM calibration entries loading Bit 4: input has too few lines Bit 5: no input video Bit 6: input data clock is too fast Bit 7: refresh rate exceed LCD panel specification
Status 1	4	R	2BH[3:0]	Internal auto calibration state

4. ELECTRICAL SPECIFICATION

This section presents the electrical specifications of the SD1200.

4.1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VCC	Power Supply	-0.3 to 6.0	V
VIN	Input Voltage	-0.3 to VCC + 0.3	V
VOUT	Output Voltage	-0.3 to VCC +0.3	V
TSTG	Storage Temperature	-55 to 150	°C

4.2. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VCC	Commercial Power Supply	4.75	5.0	5.25	V
VCC	Industrial Power Supply	4.5	5.0	5.5	V
VIN	Input Voltage	0	-	VCC	V
TJ	Commercial Junction Operating Temperature	0	25	115	°C
TJ	Industrial Junction Operating Temperature	-40	25	125	°C

4.3. General DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
IIL	Input Leakage Current	no pull – up or pull - down	-1		1	µA
IOZ	TRI-state Leakage Current		-10		10	µA
CIN	Input Capacitance			3		ρF
COUT	Output capacitance			3		ρF
CBID3	Bi-directional buffer capacitance			3		ρF

Note: *The capacitance above does not include PAD capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance, which is about 0.5 r F and the package capacitance*

4.4. DC Electrical Characteristics for 3.3 V Operation

(Under Recommended Operation Conditions and V_{CC} = 3.0 ~ 3.6V, T_J = 0°C to +115°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIL	Input low voltage	CMOS			0.3*VCC	V
VIH	Input high Voltage	CMOS	0.7*VCC			V
VT-	Schmitt trigger negative going threshold voltage	COMS		1.22		V
VT+	Schmitt trigger positive going threshold voltage	COMS		2.08		V
VOL	Output low voltage	IOH=2,4,8,12, 16,24 mA			0.4	V
VOH	Output high voltage	IOH=2,4,8,12, 16,24 mA	2.4			V
RI	Input pull-up /down resistance	VIL=0V or VIH=VCC		75		KΩ

4.5. DC Electrical Characteristics for 5V Operation

(Under Recommended Operation Conditions and V_{CC}=4.75~5.25,T_J=0°C to +115°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VIL	Input low voltage	COMS			0.3*VCC	V
VIH	Input high voltage	COMS	0.7*VCC			V
VIL	Input low voltage	TTL			0.8	V
VIH	Input high voltage	TTL	2.0			V
VT-	Schmitt trigger negative going threshold voltage	CMOS		1.84		V
VT+	Schmitt trigger Positive going threshold voltage	COMS		3.22		V
VT-	Schmitt trigger negative going threshold voltage	TTL		1.10		V
VT+	Schmitt trigger positive going threshold voltage	TTL		1.87		V
VOL	Output low voltage	IOL=2,4,8,16,24mA			0.4	V
VOH	Output high voltage	IOH=2,4,8,16,24 mA	3.5			V
RI	Input pull-up / down resistance	VIL=0V or VIH=VCC		50		KΩ

5. PACKAGE DIMENSIONS

6. ORDER INFORMATION

Order Code	Temperature	Package	Speed
SD1200	Commercial 0°C ~ 70°C	160-pin PQFP 14 x 20 (mm)	60MHz

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