DAC5675A-SP Radiation-Tolerant, 14-Bit, 400-MSPS Digital-to-Analog Converter

1 Features

- QMLV (QML Class V) MIL-PRF-38535 Qualified, SMD 5962-07204
  – 5962-0720401VXC – Qualified over the Military Temperature Range (–55°C to 125°C)
  – 5962-0720402VXC – Qualified over Reduced Temperature Range (–55°C to 115°C) for Improved Dynamic Performance
- High-Performance 52-Pin Ceramic Quad Flat Pack (HFG)
- 400-MSPS Update Rate
- LVDS-Compatible Input Interface
- Spurious-Free Dynamic Range (SFDR) to Nyquist
  – 69 dBc at 70 MHz IF, 400 MSPS
- W-CDMA Adjacent Channel Power Ratio (ACPR)
  – 73 dBc at 30.72 MHz IF, 122.88 MSPS
  – 71 dBc at 61.44 MHz IF, 245.76 MSPS
- Differential Scalable Current Outputs: 2 to 20 mA
- On-Chip 1.2-V Reference
- Single 3.3-V Supply Operation
- Power Dissipation: 660 mW at f_{CLK} = 400 MSPS, f_{OUT} = 20 MHz

2 Applications

- Radiation Hardened Digital to Analog (DAC) Applications
- Space Satellite RF Data Transmission
- Cellular Base Transceiver Station Transmit Channel:
  – CDMA: WCDMA, CDMA2000, IS-95
  – TDMA: GSM, IS-136, EDGE/GPRS
  – Supports Single-Carrier and Multicarrier Applications
- Engineering Evaluation (/EM) Samples are Available [(1)]

(1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (for example, no burn-in) and are tested to temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance on full MIL specified temperature range of –55°C to 125°C or operating life.

3 Description

The DAC5675A-SP is a radiation-tolerant, 14-bit resolution high-speed digital-to-analog converter (DAC) primarily suited for space satellite applications. The DAC5675A-SP is designed for high-speed digital data transmission in wired and wireless communication systems, high-frequency direct digital synthesis (DDS), and waveform reconstruction in test and measurement applications. The DAC5675A-SP has excellent SFDR at high intermediate frequencies, which makes it well suited for multicarrier transmission in TDMA and CDMA based cellular base transceiver stations (BTSs).

The DAC5675A-SP operates from a single supply voltage of 3.3 V. Power dissipation is 660 mW at f_{CLK} = 400 MSPS, f_{OUT} = 70 MHz. The DAC5675A-SP provides a nominal full-scale differential current output of 20 mA, supporting both single-ended and differential applications. The output current can be directly fed to the load with no additional external output buffer required. The output is referred to the analog supply voltage AV_{DD}.

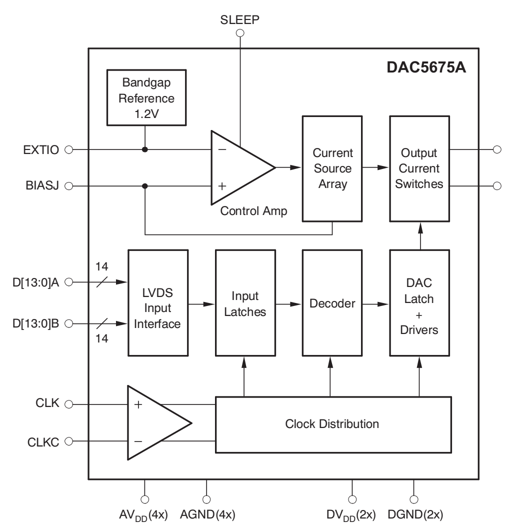
The DAC5675A-SP includes a low-voltage differential signaling (LVDS) interface for high-speed digital data input. LVDS features a low differential voltage swing with a low constant power consumption across frequency, allowing for high-speed data transmission with low noise levels (low electromagnetic interference (EMI)).

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC5675A-SP	HFG (52 CQFP)	19.05 mm × 19.05 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (January 2014) to Revision G **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated supply voltage absolute maximum ratings for AV_{DD} to DV_{DD} 5

Changes from Revision E (April 2013) to Revision F **Page**

- Added /EM bullet to *Features* 1
- Deleted Ordering Information table 3

5 Description (continued)

LVDS is typically implemented in low-voltage digital CMOS processes, making it the ideal technology for high-speed interfacing between the DAC5675A-SP and high-speed low-voltage CMOS ASICs or FPGAs.

The DAC5675A-SP current-source-array architecture supports update rates of up to 400 MSPS. On-chip edge-triggered input latches provide for minimum setup and hold times, thereby relaxing interface timing.

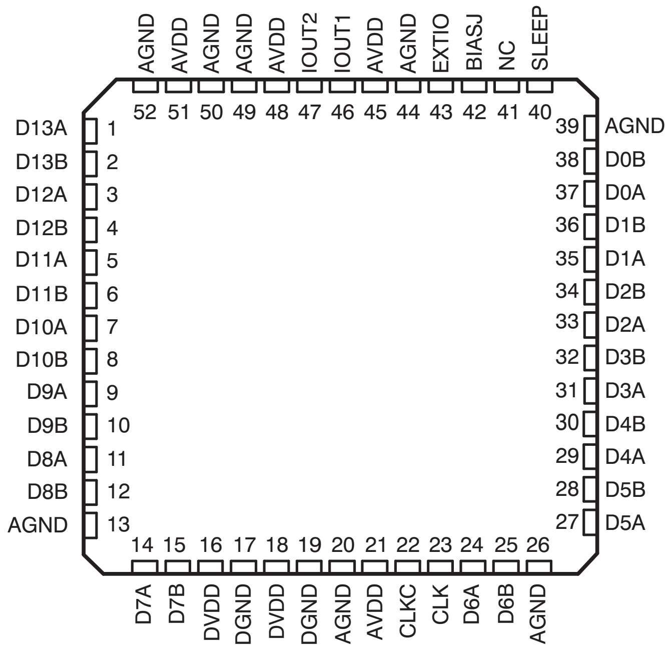
The DAC5675A-SP is specifically designed for a differential transformer-coupled output with a 50-Ω doubly-terminated load. With the 20-mA full-scale output current, both a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (–2 dBm) is supported. The last configuration is preferred for optimum performance at high output frequencies and update rates. The outputs are terminated to AVDD and have voltage compliance ranges from AV_{DD} – 1 to AV_{DD} + 0.3 V.

An accurate on-chip 1.2-V temperature-compensated bandgap reference and control amplifier allows the user to adjust this output current from 20 to 2 mA. This provides 20-dB gain range control capabilities. Alternatively, an external reference voltage may be applied. The DAC5675A-SP features a SLEEP mode, which reduces the standby power to approximately 18 mW.

The DAC5675A-SP is available in a 52-pin ceramic nonconductive tie-bar package (HFG). The device is specified for operation over the military temperature range of –55°C to 125°C and W temperature range of –55°C to 115°C.

6 Pin Configuration and Functions

HFG Package
52-Pin CQFP
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	13, 20, 26, 39, 44, 49, 50, 52	I	Analog negative supply voltage (ground). Pin 13 is internally connected to the heat slug and lid (lid is also grounded internally).
AV_{DD}	21, 45, 48, 51	I	Analog positive supply voltage
BIASJ	42	O	Full-scale output current bias
CLK	23	I	External clock input
CLKC	22	I	Complementary external clock
D[13:0]A	1, 3, 5, 7, 9, 11, 14, 24, 27, 29, 31, 33, 35, 37	I	LVDS positive input, data bits 13–0. D13A is the most significant data bit (MSB). D0A is the least significant data bit (LSB).
D[13:0]B	2, 4, 6, 8, 10, 12, 15, 25, 28, 30, 32, 34, 36, 38	I	LVDS negative input, data bits 13–0. D13B is the most significant data bit (MSB). D0B is the least significant data bit (LSB).
DGND	17, 19	I	Digital negative supply voltage (ground)
DV_{DD}	16, 18	I	Digital positive supply voltage
EXTIO	43	I/O	Internal reference output or external reference input. Requires a 0.1-μF decoupling capacitor to AGND when used as reference output.
IOUT1	46	O	DAC current output. Full-scale when all input bits are set '0'. Connect the reference side of the DAC load resistors to AV_{DD}.
IOUT2	47	O	DAC complementary current output. Full-scale when all input bits are '1'. Connect the reference side of the DAC load resistors to AV_{DD}.
NC	41		Not connected in chip. Can be high or low.
SLEEP	40	I	Asynchronous hardware power-down input. Active high. Internal pulldown.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AV_{DD} (2)	–0.3	3.6	V
	DV_{DD} (3)	–0.3	3.6	
	AV_{DD} to DV_{DD}	–3.6	3.6	
Voltage between AGND and DGND		–0.3	0.5	V
CLK, CLKC(2)		–0.3	AV_{DD} + 0.3	V
Digital input D[13:0]A, D[13:0]B(3), SLEEP, DLLOFF		–0.3	DV_{DD} + 0.3	V
IOUT1, IOUT2(2)		–1	AV_{DD} + 0.3	V
EXTIO, BIASJ(2)		–1	AV_{DD} + 0.3	V
Peak input current (any input)			20	mA
Peak total input current (all inputs)			–30	mA
Lead temperature 1.6 mm (1/16 inch) from the case for 10 s			260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND
(3) Measured with respect to DGND

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
A_{VDD}	Analog supply voltage		3.15	3.3	3.6	V
D_{VDD}	Digital supply voltage		3.15	3.3	3.6	V
T_J	Operating junction temperature range	5962-0720401	–55		125	°C
		5962-0720402	–55		115	

7.4 Thermal Information

THERMAL METRIC(1)		DAC5675A-SP HFG (CQFP) 52 PINS	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance(2)	21.813	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(3)	0.849	
$R_{\theta JB}$	Junction-to-board thermal resistance	N/A	
ψ_{JT}	Junction-to-top characterization parameter	N/A	
ψ_{JB}	Junction-to-board characterization parameter	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Board mounted, per JESD 51-5 methodology
(3) MIL-STD-883 test method 1012

7.5 DC Electrical Characteristics (Unchanged After 100 kRad)

over operating junction temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	5962-0720401			5962-0720402			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			14			14			bit
DC ACCURACY(1)									
INL	Integral nonlinearity	T_{MIN} to T_{MAX}	–4	±1.5	4.6	–4	±1.5	4.6	LSB
DNL	Differential nonlinearity	$T_{25°C}$ to T_{MAX}	–2	±0.6	2.2	–2	±0.6	2.2	LSB
		T_{MIN}	–2	±0.6	2.5	–2	±0.6	2.5	
Monotonicity			Monotonic 12b Level			Monotonic 12b Level			
ANALOG OUTPUT									
$I_{O(FS)}$	Full-scale output current		2		20	2		20	mA
	Output compliance range	AV_{DD} = 3.15 to 3.45 V, $I_{O(FS)}$ = 20 mA	AV_{DD} – 1		AV_{DD} + 0.3	AV_{DD} – 1		AV_{DD} + 0.3	V
	Offset error			0.01			0.01		%FSR
	Gain error	Without internal reference	–10	5	10	–10	5	10	%FSR
		With internal reference	–10	2.5	10	–10	2.5	10	
	Output resistance			300			300		kΩ
	Output capacitance			5			5		pF
REFERENCE OUTPUT									
$V_{(EXTIO)}$	Reference voltage		1.17	1.23	1.30	1.17	1.23	1.30	V
	Reference output current(2)			100			100		nA
REFERENCE INPUT									
$V_{(EXTIO)}$	Input reference voltage		0.6	1.2	1.25	0.6	1.2	1.25	V
	Input resistance			1			1		MΩ
	Small-signal bandwidth			1.4			1.4		MHz
	Input capacitance			100			100		pF
TEMPERATURE COEFFICIENTS									
	Offset drift			12			12		ppm of FSR/°C
$\Delta V_{(EXTIO)}$	Reference voltage drift			±50			±50		ppm/°C
POWER SUPPLY									
AV_{DD}	Analog supply voltage		3.15	3.3	3.6	3.15	3.3	3.6	V
DV_{DD}	Digital supply voltage		3.15	3.3	3.6	3.15	3.3	3.6	V
$I_{(AVDD)}$	Analog supply current(3)			115	148		115	138	mA

(1) Measured differential at I_{OUT1} and I_{OUT2}: 25 Ω to AV_{DD}
(2) Use an external buffer amplifier with high impedance input to drive any external load.
(3) Measured at f_{CLK} = 400 MSPS and f_{OUT} = 70 MHz

DC Electrical Characteristics (Unchanged After 100 kRad) (continued)

over operating junction temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	5962-0720401			5962-0720402			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{(DVDD)}$	Digital supply current(3)			85	130		85	120	mA
P_D	Power dissipation	Sleep mode		18			18		mW
		AV_{DD} = 3.3 V, DV_{DD} = 3.3 V		660	900		660	850	
APSRR	Analog and digital power-supply rejection ratio	AV_{DD} = 3.15 to 3.45 V	–0.9	±0.1	0.9	–0.9	±0.1	0.9	%FSR/V
DPSRR			–0.9	±0.1	0.9	–0.9	±0.1	0.9	

7.6 AC Electrical Characteristics (Unchanged After 100 kRad)

over operating junction temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA, differential transformer-coupled output, 50-Ω doubly-terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS		5962-0720401			5962-0720402			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUT										
f_{CLK}	Output update rate					400			400	MSPS
$t_{s(DAC)}$	Output setting time to 0.1%	Transition: code x2000 to $x23_{FF}$			12			12		ns
t_{PD}	Output propagation delay				1			1		ns
$t_{r(IOUT)}$	Output rise time, 10% to 90%				300			300		ps
$t_{f(IOUT)}$	Output fall time, 90% to 10%				300			300		ps
	Output noise	$IOUT_{FS}$ = 20 mA			55			55		pA/√Hz
		$IOUT_{FS}$ = 2 mA			30			30		
AC LINEARITY										
THD	Total harmonic distortion	f_{CLK} = 100 MSPS, f_{OUT} = 19.9 MHz			70			70		dBc
		f_{CLK} = 160 MSPS, f_{OUT} = 41 MHz			72			72		
		f_{CLK} = 200 MSPS, f_{OUT} = 70 MHz			68			68		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.0 MHz	60	68		62	68		
			f_{OUT} = 20.0 MHz, for T_{MIN}	57			57			
			f_{OUT} = 70 MHz		67			67		
			f_{OUT} = 140 MHz		55			55		
SFDR	Spurious-free dynamic range to Nyquist	f_{CLK} = 100 MSPS, f_{OUT} = 19.9 MHz			70			70		dBc
		f_{CLK} = 160 MSPS, f_{OUT} = 41 MHz			73			73		
		f_{CLK} = 200 MSPS, f_{OUT} = 70 MHz			70			70		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.0 MHz	62	68		63	68		
			f_{OUT} = 20.0 MHz, for T_{MIN}	61			61			
			f_{OUT} = 70 MHz		69			69		
			f_{OUT} = 140 MHz		56			56		
SFDR	Spurious-free dynamic range within a window, 5 MHz span	f_{CLK} = 100 MSPS, f_{OUT} = 19.9 MHz			82			82		dBc
		f_{CLK} = 160 MSPS, f_{OUT} = 41 MHz			77			77		
		f_{CLK} = 200 MSPS, f_{OUT} = 70 MHz			82			82		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.0 MHz		82			82		
			f_{OUT} = 70 MHz		82			82		
			f_{OUT} = 140 MHz		75			75		
SNR	Signal-to-noise ratio	f_{CLK} = 400 MSPS, f_{OUT} = 20.0 MHz		60	67		60	67		dBc
ACPR	Adjacent channel power ratio WCDMA with 3.84 MHz BW, 5 MHz channel spacing	f_{CLK} = 122.88 MSPS, IF = 30.72 MHz, see Figure 9			73			73		dB
		f_{CLK} = 245.76 MSPS, IF = 61.44 MHz,			71			71		
		f_{CLK} = 399.36 MSPS, IF = 153.36 MHz, see Figure 11			65			65		

AC Electrical Characteristics (Unchanged After 100 kRad) (continued)

over operating junction temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA, differential transformer-coupled output, 50-Ω doubly-terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	5962-0720401			5962-0720402			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
IMD	Two-tone intermodulation to Nyquist (each tone at –6 dBfs)	f_{CLK} = 400 MSPS, f_{OUT1} = 70 MHz, f_{OUT2} = 71 MHz		73			73		dBc
		f_{CLK} = 400 MSPS, f_{OUT1} = 140 MHz, f_{OUT2} = 141 MHz		62			62		
	Four-tone intermodulation, 15-MHz span, missing center tone (each tone at –16 dBfs)	f_{CLK} = 156 MSPS, f_{OUT} = 15.6, 15.8, 16.2, 16.4 MHz		82			82		
		f_{CLK} = 400 MSPS, f_{OUT} = 68.1, 69.3, 71.2, 72 MHz		74			74		

7.7 Digital Specifications (Unchanged After 100 kRad)

over operating junction temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	5962-0720401			5962-0720402			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
LVDS INTERFACE: NODES D[13:0]A, D[13:0]B									
V_{ITH+}	Positive-going differential input voltage threshold			100			100		mV
$V_{ITH–}$	Negative-going differential input voltage threshold			–100			–100		mV
Z_T	Internal termination impedance		90	110	132	90	110	132	Ω
C_I	Input capacitance			2			2		pF
CMOS INTERFACE (SLEEP)									
V_{IH}	High-level input voltage		2	3.3		2	3.3		V
V_{IL}	Low-level input voltage			0	0.8		0	0.8	V
I_{IH}	High-level input current		10		100	10		100	μA
I_{IL}	Low-level input current		–10		10	–10		10	μA
	Input capacitance			2			2		pF
CLOCK INTERFACE (CLK, CLKC)									
|CLK-CLKC|	Clock differential input voltage		0.4		0.8	0.4		0.8	V_{PP}
$t_{w(H)}$	Clock pulse width high			1.25			1.25		ns
$t_{w(L)}$	Clock pulse width low			1.25			1.25		ns
	Clock duty cycle		40%		60%	40%		60%	
V_{CM}	Common-mode voltage range		1.6	2	2.4	1.6	2	2.4	V
	Input resistance	Node CLK, CLKC		670			670		Ω
	Input capacitance	Node CLK, CLKC		2			2		pF
	Input resistance	Differential		1.3			1.3		kΩ
	Input capacitance	Differential		1			1		pF
TIMING									
t_{SU}	Input setup time		1.5			1.5			ns
t_H	Input hold time		0.0			0.0			ns
t_{DD}	Digital delay time (DAC latency)			3			3		clk

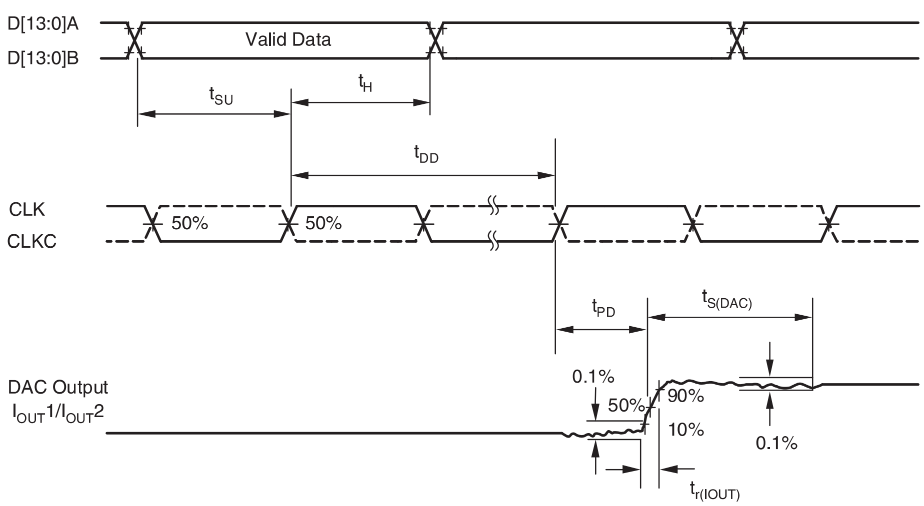


Figure 1. Timing Diagram

7.8 Electrical Characteristics(1)

over operating junction temperature range, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	LOGICAL BIT BINARY EQUIVALENT	COMMENT
V_A (V)	V_B (V)	$V_{A,B}$ (mV)	V_{COM} (V)		
1.25	1.15	100	1.2	1	Operation with minimum differential voltage (±100 mV) applied to the complementary inputs versus common-mode range
1.15	1.25	–100	1.2	0	
2.4	2.3	100	2.35	1	
2.3	2.4	–100	2.35	0	
0.1	0	100	0.05	1	
0	0.1	–100	0.05	0	
1.5	0.9	600	1.2	1	Operation with maximum differential voltage (±600 mV) applied to the complementary inputs versus common-mode range
0.9	1.5	–600	1.2	0	
2.4	1.8	600	2.1	1	
1.8	2.4	–600	2.1	0	
0.6	0	600	0.3	1	
0	0.6	–600	0.3	0	

(1) Specifications subject to change.

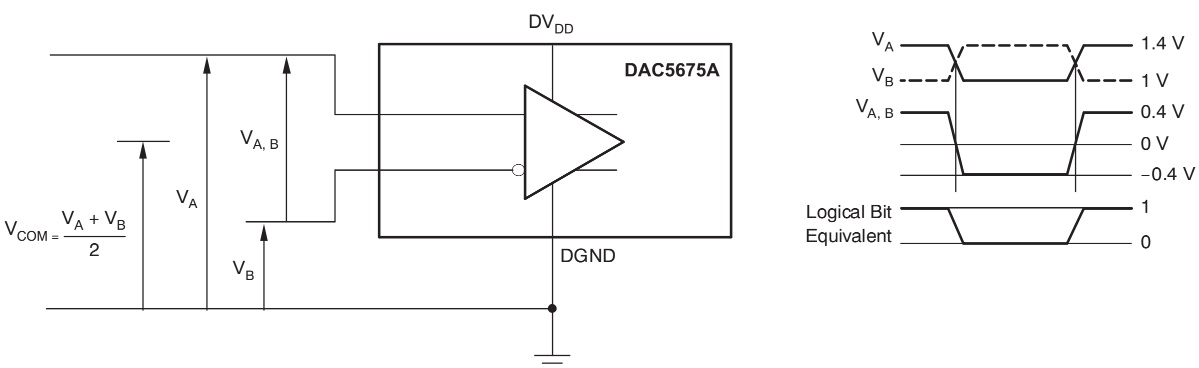


Figure 2. LVDS Timing Test Circuit and Input Test Levels

7.9 Typical Characteristics

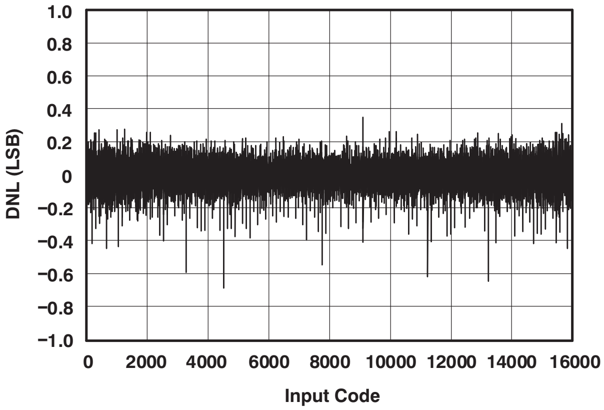


Figure 3. Differential Nonlinearity (DNL) vs Input Code

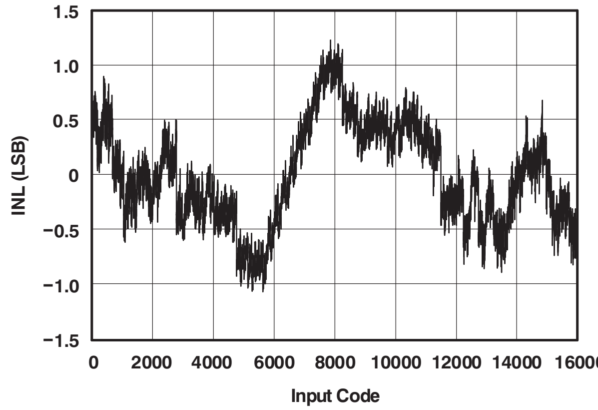


Figure 4. Integral Nonlinearity (INL) vs Input Code

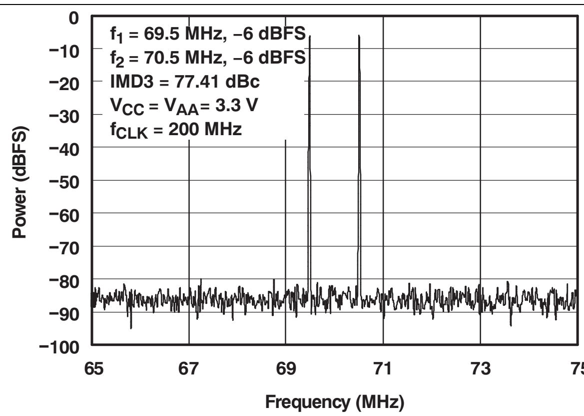


Figure 5. Two-Tone IMD (Power) vs Frequency

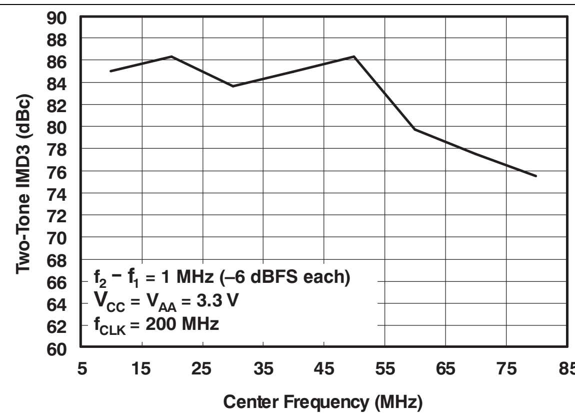


Figure 6. Two-Tone IMD3 vs Frequency

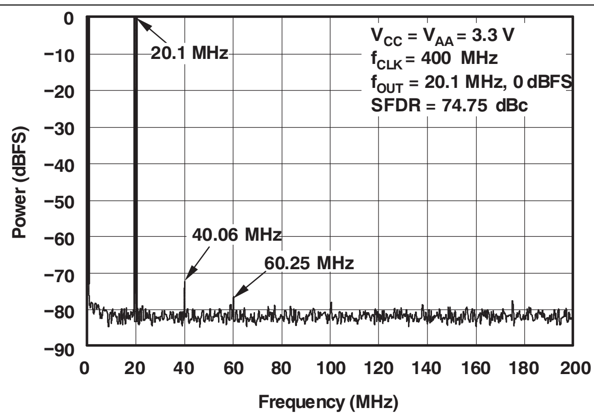


Figure 7. Single-Tone Spectrum Power vs Frequency

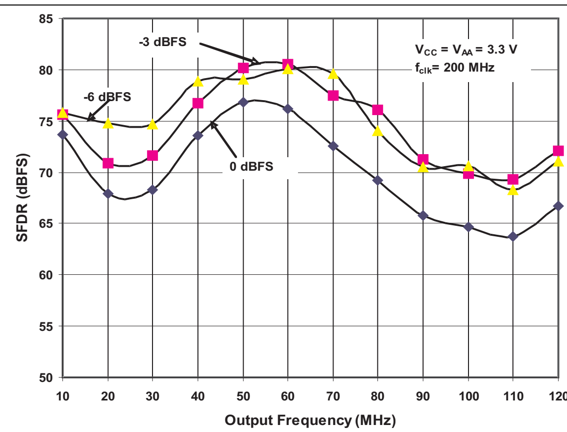


Figure 8. Spurious-Free Dynamic Range vs Frequency

Typical Characteristics (continued)

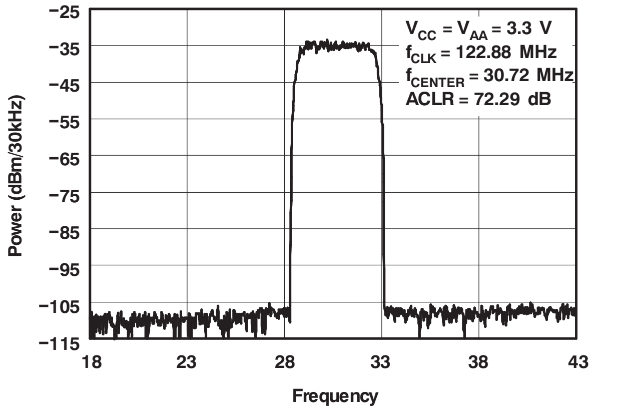


Figure 9. W-CDMA TM1 Single Carrier Power vs Frequency

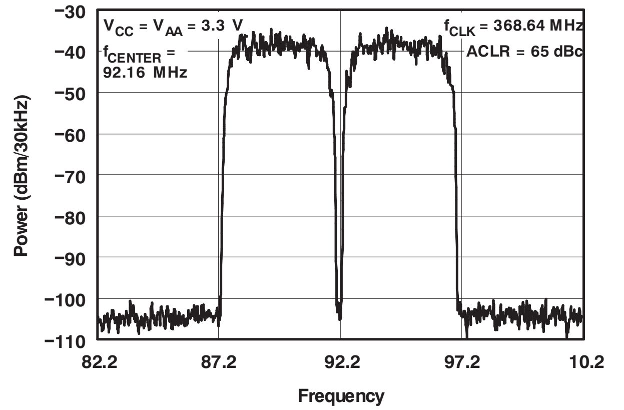


Figure 10. W-CDMA TM1 Dual Carrier Power vs Frequency

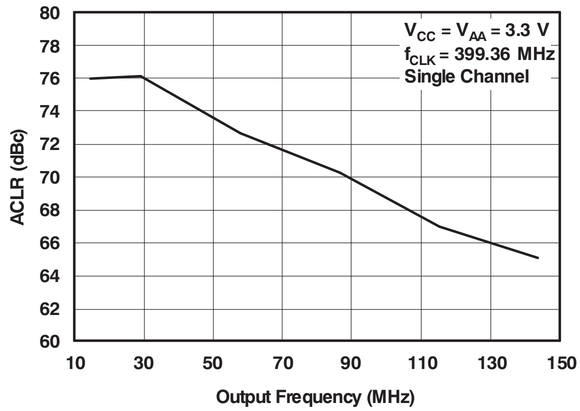


Figure 11. W-CDMA TM1 Single Carrier ACLR vs Output Frequency

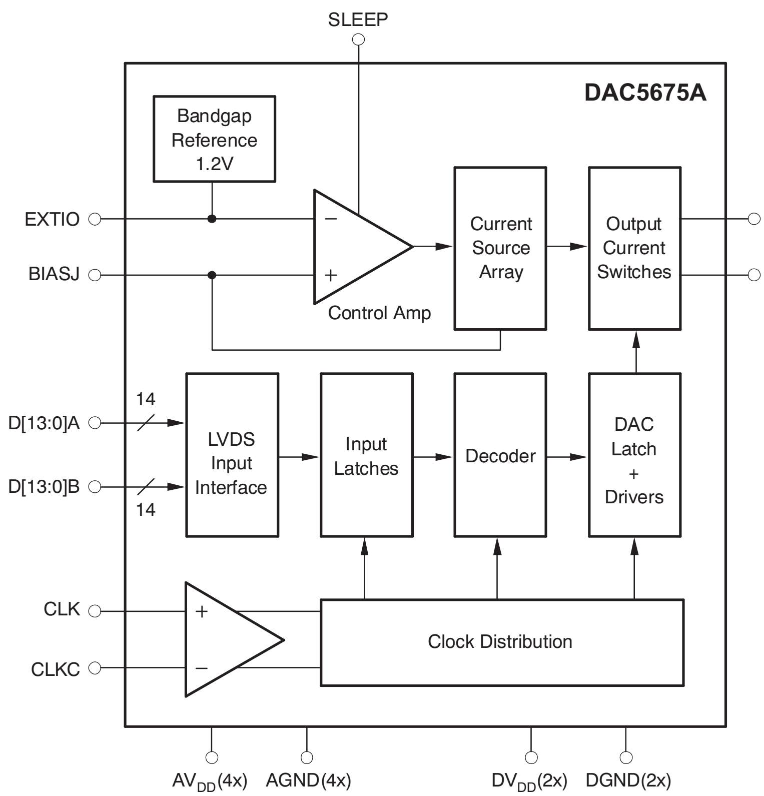
8 Detailed Description

8.1 Overview

Functional Block Diagram shows a simplified block diagram of the current steering DAC5675A-SP. The DAC5675A-SP consists of a segmented array of NPN-transistor current sources, capable of delivering a full-scale output current up to 20 mA. Differential current switches direct the current of each current source to either one of the complementary output nodes IOUT1 or IOUT2. The complementary current output enables differential operation, canceling out common-mode noise sources (digital feedthrough, on-chip, and PCB noise), dc offsets, and even-order distortion components, and doubling signal output power.

The full-scale output current is set using an external resistor (R_{BIAS}) with an on-chip bandgap voltage reference source (1.2 V) and control amplifier. The current (I_{BIAS}) through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 16 × I_{BIAS}. The full-scale current is adjustable from 20 to 2 mA by using the appropriate bias resistor value.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital Inputs

The DAC5675A-SP uses a low-voltage differential signaling (LVDS) bus input interface. The LVDS features a low differential voltage swing with low constant power consumption (4 mA per complementary data input) across frequency. The differential characteristic of LVDS allows for high-speed data transmission with low electromagnetic interference (EMI) levels. Figure 12 shows the equivalent complementary digital input interface for the DAC5675A-SP, valid for pins D[13:0]A and D[13:0]B. Note that the LVDS interface features internal 110-Ω resistors for proper termination. Figure 2 shows the LVDS input timing measurement circuit and waveforms. A common-mode level of 1.2 V and a differential input swing of 0.8 V_{PP} is applied to the inputs.

Figure 13 shows a schematic of the equivalent CMOS/TTL-compatible digital inputs of the DAC5675A-SP, valid for the SLEEP pin.

Feature Description (continued)

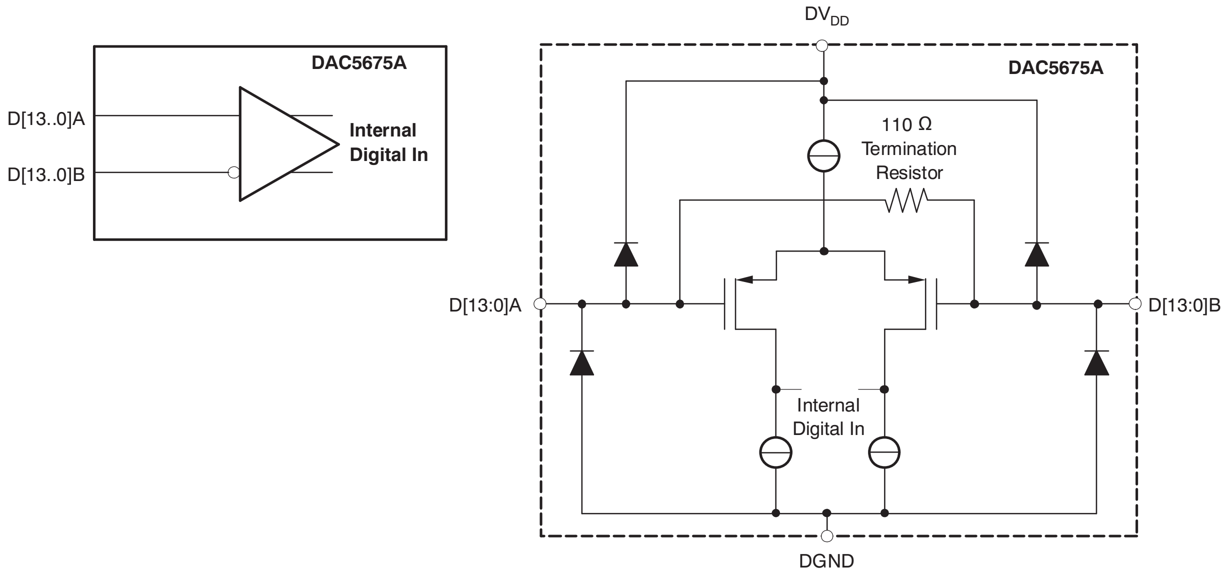


Figure 12. LVDS Digital Equivalent Input

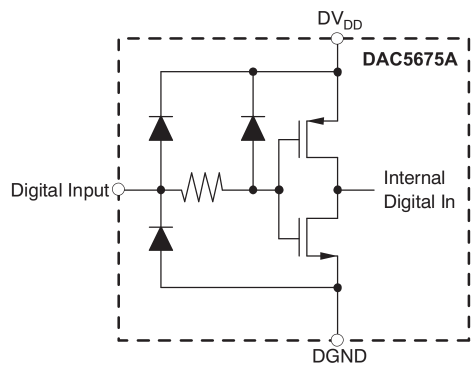


Figure 13. CMOS/TTL Digital Equivalent Input

8.3.2 Clock Input

The DAC5675A-SP features differential LVPECL-compatible clock inputs (CLK, CLKC). Figure 14 shows the equivalent schematic of the clock input buffer. The internal biasing resistors set the input common-mode voltage to approximately 2 V, while the input resistance is typically 670 Ω. A variety of clock sources can be ac-coupled to the device, including a sine-wave source (see Figure 15).

Feature Description (continued)

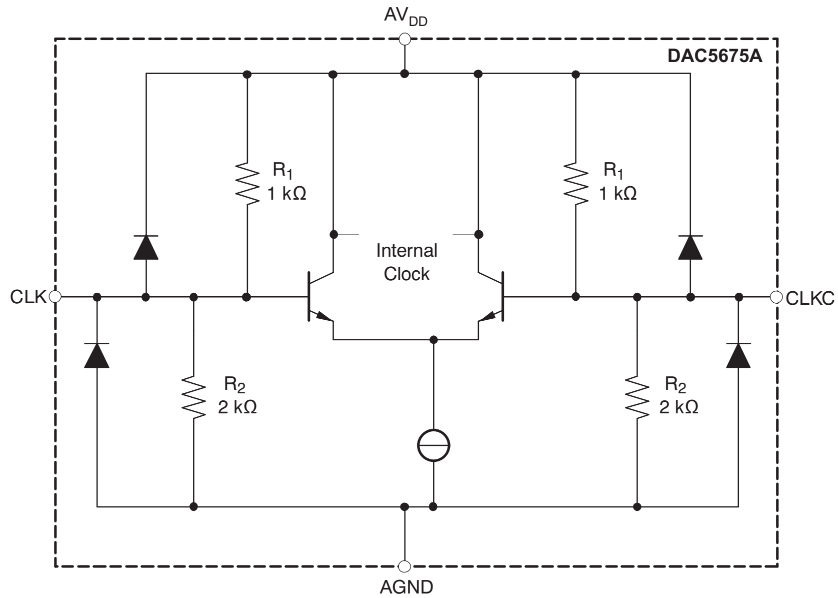


Figure 14. Clock Equivalent Input

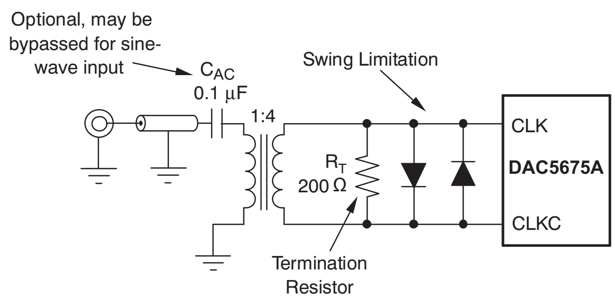


Figure 15. Driving the DAC5675A-SP With a Single-Ended Clock Source Using a Transformer

To obtain best ac performance, the DAC5675A-SP clock input should be driven with a differential LVPECL or sine-wave source as shown in Figure 16 and Figure 17. Here, the potential of V_{TT} should be set to the termination voltage required by the driver along with the proper termination resistors (R_T). The DAC5675A-SP clock input can also be driven single ended (see Figure 18).

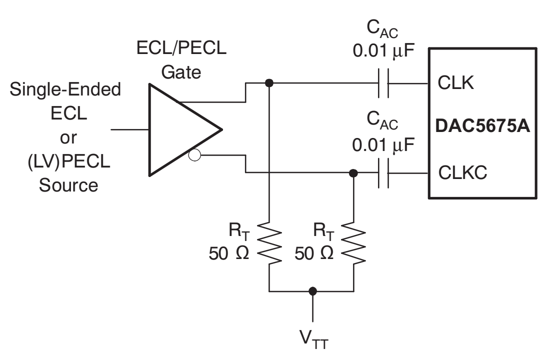


Figure 16. Driving the DAC5675A-SP With a Single-Ended ECL/PECL Clock Source

Feature Description (continued)

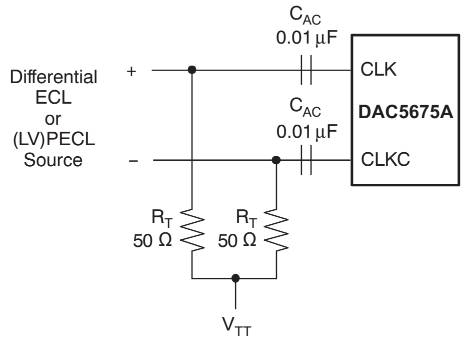


Figure 17. Driving the DAC5675A-SP With a Differential ECL/PECL Clock Source

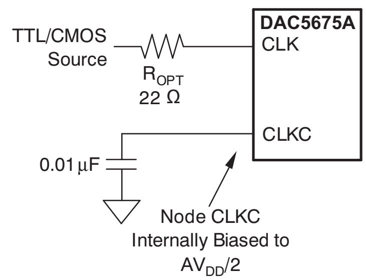


Figure 18. Driving the DAC5675A-SP With a Single-Ended TTL/CMOS Clock Source

8.3.3 Supply Inputs

The DAC5675A-SP comprises separate analog and digital supplies, AV_{DD} and DV_{DD}, respectively. These supply inputs can be set independently from 3.6 to 3.15 V.

8.3.4 DAC Transfer Function

The DAC5675A-SP has a current sink output. The current flow through IOUT1 and IOUT2 is controlled by D[13:0]A and D[13:0]B. For ease of use, D[13:0] is denoted as the logical bit equivalent of D[13:0]A and its complement D[13:0]B. The DAC5675A-SP supports straight binary coding with D13 being the MSB and D0 the LSB. Full-scale current flows through IOUT2 when all D[13:0] inputs are set high and through IOUT1 when all D[13:0] inputs are set low. The relationship between IOUT1 and IOUT2 can be expressed as Equation 1.

$$IOUT1 = IO_{(FS)} - IOUT2 \quad (1)$$

$IO_{(FS)}$ is the full-scale output current sink (2 to 20 mA). Because the output stage is a current sink, the current can only flow from AV_{DD} through the load resistors R_L into the IOUT1 and IOUT2 pins.

The output current flow in each pin driving a resistive load can be expressed as shown in Figure 19, Equation 2, and Equation 3.

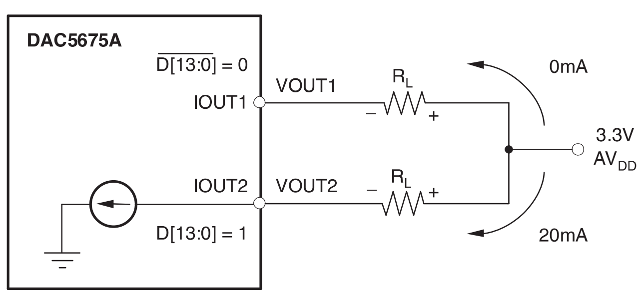


Figure 19. Relationship Between D[13:0], IOUT1 and IOUT2

Feature Description (continued)

$$IOUT1 = \frac{IO_{(FS)} \times (16383 - CODE)}{16384}$$

$$IOUT2 = \frac{IO_{(FS)} \times CODE}{16384} \quad (2)$$

where

- CODE is the decimal representation of the DAC input word (3)

This would translate into single-ended voltages at IOUT1 and IOUT2, as shown in Equation 4 and Equation 5.

$$VOUT1 = AVDD - IOUT1 \times R_L \quad (4)$$

$$VOUT2 = AVDD - IOUT2 \times R_L \quad (5)$$

Assuming that D[13:0] = 1 and the R_L is 50 Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as shown in Equation 6 through Equation 8.

$$VOUT1 = 3.3\text{ V} - 0\text{ mA} \times 50 = 3.3\text{ V} \quad (6)$$

$$VOUT2 = AVDD - 20\text{ mA} \times 50 = 2.3\text{ V} \quad (7)$$

$$VDIFF = VOUT1 - VOUT2 = 1\text{ V} \quad (8)$$

If D[13:0] = 0, then IOUT2 = 0 mA, IOUT1 = 20 mA, and the differential voltage VDIFF = –1 V.

The output currents and voltages in IOUT1 and IOUT2 are complementary. The voltage, when measured differentially, is doubled compared to measuring each output individually. Take care not to exceed the compliance voltages at the IOUT1 and IOUT2 pins to keep signal distortion low.

8.3.5 Reference Operation

The DAC5675A-SP has a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor, R_{BIAS}. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 16× this bias current. The full-scale output current $IO_{(FS)}$ is thus expressed as Equation 9.

$$I_{O(FS)} = 16 \times I_{BIAS} = \frac{16 \times V_{EXTIO}}{R_{BIAS}}$$

where

- V_{EXTIO} is the voltage at pin EXTIO (9)

The bandgap reference voltage delivers a stable voltage of 1.2 V. This reference can be overridden by applying an external voltage to terminal EXTIO. The bandgap reference can additionally be used for external reference operation. In such a case, select an external buffer amplifier with high-impedance input to limit the bandgap load current to less than 100 nA. The capacitor C_{EXT} may be omitted. Pin EXTIO serves as either an input or output node. The full-scale output current is adjustable from 20 to 2 mA by varying resistor R_{BIAS}.

8.3.6 Analog Current Outputs

Figure 20 shows a simplified schematic of the current source array output with corresponding switches. Differential NPN switches direct the current of each individual NPN current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches and is >300 kΩ in parallel with 5-pF output capacitance.

The external output resistors are referred to the positive supply, AV_{DD}.

Feature Description (continued)

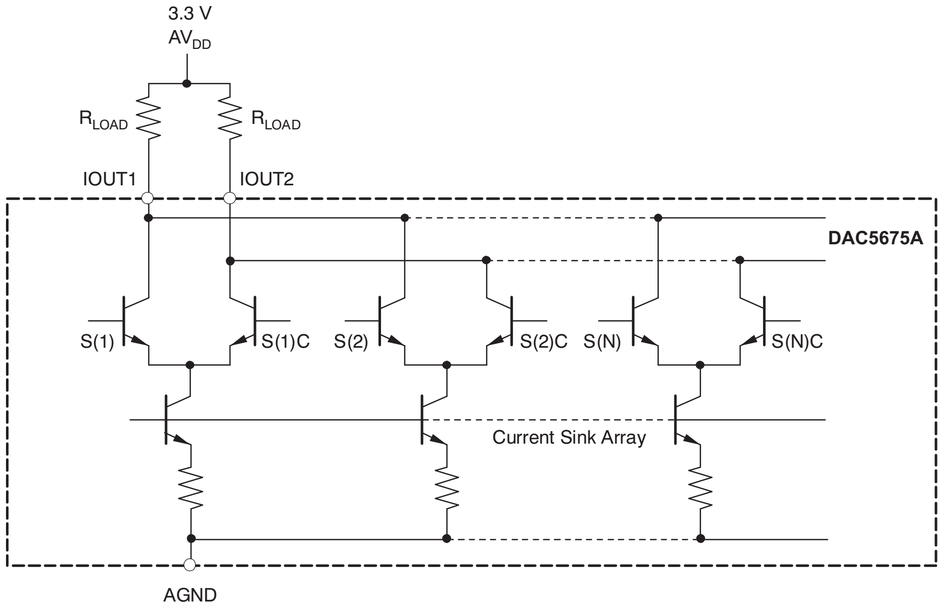


Figure 20. Equivalent Analog Current Output

Figure 21(a) shows the typical differential output configuration with two external matched resistor loads. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} (0.5 V_{PP} single ended) when applying a 20-mA full-scale output current. The output impedance of the DAC5675A-SP slightly depends on the output voltage at nodes IOUT1 and IOUT2. Consequently, for optimum dc-integral nonlinearity, choose the configuration of Figure 21(b). In this current/voltage (I-V) configuration, terminal IOUT1 is kept at AV_{DD} by the inverting operational amplifier. The complementary output should be connected to AV_{DD} to provide a dc-current path for the current sources switched to IOUT1. The amplifier maximum output swing and the full-scale output current of the DAC determine the value of the feedback resistor, R_{FB}. The capacitor C_{FB} filters the steep edges of the DAC5675A-SP current output, thereby reducing the operational amplifier slew-rate requirements. In this configuration, the operational amplifier should operate at a supply voltage higher than the resistor output reference voltage AV_{DD} as a result of its positive and negative output swing around AV_{DD}. Select node IOUT1 if a single-ended unipolar output is desired.

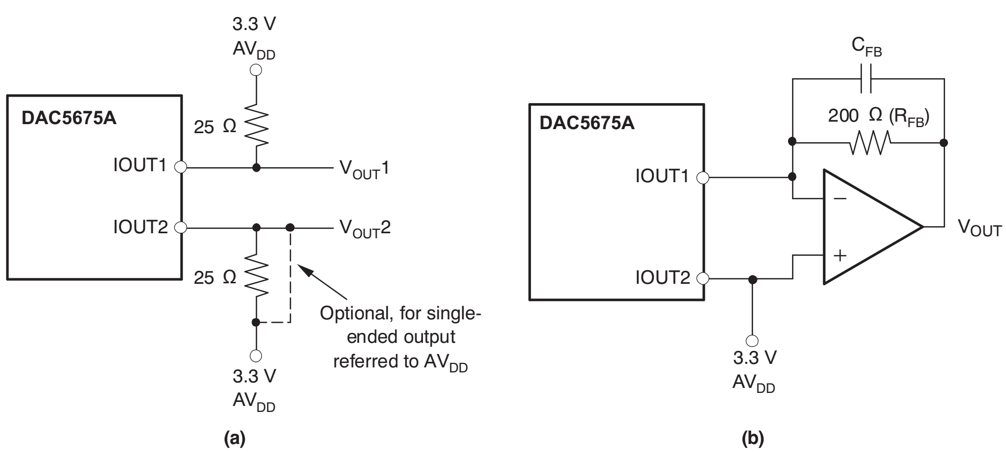


Figure 21. Output Configurations

8.4 Device Functional Modes

8.4.1 Sleep Mode

The DAC5675A-SP features a power-down mode that turns off the output current and reduces the supply current to approximately 6 mA. The power-down mode is activated by applying a logic level one to the SLEEP pin, pulled down internally.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DAC5675A-SP is a 14-bit resolution high-speed DAC. The DAC5675A-SP is designed for high-speed digital data transmission in wired and wireless communication systems, high-frequency DDS, and waveform reconstruction in test and measurement applications. The DAC5675A-SP has excellent SFDR at high intermediate frequencies, which makes it well suited for multicarrier transmission in TDMA and CDMA based cellular BTSs.

9.2 Typical Application

The DAC5675A-SP consists of a segmented array of NPN-transistor current sources, capable of delivering a full-scale output current up to 20 mA. Differential current switches direct the current of each current source to either one of the complementary output nodes IOUT1 or IOUT2. The complementary current output enables differential operation, canceling out common-mode noise sources (digital feed through, on-chip, and PCB noise), dc offsets, and even order distortion components, and doubling signal output power.

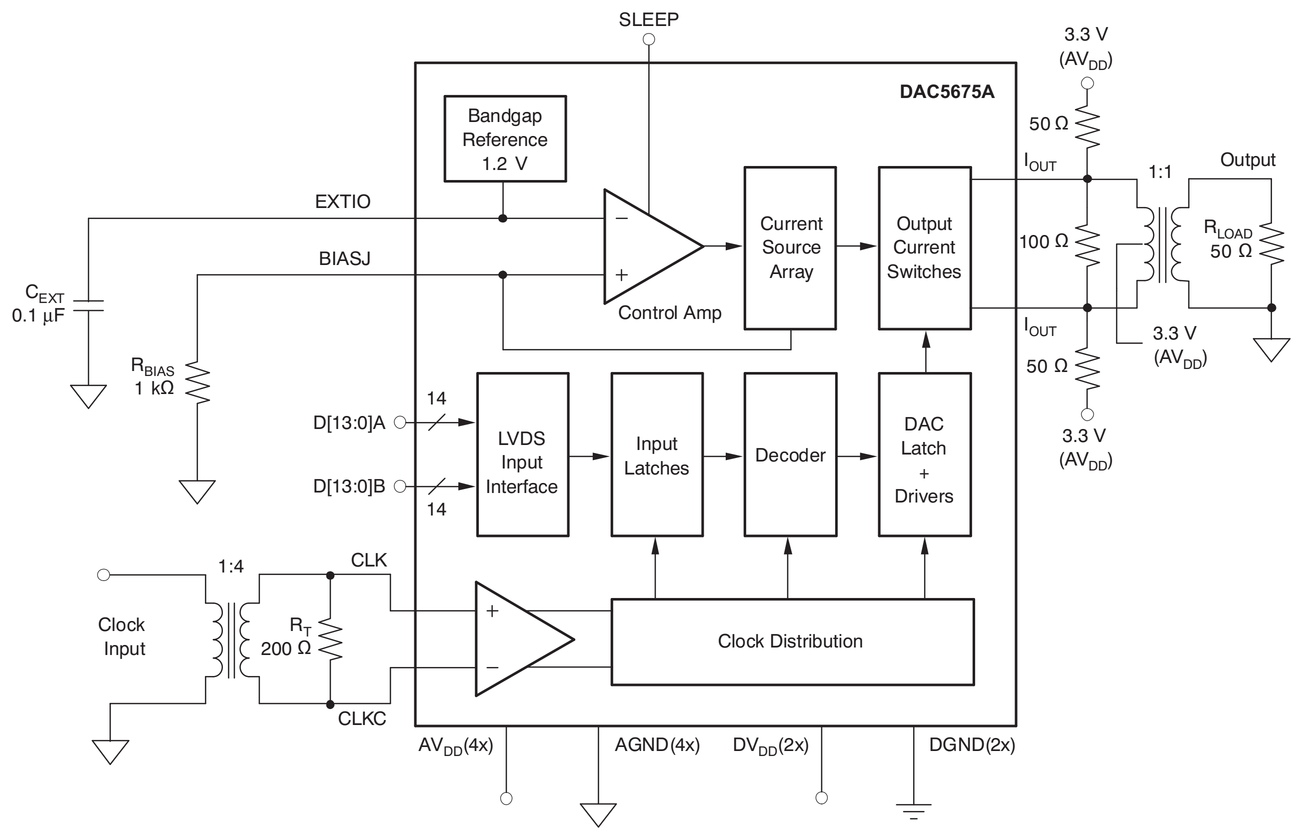


Figure 22. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

Design Parameter	Example Value
Cest	0.1 µF
Rbias	1 kΩ
RT	200 Ω
Rload	50 Ω

9.2.2 Detailed Design Procedure

The DAC5675A-SP can be easily configured to drive a doubly-terminated 50-Ω cable using a properly selected transformer. Figure 23 and Figure 24 show the 1:1 and 4:1 impedance ratio configuration, respectively. These configurations provide maximum rejection of common-mode noise sources and even-order distortion components, thereby doubling the power of the DAC to the output. The center tap on the primary side of the transformer is terminated to AV_{DD}, enabling a dc-current flow for both IOUT1 and IOUT2. Note that the ac performance of the DAC5675A-SP is optimum and specified using a 1:1 differential transformer-coupled output.

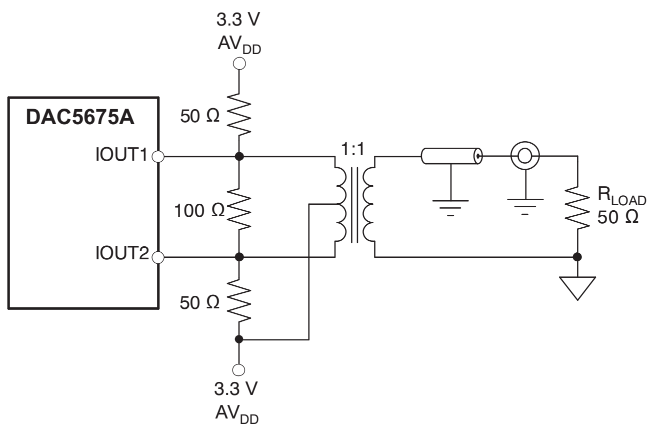


Figure 23. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

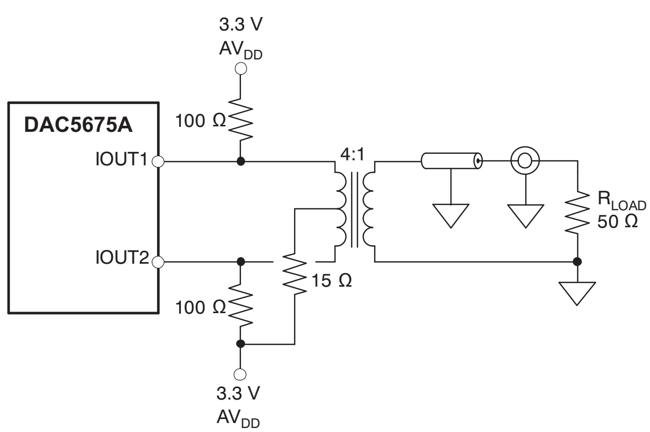


Figure 24. Driving a Doubly Terminated 50 Ω Cable Using a 4:1 Impedance Ratio Transformer

9.2.3 Application Curve

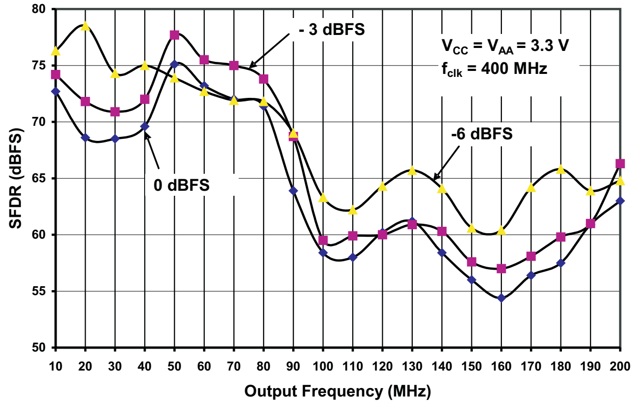


Figure 25. Spurious-Free Dynamic Range vs Frequency

10 Power Supply Recommendations

The DAC5675 uses a single 3.3-V power supply simplifying design requirements. The power supply should be filtered from any other system noise that may be present. The filtering should pay particular attention to frequencies of interest for output.

11 Layout

11.1 Layout Guidelines

- DAC output termination should be placed as close as possible to outputs.
- Keep routing for RBIAS short.
- Decoupling capacitors should be placed as close as possible to supply pins.
- Digital differential inputs must be 50 Ω to ground loosely coupled, or 100-Ω differential tightly coupled.
- Digital differential inputs must be length matched.

11.2 Layout Example

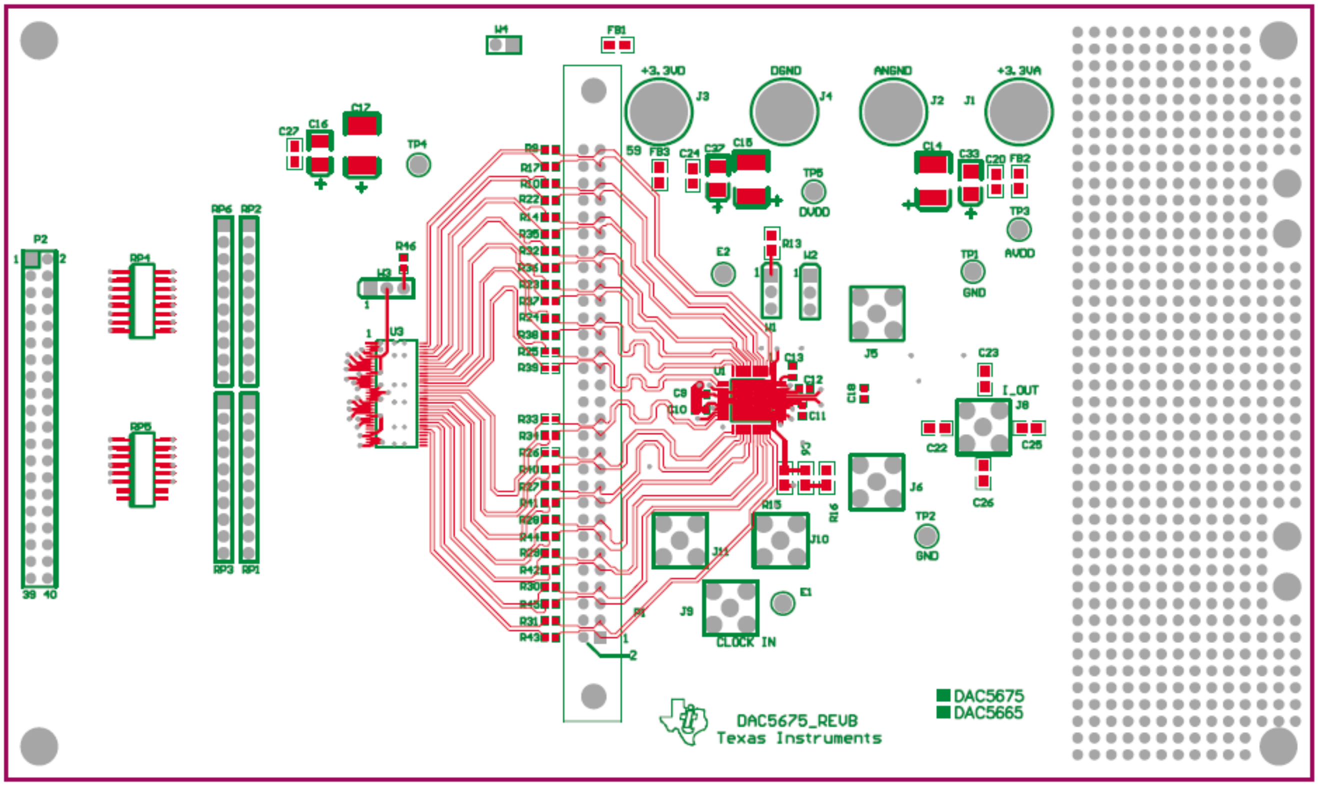


Figure 26. Top Layer

Layout Example (continued)

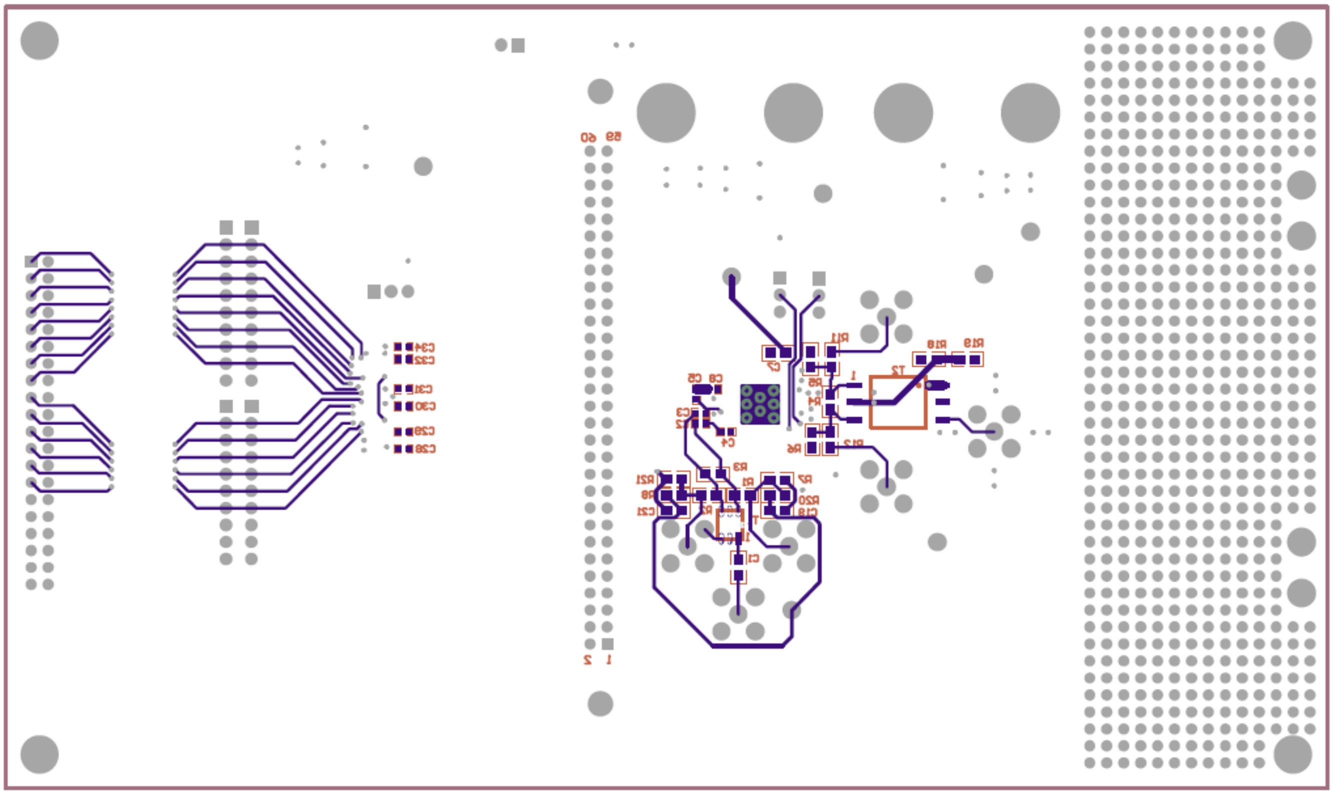


Figure 27. Bottom Layer

11.3 Thermal Considerations

This CQFP package has built-in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly under the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11.9-mm 2-board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically ground potential.

Thermal Considerations (continued)

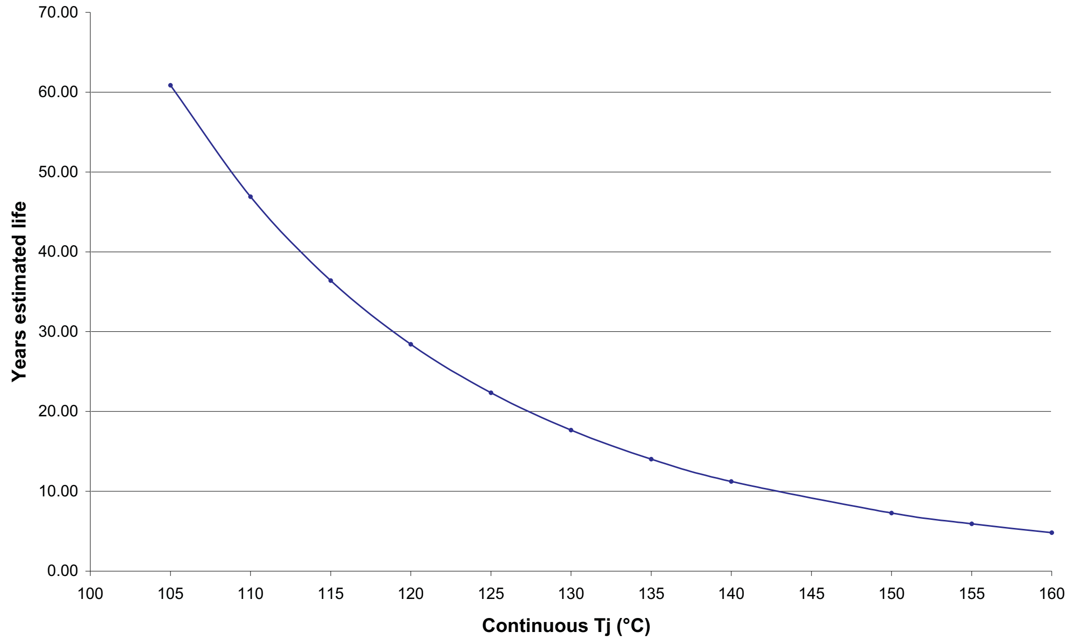


Figure 28. Estimated Device Life at Elevated Temperatures Electromigration Fail Modes

12 Device and Documentation Support

12.1 Device Support

12.1.1 Definitions of Specifications and Terminology

ACPR or adjacent channel power ratio is defined for a 3.84-Mcps 3GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

APSSR or analog power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the analog power supply AV_{DD} from the nominal. This is a dc measurement.

DPSSR or digital power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the digital power supply DV_{DD} from the nominal. This is a dc measurement.

Gain error is as the percentage error in the ratio between the measured full-scale output current and the value of 16 × $V_{(EXTIO)}/R_{BIAS}$. A $V_{(EXTIO)}$ of 1.25 V is used to measure the gain error with an external reference voltage applied. With an internal reference, this error includes the deviation of $V_{(EXTIO)}$ (internal bandgap reference voltage) from the typical value of 1.25 V.

Offset error is as the percentage error in the ratio of the differential output current (IOUT1-IOUT2) and half of the full-scale output current for input code 8192.

SINAD is the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise and harmonics, but excluding dc.

SNR is the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

THD is the ratio of the RMS sum of the first six harmonic components to the RMS value of the fundamental output signal.

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

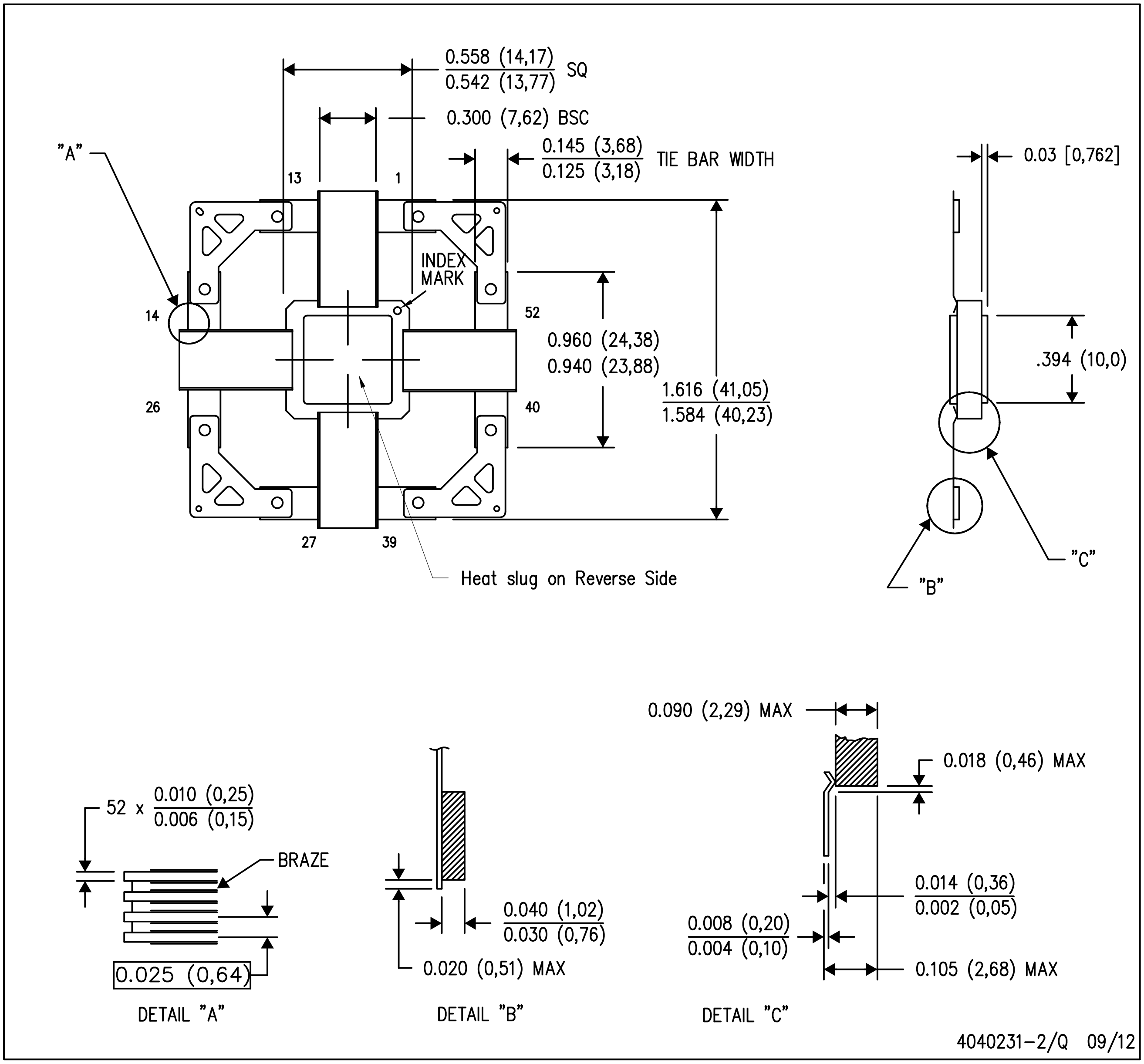
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

HFG (S–CQFP–F52) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0720401VXC	ACTIVE	CFP	HFG	52	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-0720401VX C DAC5675AMHFG-V	Samples
5962-0720402VXC	ACTIVE	CFP	HFG	52	1	TBD	Call TI	N / A for Pkg Type	-55 to 115	5962-0720402VX C DAC5675AWHFG-V	Samples
DAC5675AHFG/EM	ACTIVE	CFP	HFG	52		TBD	Call TI	N / A for Pkg Type	25 Only	DAC5675AHFG/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DAC5675A-SP :

- Catalog: DAC5675A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
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