AUK Semiconductor

S339P

Quad Voltage Comparator

Description

The S339 consists of four independent voltage comparators designed to operate from a single power supply over a wide voltage range.

Features

- Single Supply Operation: 2V to 36V.
- Dual Supply Operation: ±1V to ±18V.
- Allow Comparison of Voltages Near Ground Potential.
- Low Current Drain 800uA Typ.
- Compatible with all Forms of Logic.
- Low Input Bias Current: 25nA Typ.
- Low Input Offset Current: ±5nA Typ.
- Low Offset Voltage: ±1mV Typ.

Applications

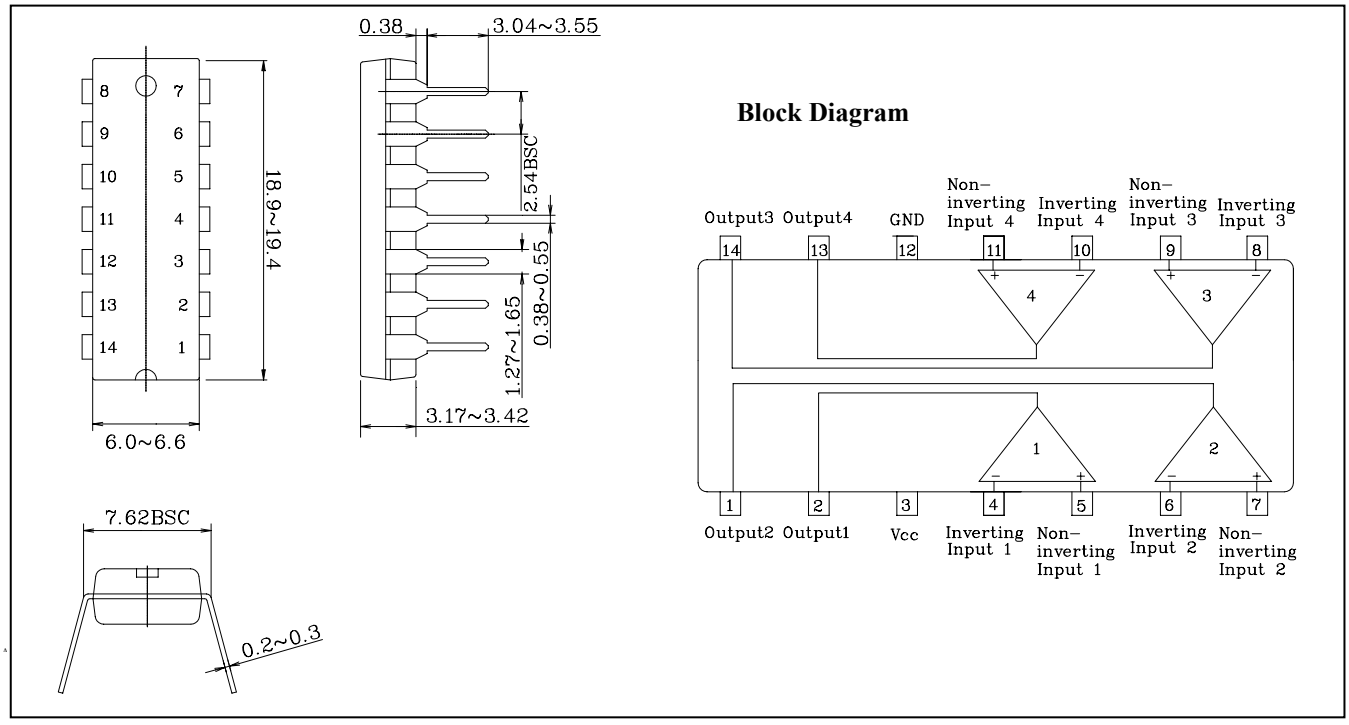
- Transducer amplifier
- DC gain blocks
- Conventional operational amplifiers

Ordering Information

Type NO.	Marking	Package Code
S339P	S339P	DIP-14

Outline Dimensions

unit : mm



Absolute maximum ratings

Characteristic	Symbol	Ratings	Unit
Supply voltage	V_{CC}	36 or ±18	V
Differential input voltage	V_{IND}	36	V
Input voltage	V_{IN}	-0.3 ~ +36	V
Power Dissipation	P_D	570	mW
Operating temperature	T_{opr}	-40 ~ +85	°C
Storage temperature	T_{stg}	-65 ~ 150	°C

Electrical Characteristics

(Unless otherwise specified. V_{CC} = 5V and –40 °C ≤ Ta ≤ +85 °C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{IOS}	V_O = 1.4V, Rs = 0Ω	-	±2	±5	mV
Input Offset Current	I_{IOS}	-	-	±5	±50	nA
Input Bias Current	I_{IB}	-	-	25	250	nA
Input Common Mode Voltage Range	V_{ICR}	-	0	-	V_{CC} –1.5	V
Supply Current	I_{CC}	V_{CC} = 5V, R_L = ∞, All Channel	-	0.8	2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V , R_L = 15 KΩ	-	200	-	V/mV
Output Voltage ('L' Level)	V_{SAT}	V_{IN+}= 0V, V_{IN-}= 1V I_{SINK}≤ 4mA	-	130	400	mV
Response Time	t_{RES}	V_{RC} = 5V, R_L = 5.1KΩ	-	1.3	-	uS
Output Sink Current	I_{SINK}	V_O≤1.5V, V_{IN+} = 0V, V_{IN-} = 1V	6	16	-	mA
Output Leakage Current	I_{Leak}	V_O = 5V V_{IN+} = 1V, V_{IN-} = 0V	-	0.1	-	nA

Electrical Characteristic Curves

Fig. 1 V_{CC}-I_{CC}

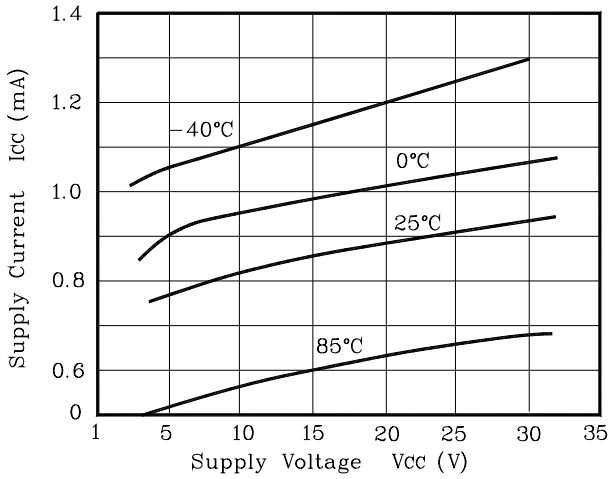


Fig. 2 V_{CC}-I_{IB}

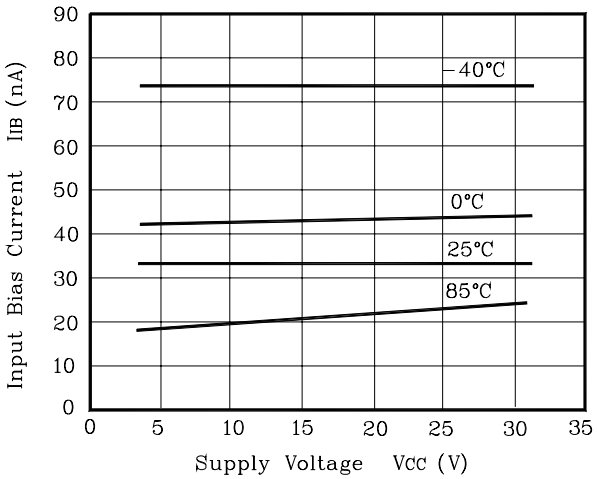


Fig. 3 V_{OL}-I_{SINK}

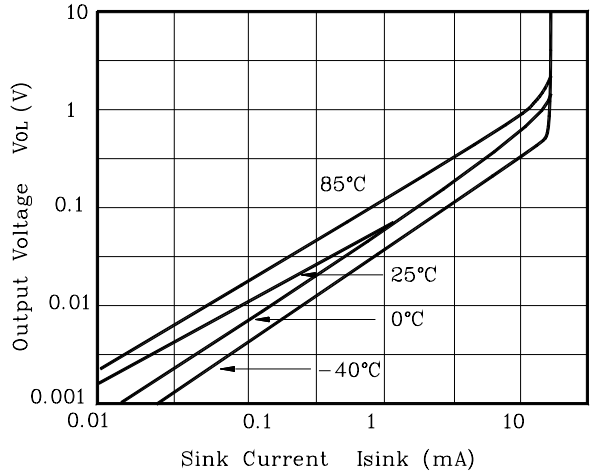


Fig. 4 P_D-Ta

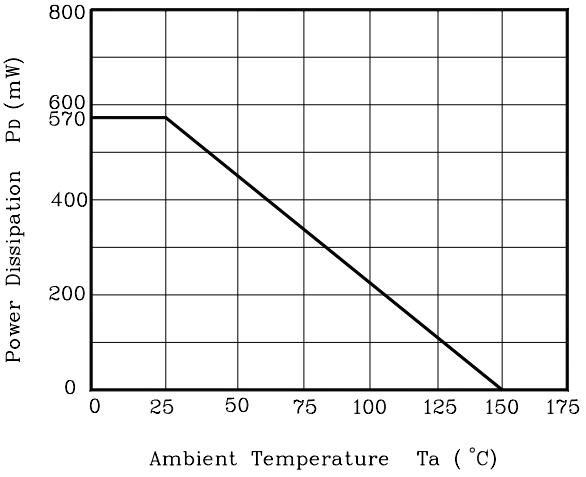


Fig. 5 V_{IN},V_{OUT}-t_{rsp}

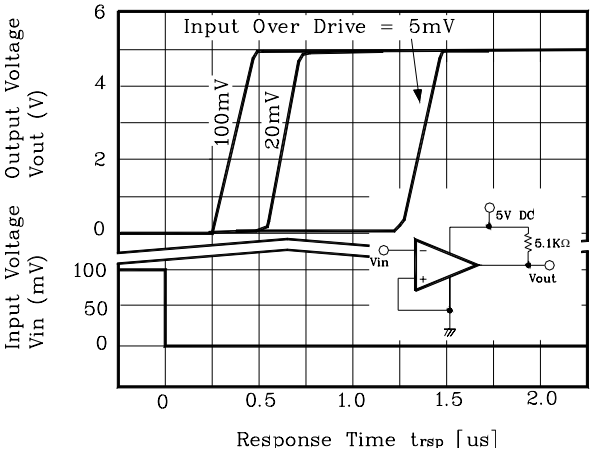
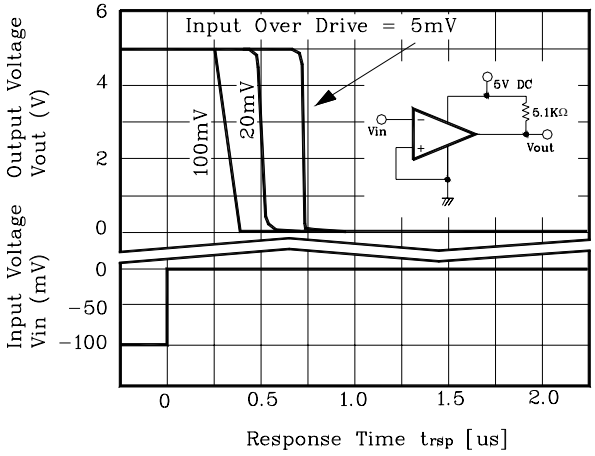


Fig. 6 V_{IN},V_{OUT}-t_{rsp}



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