LPC84x

32-bit Arm® Cortex®-M0+ microcontroller; up to 64 KB flash and 16 KB SRAM; FAIM memory; 12-bit ADC; 10-bit DACs; Comparator; Capacitive Touch Interface

Rev. 1.7 — 27 February 2018 Product data sheet

1. General description

The LPC84x are an Arm Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 30 MHz. The LPC84x support up to 64 KB of flash memory and 16 KB of SRAM.

The peripheral complement of the LPC84x includes a CRC engine, four I^2C-bus interfaces, up to five USARTs, up to two SPI interfaces, Capacitive Touch Interface, one multi-rate timer, self-wake-up timer, SCTimer/PWM, one general purpose 32-bit counter/timer, a DMA, one 12-bit ADC, two 10-bit DACs, one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 54 general-purpose I/O pins.

For additional documentation related to the LPC84x parts, see Section 18.

2. Features and benefits

- System:
  - Arm Cortex-M0+ processor (revision r0p1), running at frequencies of up to 30 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - Arm Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - System tick timer.
  - AHB multilayer matrix.
  - Serial Wire Debug (SWD) with four break points and two watch points. JTAG boundary scan (BSDL) supported.
  - Micro Trace Buffer (MTB).
- Memory:
  - Up to 64 KB on-chip flash programming memory with 64 Byte page write and erase.
  - Fast Initialization Memory (FAIM) allowing the user to configure chip behavior on power-up.
  - Code Read Protection (CRP)
  - Up to 16 KB SRAM consisting of two 8 KB contiguous SRAM banks. One 8 KB of SRAM can be used for MTB.
  - Bit-band addressing supported to permit atomic operations to modify a single bit.
- ROM API support:
  - Boot loader.
  - Supports Flash In-Application Programming (IAP).

- Supports In-System Programming (ISP) through USART, SPI, and I^2C.
- FAIM API.
- FRO API.
- On-chip ROM APIs for integer divide.

- Digital peripherals:
  - High-speed GPIO interface connected to the Arm Cortex-M0+ I/O bus with up to 54 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and digital filter. GPIO direction control supports independent set/clear/toggle of individual bits.
  - High-current source output driver (20 mA) on four pins.
  - High-current sink driver (20 mA) on two true open-drain pins.
  - GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
  - Switch matrix for flexible configuration of each I/O pin function.
  - CRC engine.
  - DMA with 25 channels and 13 trigger inputs.
  - Capacitive Touch Interface.
- Timers:
  - One SCTimer/PWM with five input and seven output functions (including capture and match) for timing and PWM applications. Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 8 match/captures, 8 events, and 8 states.
  - One 32-bit general purpose counter/timer, with four match outputs and three capture inputs. Supports PWM mode, external count, and DMA.
  - Four channel Multi-Rate Timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Self-Wake-up Timer (WKT) clocked from either Free Running Oscillator (FRO), a low-power, low-frequency internal oscillator, or an external clock input in the always-on power domain.
  - Windowed Watchdog timer (WWDT).
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 1.2 Msamples/s. The ADC supports two independent conversion sequences.
  - Comparator with five input pins and external or internal reference voltage.
  - Two 10-bit DACs.
- Serial peripherals:
  - Five USART interfaces with pin functions assigned through the switch matrix and two fractional baud rate generators.
  - Two SPI controllers with pin functions assigned through the switch matrix.
  - Four I^2C-bus interfaces. One I^2C supports Fast-mode Plus with 1 Mbit/s data rates on two true open-drain pins and listen mode. Three I^2Cs support data rates up to 400 kbit/s on standard digital pins.
- Clock generation:

- Free Running Oscillator (FRO). This oscillator provides a selectable 18 MHz, 24 MHz, and 30 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 1.125 MHz, 1.5 MHz, 1.875 MHz, 9 MHz, 12 MHz, and 15 MHz for system clock. The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- Low power boot at 1.5 MHz using FAIM memory.
- External clock input for clock frequencies of up to 25 MHz.
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- Low power oscillator can be used as a clock source to the watchdog timer.
- Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input, or the internal FRO.
- Clock output function with divider that can reflect all internal clock sources.

- Power control:
  - Reduced power modes: sleep mode, deep-sleep mode, power-down mode, and deep power-down mode.
  - Wake-up from deep-sleep and power-down modes on activity on USART, SPI, and I2C peripherals.
  - Timer-controlled self wake-up from deep power-down mode.
  - Power-On Reset (POR).
  - Brownout detect (BOD).
- Unique device serial number for identification.
- Single power supply (1.8 V to 3.6 V).
- Operating temperature range -40 °C to +105 °C.
- Available in LQFP64, LQFP48, HVQFN48, and HVQFN33 packages.

3. Applications

- Sensor gateways
- Industrial
- Gaming controllers
- 8/16-bit applications
- Consumer
- Climate control
- Simple motor control
- Portables and wearables
- Lighting
- Motor control
- Fire and security applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC845M301JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC845M301JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC845M301JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7× 7 × 0.85 mm	SOT619-1
LPC845M301JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11
LPC844M201JBD64	LQFP64	Plastic low profile quad flat package; 64 leads; body 10× 10 × 1.4 mm	SOT314-2
LPC844M201JBD48	LQFP48	Plastic low profile quad flat package; 48 leads; body 7× 7 × 1.4 mm	SOT313-2
LPC844M201JHI48	HVQFN48	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
LPC844M201JHI33	HVQFN33	HVQFN: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 5 × 5 × 0.85 mm	SOT617-11

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/KB	SRAM/KB	USART	I^2C	SPI	DAC	Capacitive Touch	GPIO	Package
LPC845M301JBD64	64	16	5	4	2	2	yes	54	LQFP64
LPC845M301JBD48	64	16	5	4	2	2	yes	42	LQFP48
LPC845M301JHI48	64	16	5	4	2	2	yes	42	HVQFN48
LPC845M301JHI33	64	16	5	4	2	1	-	29	HVQFN33
LPC844M201JBD64	64	8	2	2	2	-	-	54	LQFP64
LPC844M201JBD48	64	8	2	2	2	-	-	42	LQFP48
LPC844M201JHI48	64	8	2	2	2	-	-	42	HVQFN48
LPC844M201JHI33	64	8	2	2	2	-	-	29	HVQFN33

5. Marking

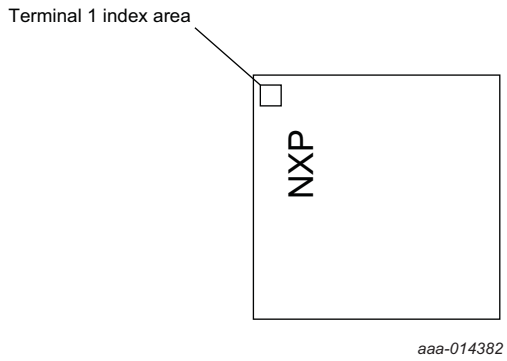


Fig 1. HVQFN48, HVQFN33 package marking

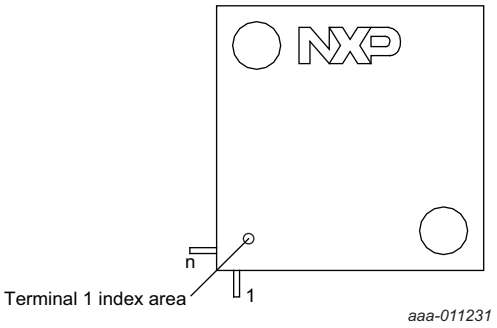


Fig 2. LQFP64, LQFP48 package marking

The LPC84x LQFP64 and LQFP48 packages have the following top-side marking:

- First line: LPC84xMy01
  - y: 3 or 2
- Second line: xxxxxx
- Third line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

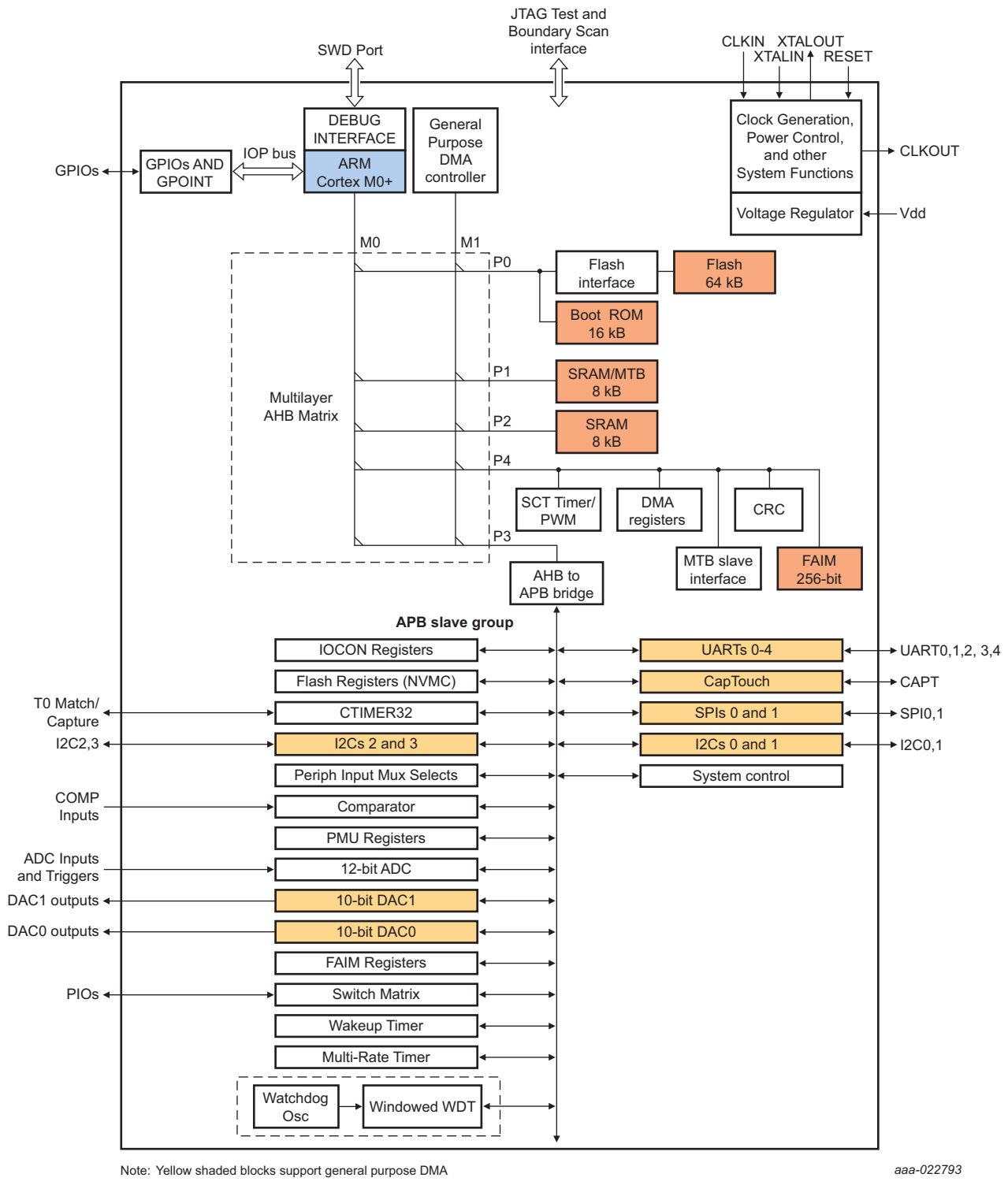
The LPC84x HVQFN48 and HVQFN33 packages have the following top-side marking:

- First line: LPC84xMy01
  - y: 3 or 2
- Second line: xxxxxx
- Third line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 13.1

6. Block diagram



Gray-shaded blocks show peripherals that can provide hardware triggers or fixed DMA requests for DMA transfers.

Fig 3. LPC84x block diagram

7. Pinning information

7.1 Pinning

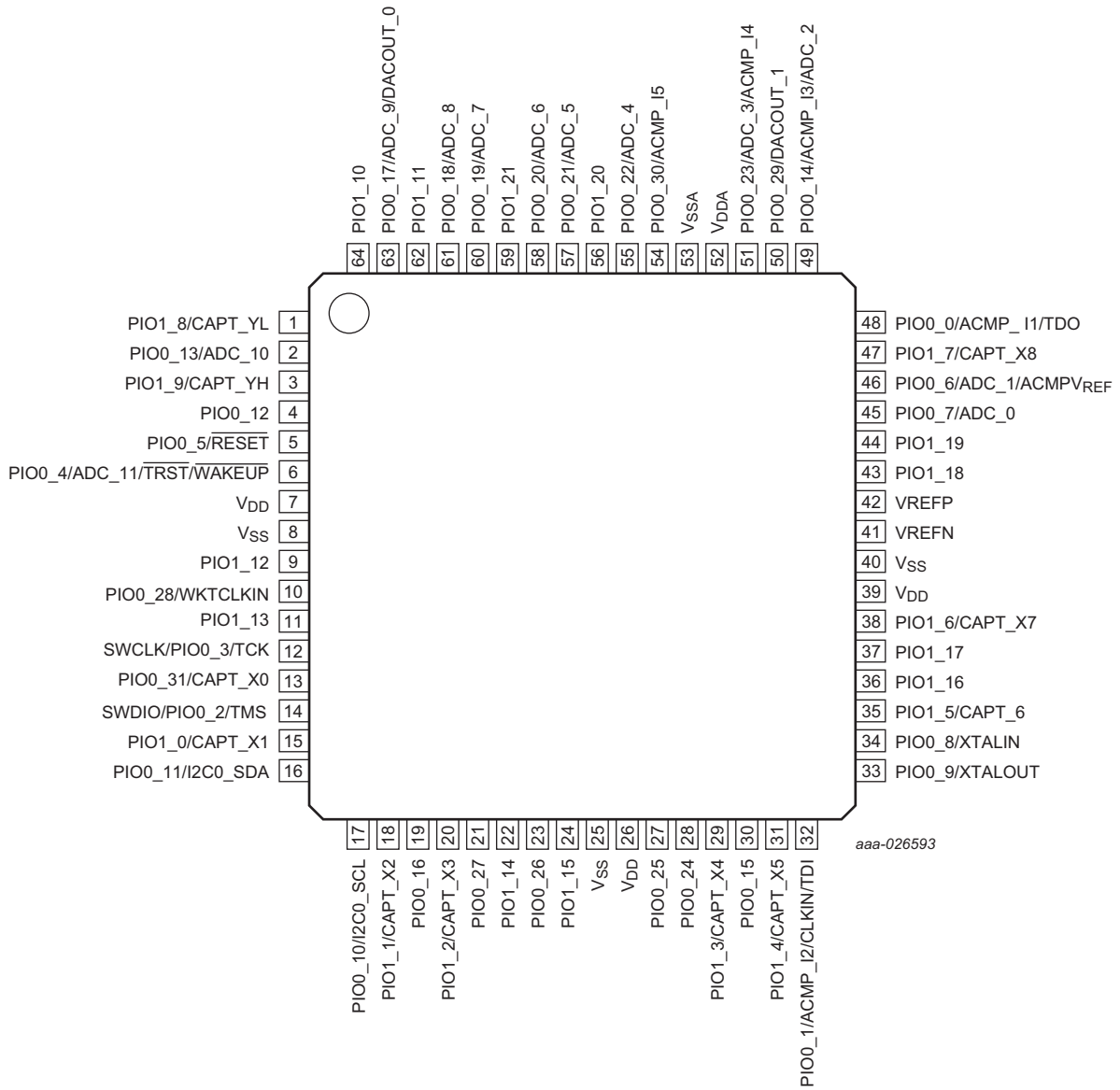


Fig 4. Pin configuration LQFP64 package

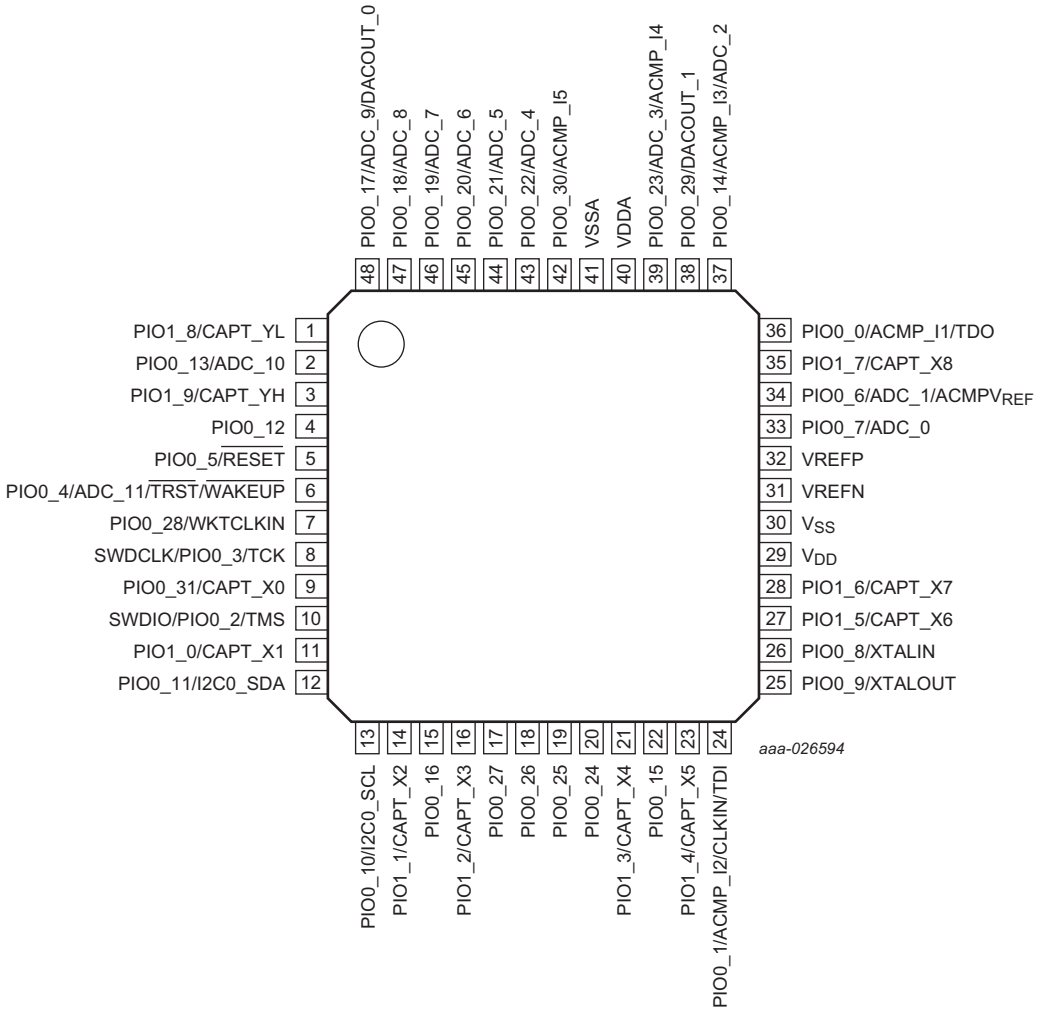


Fig 5. Pin configuration LQFP48 package

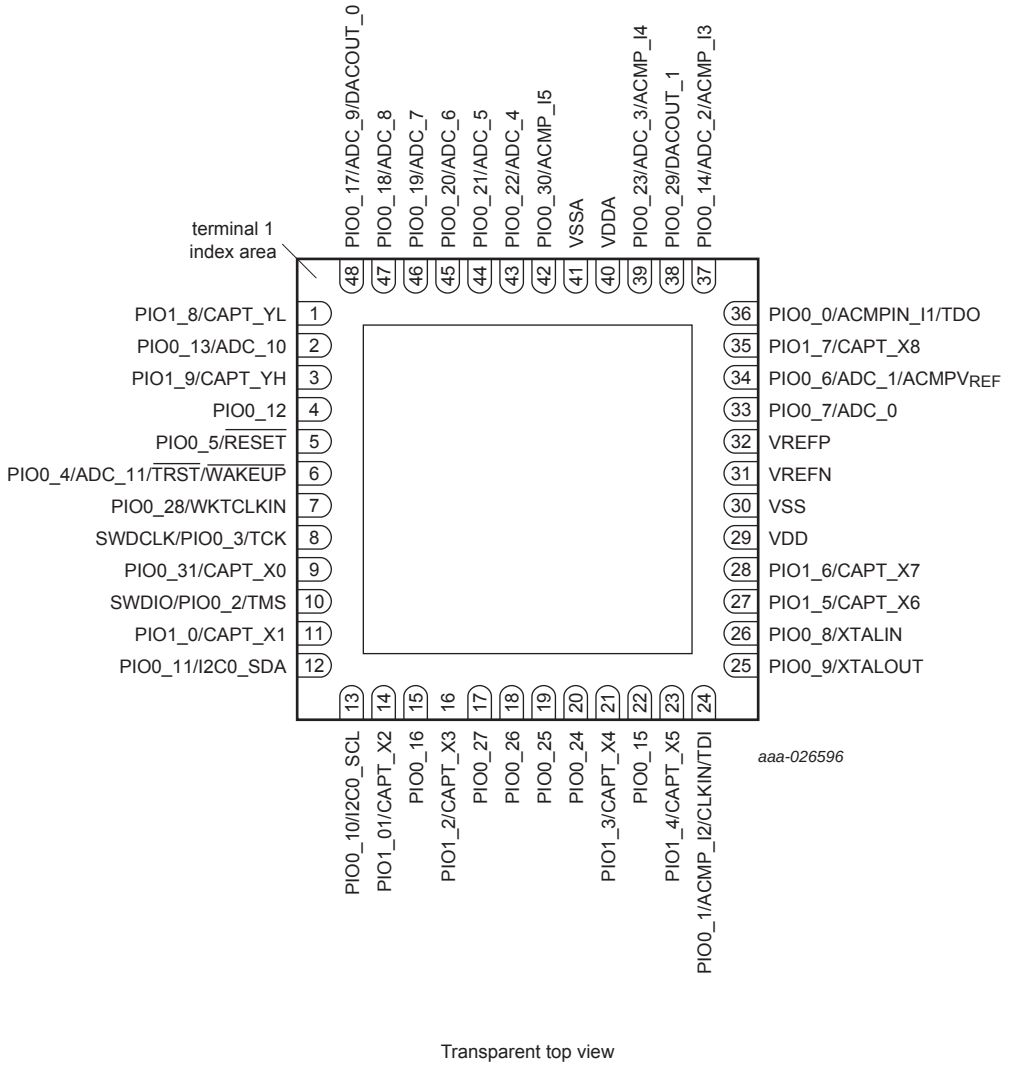


Fig 6. Pin configuration HVQFN48 package

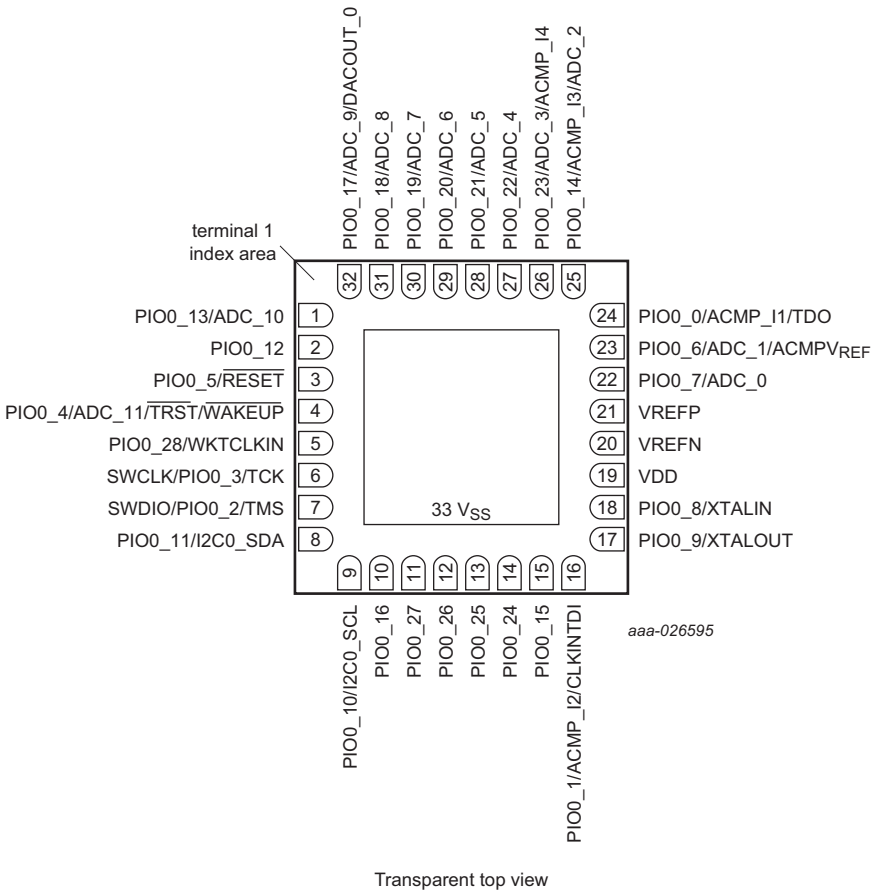


Fig 7. Pin configuration HVQFN33 package

7.2 Pin description

The pin description table shows the pin functions that are fixed to specific pins on each package. See Table 4. These fixed-pin functions are selectable through the switch matrix between GPIO and the comparator, ADC, SWD, RESET, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable functions for the I^2C, USART, SPI, CTimer, SCT pins, and other peripherals can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

Do not assign more than one output to any pin. However, an output and/or one or more inputs can be assigned to a pin. Once any function is assigned to a pin, the pin's GPIO functionality is disabled.

Pin PIO0_4 triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via an external pin, do not assign any movable function to this pin.

PIO0_10 and PIO_11 are high current source pins while PIO0_2, PIO0_3, PIO0_12, and PIO0_16 are high drive output pins.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_0/ACMP_I1/ TDO	48	36	36	24	[2]	I; PU	IO	**PIO0_0 —** General-purpose port 0 input/output 0. In boundary scan mode: TDO (Test Data Out).
							A	**ACMP_I1 —** Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	32	24	24	16	[2]	I; PU	IO	**PIO0_1 —** General-purpose port 0 input/output 1. In boundary scan mode: TDI (Test Data In).
							A	**ACMP_I2 —** Analog comparator input 2.
							I	**CLKIN —** External clock input.
SWDIO/PIO0_2/ TMS	14	10	10	7	[4]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
							I/O	**PIO0_2 —** General-purpose port 0 input/output 2.
SWCLK/PIO0_3/ TCK	12	8	8	6	[4]	I; PU	I	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
							IO	**PIO0_3 —** General-purpose port 0 input/output 3.
PIO0_4/ADC_11/ TRSTN/WAKEUP	6	6	6	4	[3]	I; PU	IO	**PIO0_4 —** General-purpose port 0 input/output 4. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin, do not assign any movable function to this pin and must be externally pulled HIGH before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode and wakes up the part. The $\overline{\text{WAKEUP}}$ pin can be left unconnected or be used as a GPIO or for any movable function if an external $\overline{\text{WAKEUP}}$ function is not needed.
							A	**ADC_11 —** ADC input 11.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
RESET/PIO0_5	5	5	5	3	[7]	I; PU	I	**RESET —** External reset input: A LOW-going pulse (minimum 20 ns to maximum 50 ns) on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin triggers a wake-up from deep power-down mode. If the part must wake up from deep power-down mode via the RESET pin, do not assign any movable function to this pin and must be externally pulled HIGH before entering deep power-down mode. The RESET pin can be left unconnected or be used as a GPIO or for any movable function if an external RESET function is not needed.
							IO	**PIO0_5 —** General-purpose port 0 input/output 5.
PIO0_6/ADC_1/ $ACMPV_{REF}$	46	34	34	23	[10]	I; PU	IO	**PIO0_6 —** General-purpose port 0 input/output 6.
							A	**ADC_1 —** ADC input 1.
							A	**$ACMPV_{REF}$ —** Alternate reference voltage for the analog comparator.
PIO0_7/ADC_0	45	33	33	22	[2]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7.
							A	**ADC_0 —** ADC input 0.
PIO0_8/XTALIN	34	26	26	18	[8]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
							A	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V in slave mode. See Section 14.2.2 "XTAL input".
PIO0_9/XTALOUT	33	25	25	17	[8]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
							A	**XTALOUT —** Output from the oscillator circuit.
PIO0_10/I2C0_SCL	17	13	13	9	[6]	Inactive	I; F	**PIO0_10 —** General-purpose port 0 input/output 10 (open-drain).
								I2C0_SCL — Open-drain I^2C-bus clock input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_11/I2C0_SDA	16	12	12	8	[6]	Inactive	I; F	**PIO0_11 —** General-purpose port 0 input/output 11 (open-drain).
								I2C0_SDA — Open-drain I^2C-bus data input/output. High-current sink if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_12	4	4	4	2	[4]	I; PU	IO	**PIO0_12 —** General-purpose port 0 input/output 12. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler.
PIO0_13/ADC_10	2	2	2	1	[2]	I; PU	IO	**PIO0_13 —** General-purpose port 0 input/output 13.
							A	**ADC_10 —** ADC input 10.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_14/ ACMP_I3/ADC_2	49	37	37	25	[2]	I; PU	IO	**PIO0_14 —** General-purpose port 0 input/output 14.
							A	**ACMP_I3 —** Analog comparator common input 3.
							A	**ADC_2 —** ADC input 2.
PIO0_15	30	22	22	15	[5]	I; PU	IO	**PIO0_15 —** General-purpose port 0 input/output 15.
PIO0_16	19	15	15	10	[4]	I; PU	IO	**PIO0_16 —** General-purpose port 0 input/output 16.
PIO0_17/ADC_9/ DACOUT_0	63	48	48	32	[2]	I; PU	IO	**PIO0_17 —** General-purpose port 0 input/output 17.
							A	**ADC_9 —** ADC input 9.
							A	**DACOUT_0 —** DAC Output 0.
PIO0_18/ADC_8	61	47	47	31	[2]	I; PU	IO	**PIO0_18 —** General-purpose port 0 input/output 18.
							A	**ADC_8 —** ADC input 8.
PIO0_19/ADC_7	60	46	46	30	[2]	I; PU	IO	**PIO0_19 —** General-purpose port 0 input/output 19.
							A	**ADC_7 —** ADC input 7.
PIO0_20/ADC_6	58	45	45	29	[2]	I; PU	IO	**PIO0_20 —** General-purpose port 0 input/output 20.
							A	**ADC_6 —** ADC input 6.
PIO0_21/ADC_5	57	44	44	28	[2]	I; PU	IO	**PIO0_21 —** General-purpose port 0 input/output 21.
							A	**ADC_5 —** ADC input 5.
PIO0_22/ADC_4	55	43	43	27	[2]	I; PU	IO	**PIO0_22 —** General-purpose port 0 input/output 22.
							A	**ADC_4 —** ADC input 4.
PIO0_23/ADC_3/ ACMP_I4	51	39	39	26	[2]	I; PU	IO	**PIO0_23 —** General-purpose port 0 input/output 23.
							A	**ADC_3 —** ADC input 3.
							A	**ACMP_I4 —** Analog comparator common input 4.
PIO0_24	28	20	20	14	[5]	I; PU	IO	**PIO0_24 —** General-purpose port 0 input/output 24. In ISP mode, this is the U0_RXD pin.
PIO0_25	27	19	19	13	[5]	I; PU	IO	**PIO0_25 —** General-purpose port 0 input/output 25. In ISP mode, this pin is the U0_TXD pin.
PIO0_26	23	18	18	12	[5]	I; PU	IO	**PIO0_26 —** General-purpose port 0 input/output 26.
PIO0_27	21	17	17	11	[5]	I; PU	IO	**PIO0_27 —** General-purpose port 0 input/output 27.
PIO0_28/ WKTCLKIN	10	7	7	5	[3]	I; PU	IO	**PIO0_28 —** General-purpose port 0 input/output 28. This pin can host an external clock for the self-wake-up timer. To use the pin as a self-wake-up timer clock input, select the external clock in the wake-up timer CTRL register. The external clock input is active in all power modes, including deep power-down.
PIO0_29/ DACOUT_1	50	38	38	-	[5]	I; PU	IO	**PIO0_29 —** General-purpose port 0 input/output 29.
							A	**DACOUT_1 —** DAC output 1.
PIO0_30/ACMP_I5	54	42	42	-	[5]	I; PU	IO	**PIO0_30 —** General-purpose port 0 input/output 30.
							A	**ACMP_I5 —** Analog comparator common input 5.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
PIO0_31/CAPT_X0	13	9	9	-	[5]	I; PU	IO	**PIO0_31 —** General-purpose port 0 input/output 31.
								CAPT_X0 — Capacitive Touch X sensor 0.
PIO1_0/CAPT_X1	15	11	11	-	[5]	I; PU	IO	**PIO1_0 —** General-purpose port 1 input/output 0.
								CAPT_X1 — Capacitive Touch X sensor 1.
PIO1_1/CAPT_X2	18	14	14	-	[5]	I; PU	IO	**PIO1_1 —** General-purpose port 1 input/output 1.
								CAPT_X2 — Capacitive Touch X sensor 2.
PIO1_2/CAPT_X3	20	16	16	-	[5]	I; PU	IO	**PIO1_2 —** General-purpose port 1 input/output 2.
								CAPT_X3 — Capacitive Touch X sensor 3.
PIO1_3/CAPT_X4	29	21	21	-	[5]	I; PU	IO	**PIO1_3 —** General-purpose port 1 input/output 3.
								CAPT_X4 — Capacitive Touch X sensor 4.
PIO1_4/CAPT_X5	31	23	23	-	[5]	I; PU	IO	**PIO1_4 —** General-purpose port 1 input/output 4.
								CAPT_X5 — Capacitive Touch X sensor 5.
PIO1_5/CAPT_X6	35	27	27	-	[5]	I; PU	IO	**PIO1_5 —** General-purpose port 1 input/output 5.
								CAPT_X6 — Capacitive Touch X sensor 6.
PIO1_6/CAPT_X7	38	28	28	-	[5]	I; PU	IO	**PIO1_6 —** General-purpose port 1 input/output 6.
								CAPT_X7 — Capacitive Touch X sensor 7.
PIO1_7/CAPT_X8	47	35	35	-	[5]	I; PU	IO	**PIO1_7 —** General-purpose port 1 input/output 7.
								CAPT_X8 — Capacitive Touch X sensor 8.
PIO1_8/CAPT_YL	1	1	1	-	[5]	I; PU	IO	**PIO1_8 —** General-purpose port 1 input/output 8.
								CAPT_YL — Capacitive Touch Y Low.
PIO1_9/CAPT_YH	3	3	3	-	[5]	I; PU	IO	**PIO1_9 —** General-purpose port 1 input/output 9.
								CAPT_YH — Capacitive Touch Y High.
PIO1_10	64	-	-	-	[5]	I; PU	IO	**PIO1_10 —** General-purpose port 1 input/output 10.
PIO1_11	62	-	-	-	[5]	I; PU	IO	**PIO1_11 —** General-purpose port 1 input/output 11.
PIO1_12	9	-	-	-	[5]	I; PU	IO	**PIO1_12 —** General-purpose port 1 input/output 12.
PIO1_13	11	-	-	-	[5]	I; PU	IO	**PIO1_13 —** General-purpose port 1 input/output 13.
PIO1_14	22	-	-	-	[5]	I; PU	IO	**PIO1_14 —** General-purpose port 1 input/output 14.
PIO1_15	24	-	-	-	[5]	I; PU	IO	**PIO1_15 —** General-purpose port 1 input/output 15.
PIO1_16	36	-	-	-	[5]	I; PU	IO	**PIO1_16 —** General-purpose port 1 input/output 16.
PIO1_17	37	-	-	-	[5]	I; PU	IO	**PIO1_17 —** General-purpose port 1 input/output 17.
PIO1_18	43	-	-	-	[5]	I; PU	IO	**PIO1_18 —** General-purpose port 1 input/output 18.
PIO1_19	44	-	-	-	[5]	I; PU	IO	**PIO1_19 —** General-purpose port 1 input/output 19.
PIO1_20	56	-	-	-	[5]	I; PU	IO	**PIO1_20 —** General-purpose port 1 input/output 20.
PIO1_21	59	-	-	-	[5]	I; PU	IO	**PIO1_21 —** General-purpose port 1 input/output 21.
V_{DD}	7;26;39	29	29	19		-	-	Supply voltage for the I/O pad ring, the and core voltage regulator.
V_{DDA}	52	40	40					Analog supply voltage.
V_{SS}	8;25;40	30	30	33[11]		-	-	Ground.

Table 4. Pin description

Symbol	LQFP64	LQFP48	HVQFN48	HVQFN33		Reset state[1]	Type	Description
V_{SSA}	53	41	41					Analog ground.
VREFN	41	31	31	20		-	-	ADC negative reference voltage.
VREFP	42	32	32	21		-	-	ADC positive reference voltage. Must be equal or lower than V_{DDA}.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled; F = floating. For pin states in the different power modes, see Section 14.6 “Pin states in different power modes”. For termination on unused pins, see Section 14.5 “Termination of unused pins”.

[2] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. This pin is active in deep power-down mode and includes a 20 ns glitch filter (active in all power modes). In deep power-down mode, pulling the $\overline{\text{WAKEUP}}$ pin LOW wakes up the chip. The wake-up pin function can be disabled and the pin can be used for other purposes, if the WKT low-power oscillator is enabled for waking up the part from deep power-down mode. See Table 20 “Dynamic characteristics: WKTCLKIN pin” for the WKTCLKIN input.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[6] True open-drain pin. I^2C-bus pins compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[7] See Figure 14 for the reset pad configuration. This pin includes a 20 ns glitch filter (active in all power modes). $\overline{\text{RESET}}$ functionality is available in deep power-down mode. Use the $\overline{\text{WAKEUP}}$ pin to reset the chip and wake up from deep power-down mode.

[8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured for XTALIN and XTALOUT, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[9] The WKTCLKIN function is enabled in the DPDCTRL register in the PMU. See the LPC84x user manual.

[10] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

[11] Thermal pad for HVQFN33.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_31, PIO1_0 to PIO1_21 through switch matrix)

Function name	Type	Description
Ux_TXD	O	Transmitter output for USART0 to USART4.
Ux_RXD	I	Receiver input for USART0 to USART4.
$\overline{\text{Ux\_RTS}}$	O	Request To Send output for USART0 to USART4.
$\overline{\text{Ux\_CTS}}$	I	Clear To Send input for USART0 to USART4.
Ux_SCLK	I/O	Serial clock input/output for USART0 to USART4 in synchronous mode.
SPIx_SCK	I/O	Serial clock for SPI0 and SPI1.
SPIx_MOSI	I/O	Master Out Slave In for SPI0 and SPI1.
SPIx_MISO	I/O	Master In Slave Out for SPI0 and SPI1.

Table 5. Movable functions (assign to pins PIO0_0 to PIO0_31, PIO1_0 to PIO1_21 through switch matrix)

Function name	Type	Description
SPIx_SSEL0	I/O	Slave select 0 for SPI0 and SPI1.
SPIx_SSEL1	I/O	Slave select 1 for SPI0 and SPI1.
SPIx_SSEL2	I/O	Slave select 2 for SPI0 and SPI1.
SPIx_SSEL3	I/O	Slave select 3 for SPI0 and SPI1.
SCT_PIN0	I	Pin input 0 to the SCT input multiplexer.
SCT_PIN1	I	Pin input 1 to the SCT input multiplexer.
SCT_PIN2	I	Pin input 2 to the SCT input multiplexer.
SCT_PIN3	I	Pin input 3 to the SCT input multiplexer.
SCT_OUT0	O	SCT output 0.
SCT_OUT1	O	SCT output 1.
SCT_OUT2	O	SCT output 2.
SCT_OUT3	O	SCT output 3.
SCT_OUT4	O	SCT output 4.
SCT_OUT5	O	SCT output 5.
I2Cx_SDA	I/O	I^2C1, I^2C2, and I^2C3 bus data input/output.
I2Cx_SCL	I/O	I^2C1, I^2C2, and I^2C3 bus clock input/output.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.
T0_MAT0	O	Timer Match channel 0.
T0_MAT1	O	Timer Match channel 1.
T0_MAT2	O	Timer Match channel 2.
T0_MAT3	O	Timer Match channel 3.
T0_CAP0	I	Timer Capture channel 0.
T0_CAP1	I	Timer Capture channel 1.
T0_CAP2	I	Timer Capture channel 2.

8. Functional description

8.1 Arm Cortex-M0+ core

The Arm Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. The core revision is r0p1.

Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The Arm Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 On-chip flash program memory

The LPC84x contain up to 64 KB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

8.3 On-chip SRAM

The LPC84x contain a total of 16KB on-chip static RAM data memory in two separate SRAM blocks with one combined clock for both SRAM blocks. One 8 KB of SRAM can be used for MTB.

A bit-band module is added in series with the AHB matrix to allow atomic read-modify-write operations acting on a single bit.

8.4 FAIM memory

The LPC84x includes the FAIM memory and is used to configure the part at start-up. It is 128/256 bits in size and is used to configure the following:

- Clocks and PMU for low-power start-up.
- Low power boot at 1.5 MHz using FAIM memory.
- Pin configuration including direction and pull- up or pull-down.
- Specification of pins to use for ISP entry for each serial peripheral.
- Select whether SWCLK and SWDIO are enabled on reset.

Remark: The FAIM programming voltage range is 3.0 V ≤ Vdd ≤ 3.6 V.

8.5 On-chip ROM

The on-chip ROM contains the bootloader:

- Boot loader.
- Supports Flash In-Application Programming (IAP).
- Supports In-System Programming (ISP) through USART, SPI, and I^2C.
- On-chip ROM APIs for integer divide.
- FAIM API.
- FRO API.

8.6 Memory map

The LPC84x incorporates several distinct memory regions. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The Arm private peripheral bus includes the Arm core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.

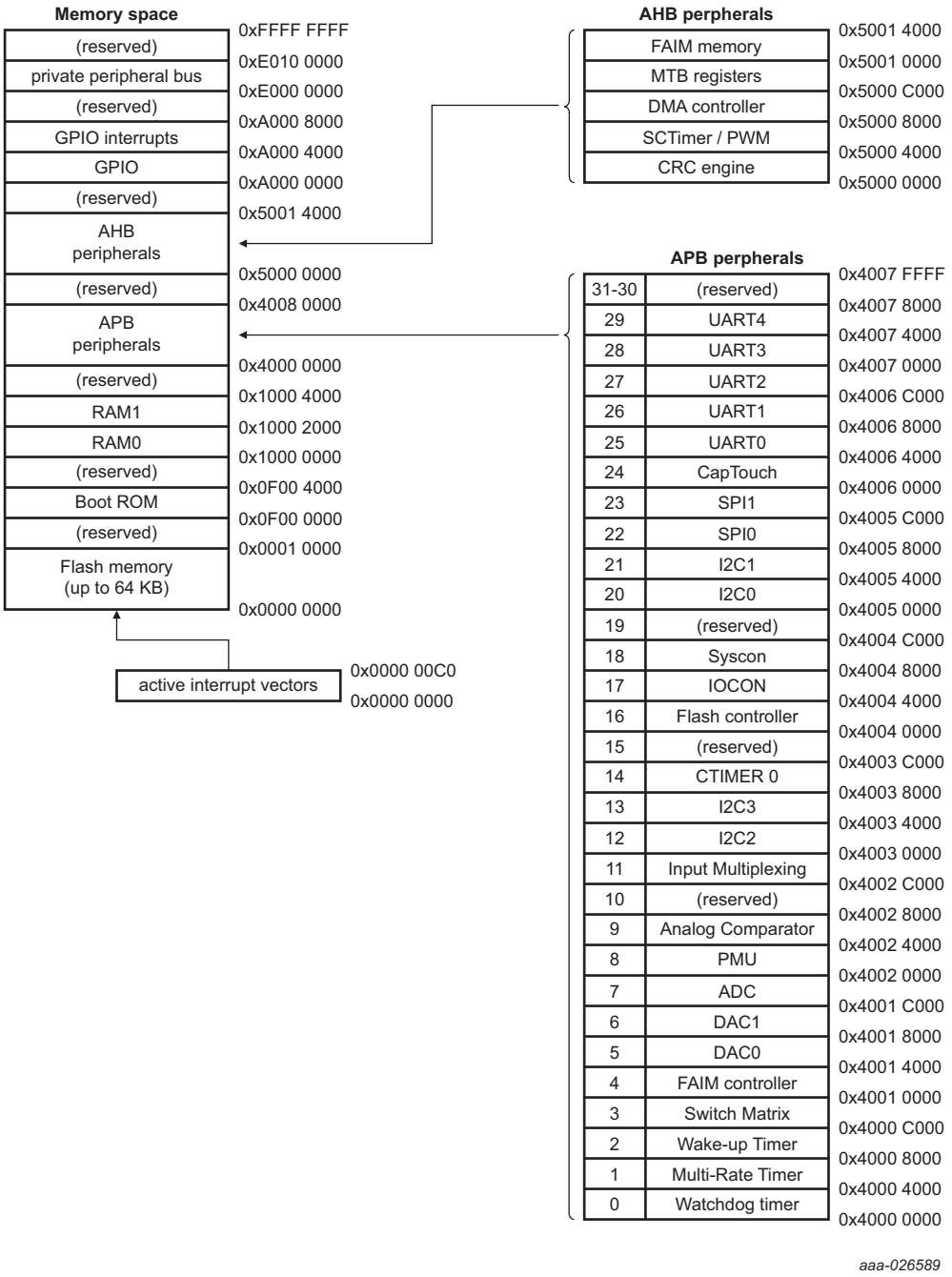


Fig 8. LPC84x AHB Memory mapping

8.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.7.1 Features

- Nested Vectored Interrupt Controller is a part of the Arm Cortex-M0+.
- Tightly coupled interrupt controller provides low interrupt latency.
- Controls system exceptions and peripheral interrupts.
- Supports 32 vectored interrupts.
- In the LPC84x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the Arm exceptions SVCall and PendSV.
- Supports NMI.

8.7.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.8 System tick timer

The Arm Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

8.9 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in Table 4 can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.
- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see Figure 11 “LPC84x clock generation”). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- The switch matrix setting enables the analog input mode on pins with analog and digital functions. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See Section 8.10 for details.

8.9.1 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output.
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled.
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Digital input: Programmable input digital filter selectable on all pins.
- Analog input: Selected through the switch matrix.

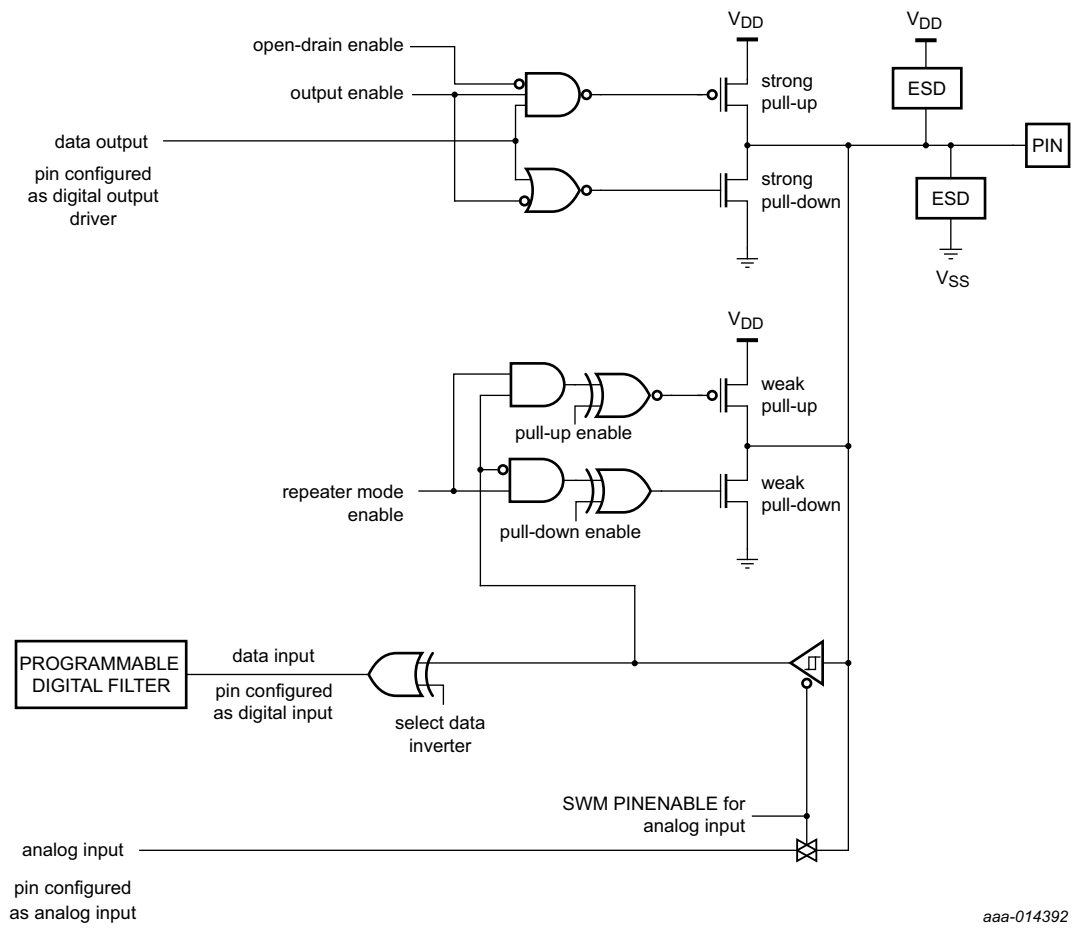


Fig 9. Standard I/O pad configuration

8.10 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions, for example, the USART, SPI, SCTimer/PWM, CTimer, and I^2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in Table 5.

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in Table 4. If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

8.11 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC84x use accelerated GPIO functions:

- GPIO registers are on the Arm Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 15 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

8.11.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to GPIO inputs with internal pull-up resistors enabled after reset - except for the I^2C-bus true open-drain pins PIO0_10 and PIO0_11.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see Figure 9).
- Direction (input/output) can be set and cleared individually.
- Pin direction bits can be toggled.

8.12 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.12.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the LPC84x from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to eight pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be also programmed to generate an RXEV notification to the Arm CPU. The RXEV signal can be connected to a pin.
  - The pattern match engine does not facilitate wake-up.

8.13 DMA controller

The DMA controller can access all memories and the USART, SPI, I^2C, DAC, and Capacitive Touch. DMA transfers can also be triggered by internal events like the ADC interrupts, the pin interrupts (PININT0 and PININT1), the SCTimer DMA requests, CTimer, and the DMA trigger outputs.

8.13.1 Features

- Twenty five channels with each channel connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events or by two pin interrupts. Each DMA channel can select one trigger input from13 sources.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with two entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

8.13.2 DMA trigger input MUX (TRIGMUX)

Each DMA trigger is connected to a programmable multiplexer which connects the trigger input to one of multiple trigger sources. Each multiplexer supports the same trigger sources: the ADC sequence interrupts, the SCT DMA request lines, and pin interrupts PININT0 and PININT1, and the outputs of the DMA triggers 0 and 1 for chaining DMA triggers.

8.14 USART0/1/2/3/4

All USART functions are movable functions and are assigned to pins through the switch matrix.

8.14.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions connected to all digital pins except the open-drain pins.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.

8.15 SPI0/1

All SPI functions are movable functions and are assigned to pins through the switch matrix.

8.15.1 Features

- Maximum data rates of up to 30 Mbit/s in master mode and up to 18 Mbit/s in slave mode for SPI functions connected to all digital pins except the open-drain pins.

- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data, which can be useful while setting up an SPI memory.
- Control information can optionally be written along with data, which allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

8.16 I²C-bus interface (I²C0/1/2/3)

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master.

The I2C0-bus functions are fixed-pin functions. All other I2C-bus functions for I2C1/2/3 are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain pins provide the electrical characteristics to support the full I2C-bus specification (see Ref. 3).

8.16.1 Features

- I2C0 supports Fast-mode Plus with data rates of up to 1 Mbit/s in addition to standard and fast modes on two true open-drain pins.
- True open-drain pins provide fail-safe operation: When the power to an I²C-bus device is switched off, the SDA and SCL pins connected to the I²C0-bus are floating and do not disturb the bus.
- I2C1/2/3 support standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.

8.17 Capacitive Touch Interface

The Capacitive Touch interface is designed to handle up to nine capacitive buttons in different sensor configurations, such as slider, rotary, and button matrix. It operates in sleep, deep sleep, and power-down modes, allowing very low power performance.

The Capacitive Touch module measures the change in capacitance of an electrode plate when an earth-ground connected object (for example, finger) is brought within close proximity.

8.18 SCTimer/PWM

The SCTimer/PWM can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCTimer/PWM can employ up to eight different programmable states, which can change under the control of events, to provide complex timing patterns.

The inputs to the SCT are multiplexed between movable functions from the switch matrix and internal connections such as the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED. The signal on each SCT input is selected through the INPUT MUX.

All outputs of the SCT are movable functions and are assigned to pins through the switch matrix. One SCT output can also be selected as one of the ADC conversion triggers.

8.18.1 Features

- Each SCTimer/PWM supports:
  - Eight match/capture registers.
  - Eight events.
  - Eight states.
  - Five inputs. The fifth input is hard-wired to a clock source. Each input is configurable through an input multiplexer to use one of four external pins (connected through the switch matrix) or one of four internal sources. The maximum input signal frequency is 25 MHz.
  - Six outputs. Connected to pins through the switch matrix.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to eight match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to six single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:

- The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
- Selected events can limit, halt, start, or stop a counter or change its direction.
- Events trigger state changes, output toggles, interrupts, and DMA transactions.
- Match register 0 can be used as an automatic limit.
- In bidirectional mode, events can be enabled based on the count direction.
- Match events can be held until another qualifying event occurs.

- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.
- One SCTimer match output can be selected as ADC hardware trigger input.

8.18.2 SCTimer/PWM input MUX (INPUT MUX)

Each input of the SCTimer/PWM is connected to a programmable multiplexer which allows to connect one of multiple internal or external sources to the input. The available sources are the same for each SCTimer/PWM input and can be selected from four pins configured through the switch matrix, the ADC threshold compare interrupt, the comparator output, and the Arm core signals Arm_TXEV and DEBUG_HALTED.

8.19 CTIMER

8.19.1 General-purpose 32-bit timers/external event counter

The LPC84x has one general-purpose 32-bit timer/counter.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.19.2 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to three 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins can vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.

- Reset timer on match with optional interrupt generation.
- Shadow registers are added for glitch-free PWM output.

- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins can vary by device):
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins can vary by device.)

8.20 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

8.20.1 Features

- 31-bit interrupt timer
- Four channels independently counting down from individually set values
- Bus stall, repeat and one-shot interrupt modes

8.21 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to service the watchdog timer periodically within a programmable time window.

8.21.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) is generated by the dedicated watchdog oscillator (WDOSC).

8.22 Self-Wake-up Timer (WKT)

The self-wake-up timer is a 32-bit, loadable down counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur prior to entering a reduced power mode.

8.22.1 Features

- 32-bit loadable down counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports three clock sources: an external clock on the WKTCLKIN pin, the low-power oscillator, and the FRO. The low-power oscillator is located in the always-on power domain, so it can be used as the clock source in deep power-down mode.
- The WKT can be used for waking up the part from any reduced power mode, including deep power-down mode, or for general-purpose timing.

8.23 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in Table 29.

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled through the switch matrix.

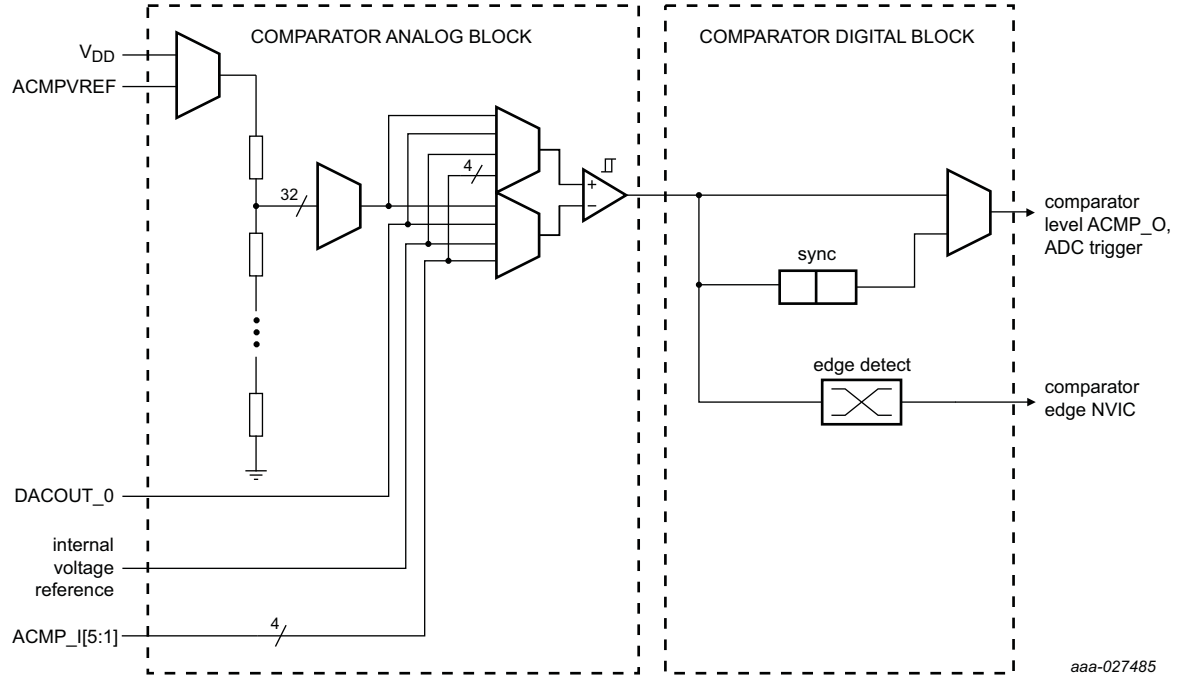


Fig 10. Comparator block diagram

8.23.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or $ACMPV_{REF}$); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- One comparator output is internally collected to the ADC trigger input multiplexer.

8.24 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 1.2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the pin triggers, the SCT output SCT_OUT3, the analog comparator output, and the Arm TXEV.

The ADC includes a hardware threshold compare function with zero-crossing detection.

Remark: For best performance, select VREFP and VREFN at the same voltage levels as V_{DD} and V_{SS}. When selecting VREFP and VREFN different from VDD and VSS, ensure that the voltage midpoints are the same:

(VREFP-VREFN)/2 + VREFN = V_{DD}/2

8.24.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 1.2 MSamples/s.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (not to exceed V_{DD} voltage level).
- Burst conversion mode for single or multiple inputs.
- Hardware calibration mode.

8.25 Digital-to-Analog Converter (DAC)

The DAC supports a resolution of 10 bits. Conversions can be triggered by an external pin input or an internal timer.

The DAC includes an optional automatic hardware shut-off feature which forces the DAC output voltage to zero while a HIGH level on the external DAC_SHUTOFF pin is detected.

8.25.1 Features

- 10-bit digital-to-analog converter.
- Supports DMA.
- Internal timer or pin external trigger for staged, jitter-free DAC conversion sequencing.
- Automatic hardware shut-off triggered by an external pin.

8.26 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

8.26.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.

- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

8.27 Clocking and power control

8.27.1 Crystal and internal oscillators

The LPC84x include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. Free Running Oscillator.
3. Watchdog Oscillator
4. Low Power Oscillator

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC84x operates from the FRO until switched by software allowing the part to run without any external crystal and the bootloader code to operate at a known frequency.

See Figure 11 for an overview of the LPC84x clock generation.

8.27.1.1 Free Running Oscillator (FRO)

The FRO oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- This oscillator provides a selectable 18 MHz, 24 MHz, and 30 MHz outputs that can be used as a system clock. Also, these outputs can be divided down to 1.125 MHz, 1.5 MHz, 1.875 MHz, 9 MHz, 12 MHz, and 15 MHz for system clock.
- The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range of 0 C to 70 C.
- By default, the fro_oscout is 24 MHz and is divided by 2 to provide a default system (CPU) clock frequency of 12 MHz.

8.27.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

8.27.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is ± 40%.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz (± 40% accuracy) oscillator serves as the clock input to the WKT. This oscillator can be configured to run in all low-power modes.

8.27.2 Clock input

An external clock source can be supplied on the selected CLKIN pin directly to the PLL input. When selecting a clock signal for the CLKIN pin, follow the specifications for digital I/O pins in Table 13 “Static characteristics, supply pins” and Table 19 “Dynamic characteristics: I/O pins[1]”.

An 1.8 V external clock source can be supplied on the XTALIN pins to the system oscillator limiting the voltage of this signal (see Section 14.2 “XTAL oscillator”).

The maximum frequency for both clock signals is 25 MHz.

8.27.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is nominally 100 μs.

8.27.4 Clock output

The LPC84x features a clock output function that routes the FRO, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

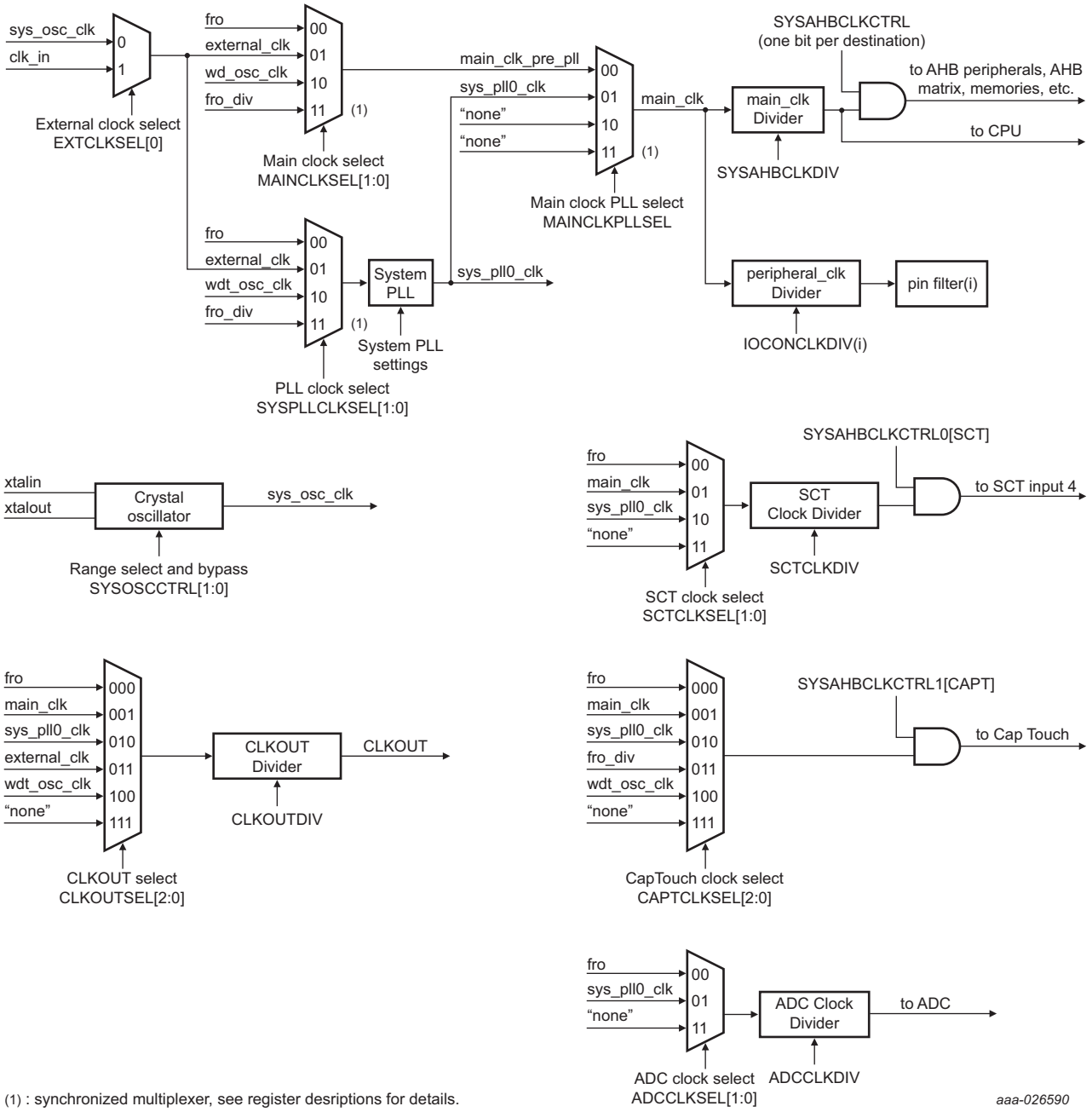


Fig 11. LPC84x clock generation

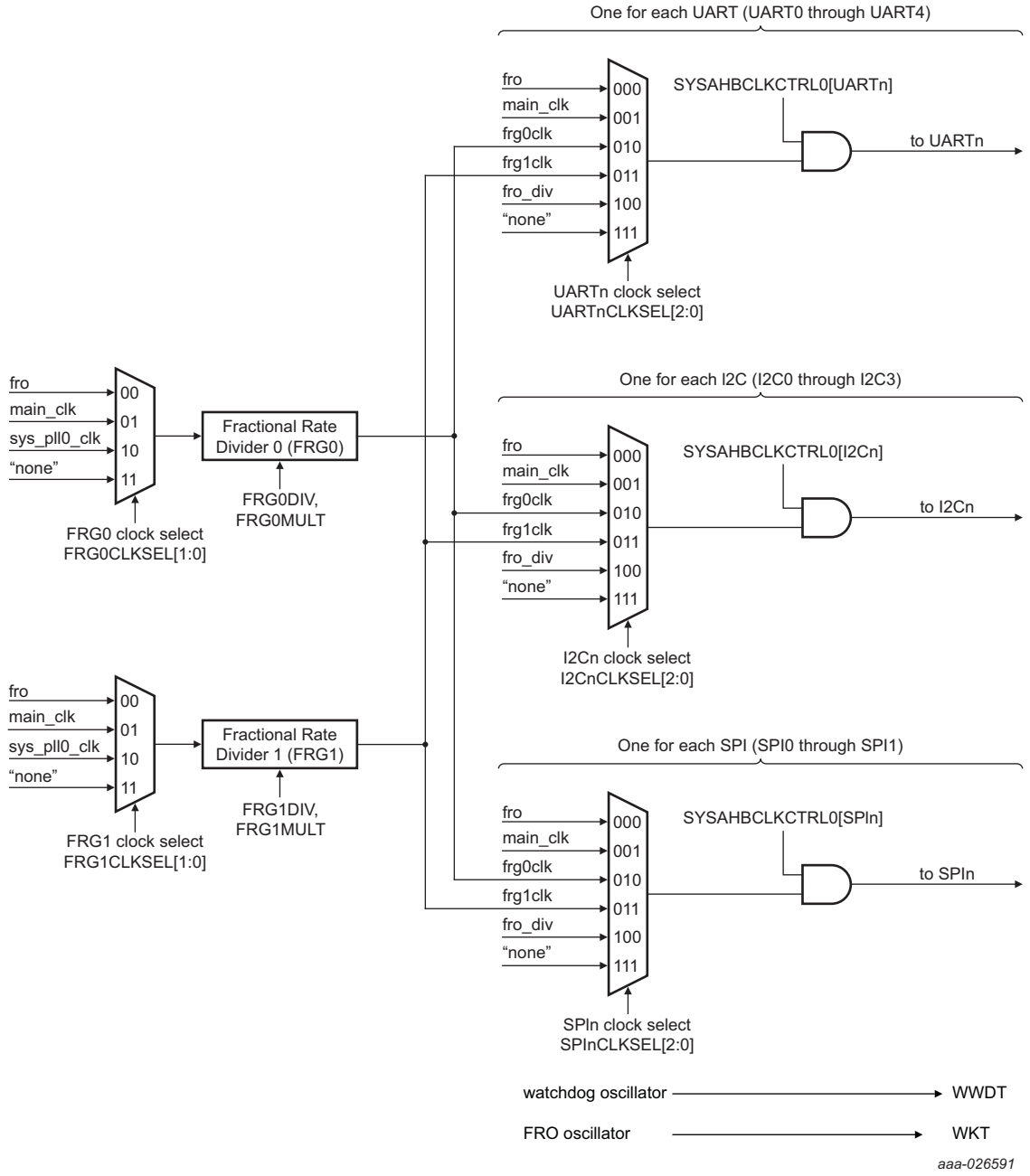


Fig 12. LPC84x clock generation (continued)

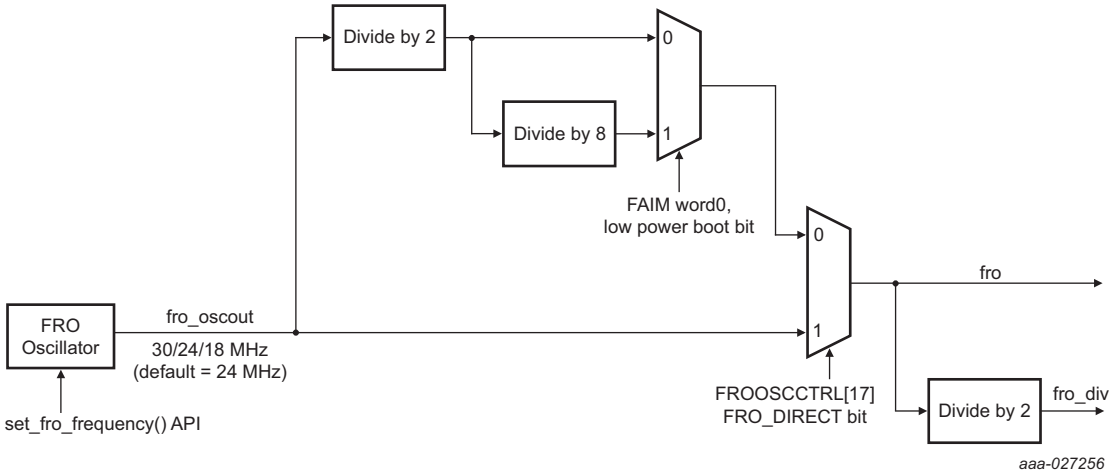


Fig 13. LPC84x FRO subsystem

Table 6. Clocking diagram signal name descriptions

Name	Description
sys_osc_clk	This is the internal clock that comes from external crystal oscillator through dedicated pins.
frg_clk	The output of the Fractional Rate Generator. The FRG and its source selection are shown in Figure 12 “LPC84x clock generation (continued)”.
fro	The output of the currently selected on-chip FRO oscillator. See UM11029 User manual.
fro_div	The FRO output. This may be either 15 MH, 12 MHz, or 9 MHz. See UM11029 User manual.
main_clk	The main clock used by the CPU and AHB bus, and potentially many others. The main clock and its source selection are shown in Figure 11 “LPC84x clock generation”.
“none”	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.
sys_pll0_clk	The output of the System PLL. The System PLL and its source selection are shown in Figure 11 “LPC84x clock generation”.
wdt_osc_clk	The output of the watchdog oscillator, which has a selectable target frequency. It must also be enabled in the PDRINCFG0 register. See UM11029 User manual.
xtalin	Input of the main oscillator. If used, this is connected to an external crystal and load capacitor.
xtalout	Output of the main oscillator. If used, this is connected to an external crystal and load capacitor.
clk_in	This is the internal clock that comes from the main CLK_IN pin function. Connect that function to the pin by selecting it in the IOCON block.
external_clk	This is the internal clock that comes from the external crystal oscillator or the CLK_IN pin.

8.27.5 Power control

The LPC84x supports the Arm Cortex-M0+ sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.27.5.1 Sleep mode

When sleep mode is entered, the clock to the core is stopped. Resumption from the sleep mode does not need any special sequence but re-enabling the clock to the Arm core.

In sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

8.27.5.2 Deep-sleep mode

In deep-sleep mode, the LPC84x core is in sleep mode and all peripheral clocks and all clock sources are off except for the FRO and watchdog oscillator or low-power oscillator if selected. The FRO output is disabled. In addition, all analog blocks are shut down and the flash is in standby mode. In deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC84x can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

8.27.5.3 Power-down mode

In power-down mode, the LPC84x is in sleep mode and all peripheral clocks and all clock sources are off except for watchdog oscillator or low-power oscillator if selected. In addition, all analog blocks and the flash are shut down. In power-down mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC84x can wake up from power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, an interrupt from Capacitive Touch, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to deep-sleep mode at the expense of longer wake-up times.

8.27.5.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the $\overline{\text{WAKEUP}}$ pin and the self-wake-up timer. The LPC84x can wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin, $\overline{\text{RESET}}$ pin, or without an external signal by using the time-out of the self-wake-up timer (see Section 8.22).

The LPC84x can be prevented from entering deep power-down mode by setting a lock bit in the PMU block. Locking out deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the part must wake up from deep power-down mode via the $\overline{\text{WAKEUP}}$ pin or $\overline{\text{RESET}}$ pin, do not assign any movable function to this pin and must be externally pulled HIGH before entering deep power-down mode.

Table 7. Peripheral configuration in reduced power modes

Peripheral	Sleep mode	Deep-sleep mode	Power-down mode	Deep power-down mode
FRO	software configurable	on	off	off
FRO output	software configurable	off	off	off
Flash	software configurable	on	off	off
BOD	software configurable	software configurable	software configurable	off
PLL	software configurable	off	off	off
SysOsc	software configurable	off	off	off
WDosc/WWDT	software configurable	software configurable	software configurable	off
Digital peripherals	software configurable	off	off	off
WKT/low-power oscillator	software configurable	software configurable	software configurable	software configurable
ADC	software configurable	off	off	off
DAC0/1	software configurable	off	off	off
Capacitive Touch	software configurable	software configurable	software configurable	off
Comparator	software configurable	off	off	off

Table 8. Wake-up sources for reduced power modes

power mode	Wake-up source	Conditions
Sleep	Any interrupt	Enable interrupt in NVIC.
	$\overline{\text{RESET}}$ pin PIO0_5	Enable the reset function in the PINENABLE0 register via switch matrix.
Deep-sleep and power-down	Pin interrupts	Enable pin interrupts in NVIC and STARTERP0 registers.
	BOD interrupt	• Enable interrupt in NVIC and STARTERP1 registers. • Enable interrupt in BODCTRL register. • BOD powered in PDSLEEPCFG register.
	BOD reset	• Enable reset in BODCTRL register. • BOD powered in PDSLEEPCFG register.
	WWDT interrupt	• Enable interrupt in NVIC and STARTERP1 registers. • WWDT running. Enable WWDT in WWDT MOD register and feed. • Enable interrupt in WWDT MOD register. • WDOsc powered in PDSLEEPCFG register.
	WWDT reset	• WWDT running. • Enable reset in WWDT MOD register. • WDOsc powered in PDSLEEPCFG register.
	Self-Wake-up Timer (WKT) time-out	• Enable interrupt in NVIC and STARTERP1 registers. • Enable low-power oscillator in the DPDCTRL register in the PCON block. • Select low-power clock for WKT clock in the WKT CTRL register. • Start the WKT by writing a time-out value to the WKT COUNT register.
	Interrupt from USART/SPI/I2C peripheral	• Enable interrupt in NVIC and STARTERP1 registers. • Enable USART/I2C/SPI interrupts. • Provide an external clock signal to the peripheral. • Configure the USART in synchronous slave mode and I2C and SPI in slave mode.
	$\overline{\text{RESET}}$ pin PIO0_5	Enable the reset function in the PINENABLE0 register via switch matrix.
	Interrupt from Capacitive Touch peripheral	• Enable interrupt in NVIC and STARTERP1 registers. • Enable the Capacitive Touch interrupt. • Switch FCLK clock source to the WDOsc. • Set Capacitive Touch registers. • Provide a touch event to the peripheral.
Deep power-down	$\overline{\text{WAKEUP}}$ pin PIO0_4	Enable the $\overline{\text{WAKEUP}}$ function in the DPDCTRL register in the PMU.
	$\overline{\text{RESET}}$ pin PIO0_5	Enable the reset function in the DPDCTRL register in the PMU to allow wake-up in deep power-down mode.
	WKT time-out	• Enable the low-power oscillator in the DPDCTRL register in the PMU. • Enable the low-power oscillator to keep running in deep power-down mode in the DPDCTRL register in the PMU. • Select low-power clock for WKT clock in the WKT CTRL register. • Start WKT by writing a time-out value to the WKT COUNT register.

8.27.6 Wake-up process

The LPC84x begin operation at power-up by using the FRO as the clock source allowing chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL are needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

8.28 System control

8.28.1 Reset

Reset has four sources on the LPC84x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the FRO and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

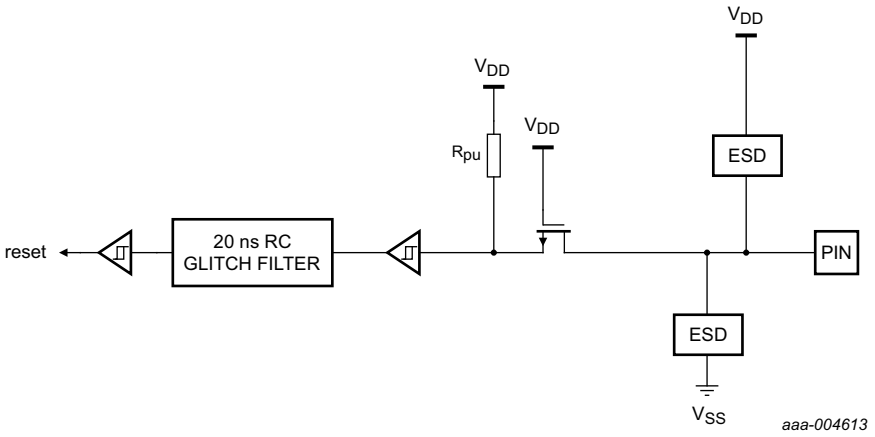


Fig 14. Reset pad configuration

8.28.2 Brownout detection

The LPC84x includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

8.28.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the ISP entry pin can be disabled without enabling CRP. For details, see the *LPC84x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using the ISP entry pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION	
	If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of the ISP entry pin for valid user code can be disabled. For details, see the *LPC84x user manual*.

8.28.4 APB interface

The APB peripherals are located on one APB bus.

8.28.5 AHBLite

The AHBLite connects the CPU bus of the Arm Cortex-M0+ to the flash memory, the main static RAM, the CRC, the DMA, the ROM, and the APB peripherals.

8.29 Emulation and debugging

Debug functions are integrated into the Arm Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The Arm Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC84x.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the Arm SWD debug ($\overline{\text{RESET}}$ = HIGH). The Arm SWD debug port is disabled while the LPC84x is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode (see Table 4).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)		[2]	−0.5	+4.6	V
V_{DDA}	Analog supply voltage	on pin VDDA		−0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP		−0.5	V_{DD}	V
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.8$ V	[3][4]	−0.5	+5.5	V
		on I2C open-drain pins	[5]	−0.5	+5.5	V
		3 V tolerant I/O pin $ACMPV_{REF}$	[6]	−0.5	+3.6	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[7][8] [9]	−0.5	+4.6	V
$V_{i(xtal)}$	crystal input voltage		[2]	−0.5	+2.5	V
I_{DD}	supply current	per supply pin (LQFP64)		-	100	mA
		per supply pin (LQFP48, HVQFN48)		-	75	
		per supply pin (HVQFN33)		-	50	
I_{SS}	ground current	per ground pin (LQFP64);		-	100	mA
		per ground pin (LQFP48, HVQFN48)		-	75	
		per ground pin (HVQFN33)		-	100	
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[10]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C

Table 9. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot(pack)}$	total power dissipation (per package)	LQFP64, based on package heat transfer, not device power consumption	[12]	-	0.66	W
		LQFP64, based on package heat transfer, not device power consumption	[13]	-	0.48	W
		LQFP48, based on package heat transfer, not device power consumption	[12]	-	0.48	W
		LQFP48, based on package heat transfer, not device power consumption	[13]	-	0.34	W
		HVQFN48, based on package heat transfer, not device power consumption	[12]	-	1.12	W
		HVQFN48, based on package heat transfer, not device power consumption	[13]	-	0.46	W
		HVQFN33, based on package heat transfer, not device power consumption	[12]	-	0.98	W
		HVQFN33, based on package heat transfer, not device power consumption	[13]	-	0.34	W
V_{esd}	electrostatic discharge voltage	human body model; all pins		-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 13) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_10 and PIO0_11 and except the 3 V tolerant pin PIO0_6.

[4] Including the voltage on outputs in 3-state mode.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] V_{DD} present or not present.

[7] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[8] If the comparator is configured with the common mode input $V_{IC} = V_{DD}$, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] JEDEC (4.5 in × 4 in); still air.

[13] Single layer (4.5 in × 3 in); still air.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 10. Thermal resistance

Symbol	Parameter	Conditions	Max/min	Unit
HVQFN33 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	40 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	114 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		20 ± 15 %	°C/W
HVQFN48 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	35 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	85 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		9 ± 15 %	°C/W
LQFP48 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	82 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	115 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		30 ± 15 %	°C/W
LQFP64 package				
$R_{th(j-a)}$	thermal resistance from junction-to-ambient	JEDEC (4.5 in × 4 in); still air	59 ± 15 %	°C/W
		single-layer (4.5 in × 3 in); still air	82 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction-to-case		18 ± 15 %	°C/W

11. Static characteristics

11.1 General operating conditions

Table 11. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock		-	-	30	MHz
V_{DD}	supply voltage (core and external rail)		[3]	1.8	-	3.6	V
		FAIM programming only		3.0	-	3.6	V
		For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{DDA}	analog supply voltage	For ADC operations		2.4	-	3.6	V
		For DAC operations		2.7	-	3.6	V
V_{ref}	ADC positive reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	1.8	1.95	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[2]	-	-	7.1	pF
		I^2C-bus pins	[2]	-	-	2.5	pF
		pins with digital functions only	[2]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Including bonding pad capacitance. Based on simulation, not tested in production.

[3] The V_{DD} supply voltage must be 1.9 V or above when connecting an external crystal oscillator to the system oscillator. If the V_{DD} supply voltage is below 1.9 V, an external clock source can be fed to the XTALIN by bypassing the system oscillator or the other clock sources mentioned above can be used.

11.2 Power-up ramp conditions

Table 12. Power-up characteristics[1]

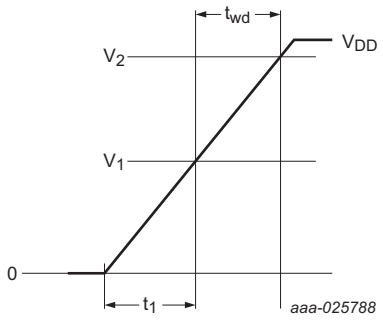
T_{amb} = −40 °C to +105 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{wd}	Window duration (time where $V_1<V_{DD}<V_2$)		-	-	8	ms
V_1	Window low voltage	[2]	1.4	-	-	V
V_2	Window high voltage	[3]	-	-	1.8	V

[1] Assert the external reset pin until V_{DD} is > 1.8 V if the power-up characteristic specification cannot be implemented.

[2] V_{DD} to stay above V_1 for the entire duration t_{wd}.

[3] V_{DD} to stay below V_2 for the minimum duration of t_{wd}.



t_1: The time when there is no restriction on the ramp rate.

Fig 15. Power-up ramp

11.3 Power consumption

Power measurements in active, sleep, deep-sleep, and power-down modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.

Table 13. Static characteristics, supply pins

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[9]	Unit
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash;					
		system clock = 1.5 MHz; V_{DD} = 3.3 V; Low power boot	[3][4][5][6]	-	530	-	µA
		system clock = 12 MHz; V_{DD} = 3.3 V; Normal boot	[3][4][5][6]	-	2.0	-	mA
		system clock = 30 MHz; V_{DD} = 3.3 V; Normal boot	[3][4][5][6]	-	4.0	-	mA
		Sleep mode					
		system clock = 12 MHz; V_{DD} = 3.3 V	[3][4][5][6]	-	1.3	-	mA
		system clock = 30 MHz; V_{DD} = 3.3 V	[3][4][5][6]	-	2.8	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V;	[3][7]				
		T_{amb} = 25 °C		-	240	320	µA
		T_{amb} = 105 °C		-	-	425	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V	[3][7]				
		T_{amb} = 25 °C		-	1.5	10	µA
		T_{amb} = 105 °C		-	-	70	µA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; 10 kHz low-power oscillator and self-wake-up timer (WKT) disabled	[8]				
		T_{amb} = 25 °C		-	0.4	1.0	µA
		T_{amb} = 105 °C		-	-	4.25	µA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; 10 kHz low-power oscillator and self-wake-up timer (WKT) enabled		-	1.3	-	µA
		Deep power-down mode; V_{DD} = 3.3 V; external clock input WKTCLKIN @ 10 kHz with self-wake-up timer enabled		-	0.43	-	µA
		Deep power-down mode; V_{DD} = 3.3 V; external clock input WKTCLKIN @ 32 kHz with self-wake-up timer enabled		-	0.43	-	µA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), VDD = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] FRO enabled; system oscillator disabled; system PLL disabled.

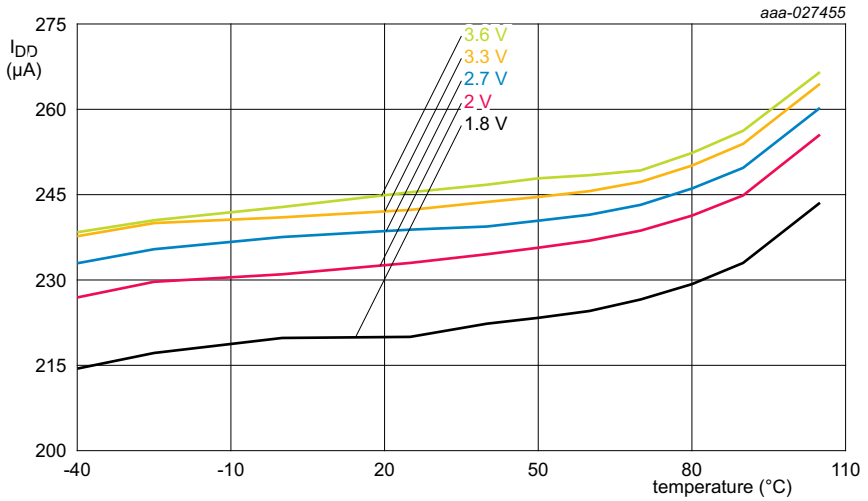
[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks disabled in system configuration block.

[7] All oscillators and analog blocks turned off.

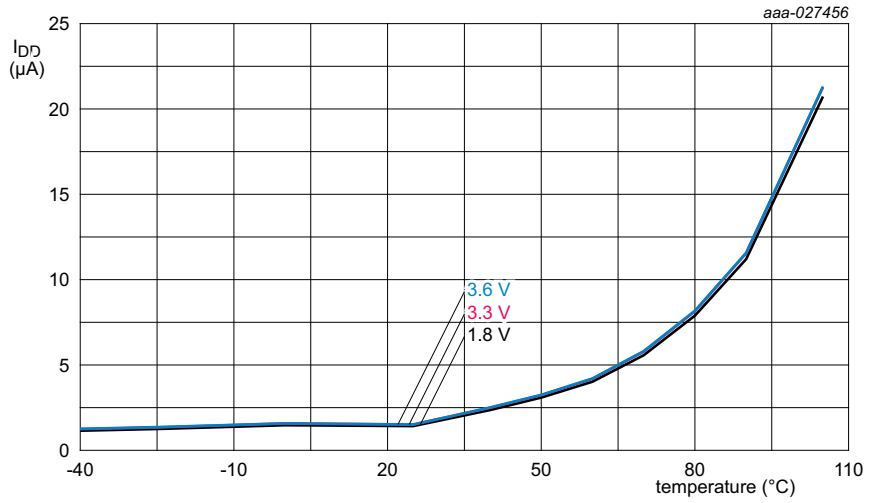
[8] $\overline{\text{WAKEUP}}$ pin pulled HIGH externally.

[9] Tested in production, VDD = 3.6 V.



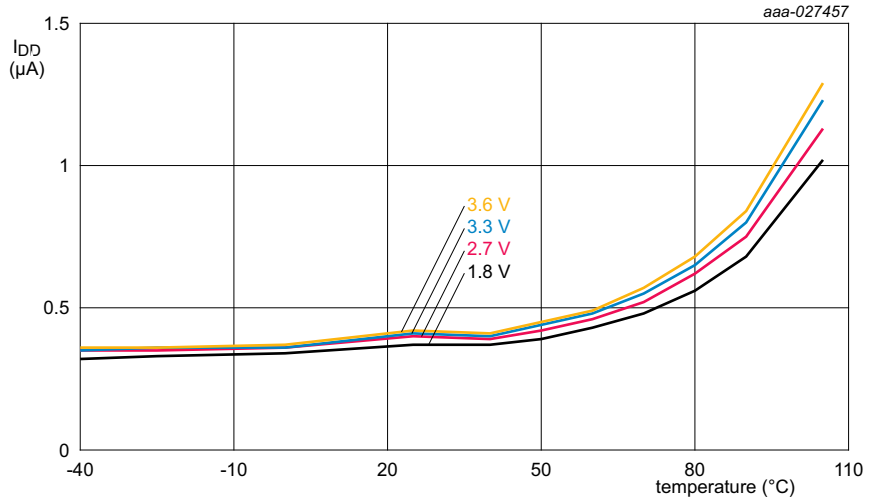
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



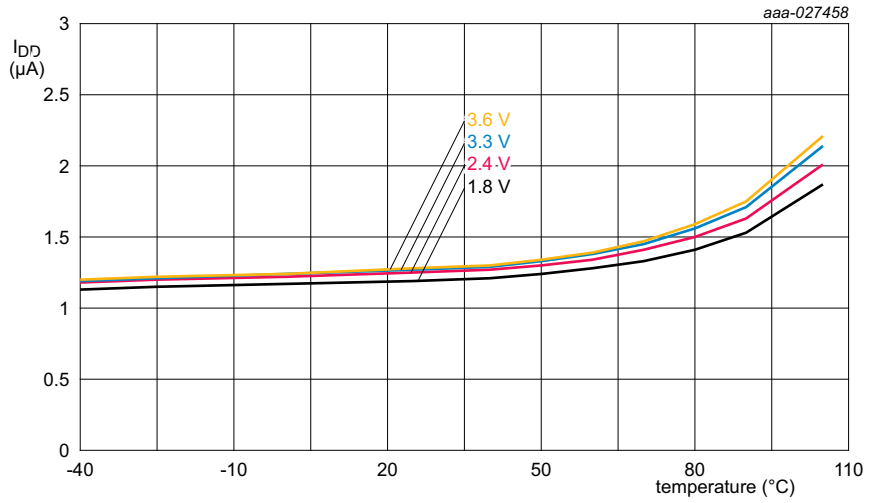
Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 17. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



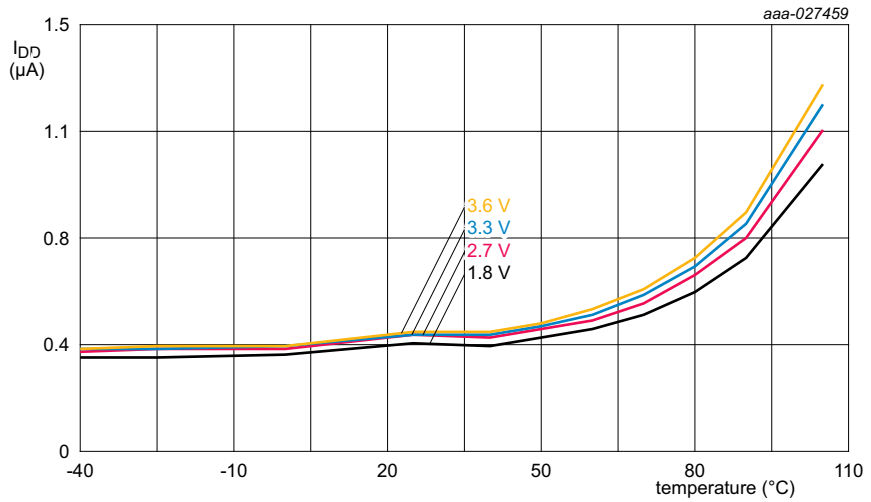
WKT not running.

Fig 18. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



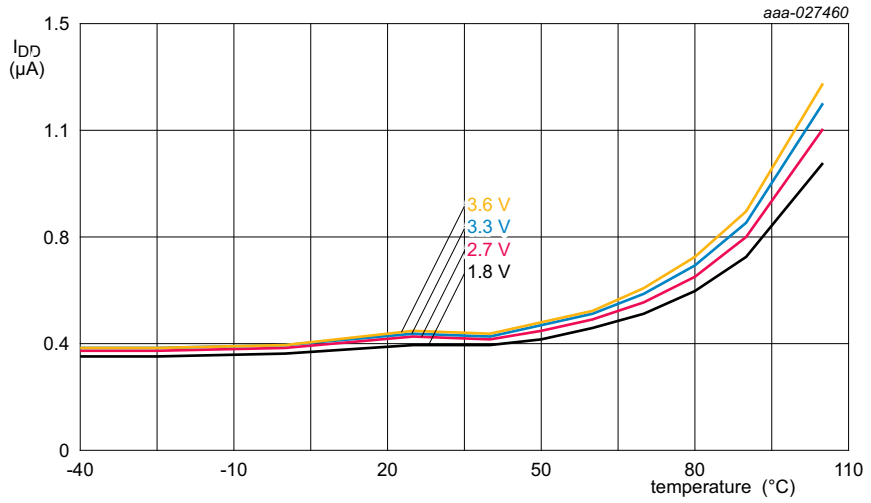
WKT running with internal 10 kHz low-power oscillator.

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (internal clock)



WKT running with external 10 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 20. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 10 kHz input clock)



WKT running with external 32 kHz clock. Clock input waveform: square wave with rise time and fall time of 5 ns.

Fig 21. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD} (external 32 kHz input clock)

11.4 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed. Measured on a typical sample at T_{amb} = 25 °C.

The supply currents are shown for FRO clock frequencies of 12 MHz and 30 MHz.

Table 14. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
FRO	89	-	-	System oscillator running; PLL off; independent of main clock frequency; FRO = 24 MHz. FRO output disabled.
System oscillator at 12 MHz	243	-	-	FRO running; PLL off; independent of main clock frequency.
Watchdog oscillator	1	-	-	FRO; PLL off; independent of main clock frequency.
BOD	42	-	-	Independent of main clock frequency.
Flash	273	-	-	-
Main PLL	156	-	-	FRO (24 MHz) running; Main clock running at fro_div (12 MHz)
CLKOUT	-	25	61	Main clock divided by 4 in the CLKOUTDIV register. Not connected to pin.
ROM	-	35	86	-
GPIO + pin interrupt/pattern match	-	159	384	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
SWM	-	85	206	-
IOCON	-	80	193	-
SCTimer/PWM	-	172	419	-
CTimer		51	123	
MRT	-	102	245	-
WWDT	-	28	70	-
I2C0	-	54	131	-
I2C1	-	47	115	-
I2C2	-	44	106	-
I2C3	-	60	145	-
SPI0	-	43	106	-
SPI1	-	44	107	-
USART0	-	53	128	-
USART1	-	53	130	-
USART2	-	46	90	-

Table 14. Power consumption for individual analog and digital blocks *...continued*

Peripheral	Typical supply current in µA			Notes
	System clock frequency =			
	n/a	12 MHz	30 MHz	
USART3	-	58	142	-
USART4	-	56	137	-
Comparator ACMP	-	79	144	-
ADC	-	78	190	Digital controller only. Analog portion of the ADC disabled in the PDRUNCFG register.
	-	78	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 1 in the ADC CTRL register (ADC in low-power mode).
	-	79	190	Combined analog and digital logic. ADC enabled in the PDRUNCFG register and LPWRMODE bit set to 0 in the ADC CTRL register (ADC powered).
DAC 0	-	46	107	-
DAC 1	-	36	88	-
Capacitive Touch	-	49	117	-
DMA	-	355	858	-
CRC	-	36	83	-

11.5 Pin characteristics

Table 15. Static characteristics, pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins configured as digital pins, RESET							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V; 5 V tolerant pins except PIO0_6		0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		$V_{DD} - 0.4$	-	-	V
		I_{OH} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		$V_{DD} - 0.5$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA; 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		$V_{OH} = V_{DD} - 0.5$ V; 1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[5]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V	[6]	15	50	85	µA
		1.8 V ≤ V_{DD} < 2.0 V		10	50	85	
		$V_{DD} < V_I$ < 5 V		0	0	0	µA
High-drive output pin configured as digital pin (PIO0_2, PIO0_3, PIO0_12, and PIO0_16)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10[2]	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10[2]	nA

Table 15. Static characteristics, pin characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10[2]	nA
V_I	input voltage	$V_{DD} \geq$ 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 20 mA; 2.5 V <= V_{DD} < 3.6 V		V_{DD} − 0.5	-	-	V
		I_{OH} = 12 mA; 1.8 V <= V_{DD} < 2.5 V		V_{DD} − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA 2.5 V <= V_{DD} < 3.6 V		-	-	0.5	V
		I_{OL} = 3 mA 1.8 V <= V_{DD} < 2.5 V		-	-	0.5	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.5 V; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		V_{OH} = V_{DD} − 0.5 V; 1.8 V <= V_{DD} < 2.5 V		12	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[5]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[6]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[6]	−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_10 and PIO0_11)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as standard mode pins 2.5 V <= V_{DD} < 3.6 V		3.5	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; I^2C-bus pins configured as Fast-mode Plus pins; 2.5 V <= V_{DD} < 3.6 V		20	-	-	mA
		1.8 V <= V_{DD} < 2.5 V		16	-	-	mA

Table 15. Static characteristics, pin characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{LI}	input leakage current	$V_I = V_{DD}$	[7]	-	2	4	µA
		V_I = 5 V		-	10	22	µA

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Based on characterization. Not tested in production.

[3] Including voltage on outputs in 3-state mode.

[4] 3-state outputs go into 3-state mode in deep power-down mode.

[5] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[6] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 22.

[7] To V_{SS}.

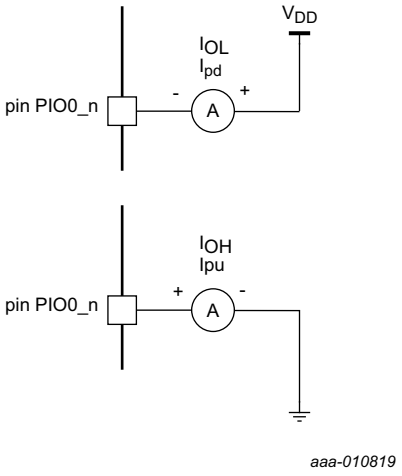
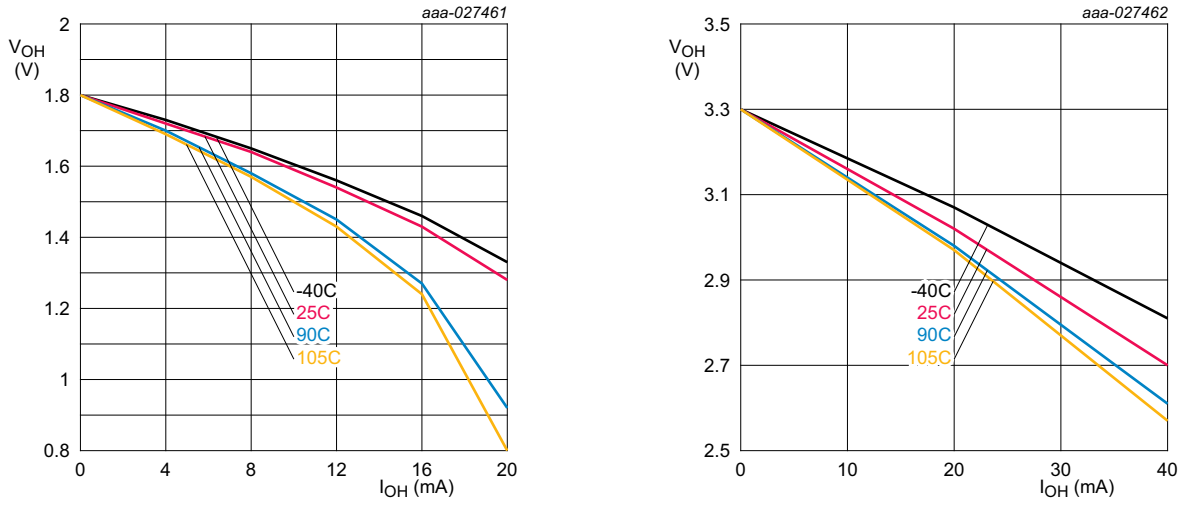


Fig 22. Pin input/output current measurement

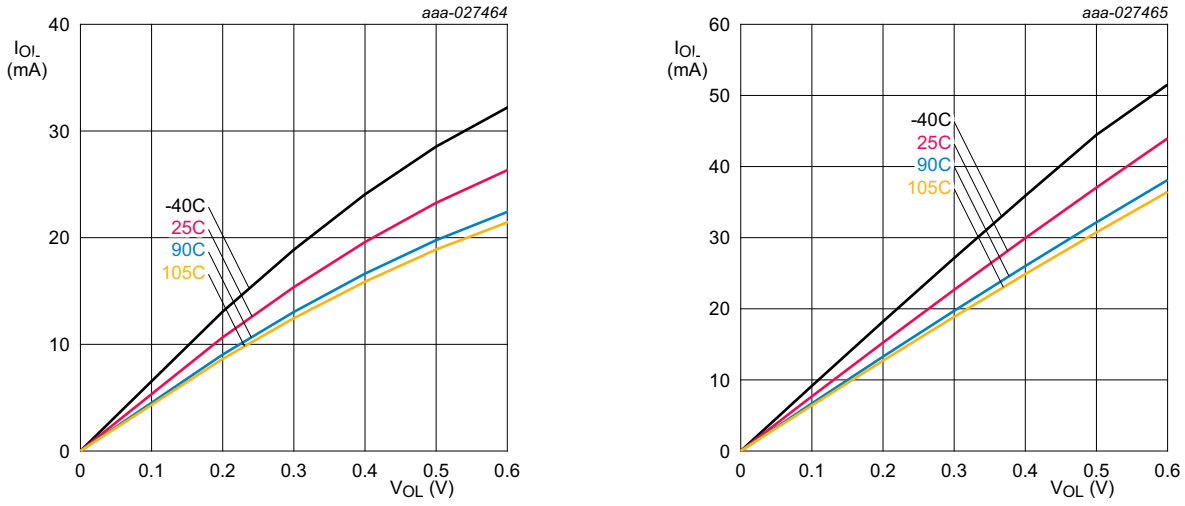
11.5.1 Electrical pin characteristics



Conditions: V_{DD} = 1.8 V; on pin PIO0_12.

Conditions: V_{DD} = 3.3 V; on pin PIO0_12.

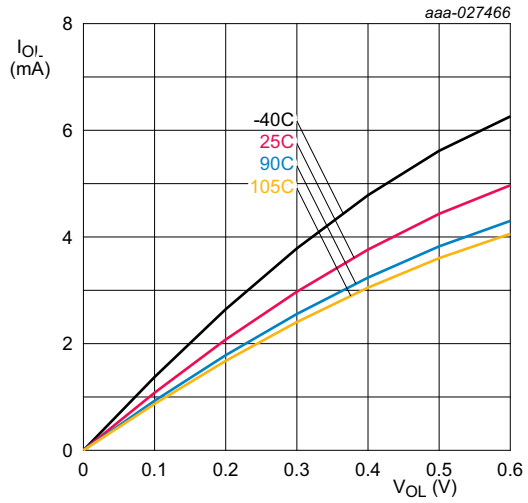
Fig 23. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



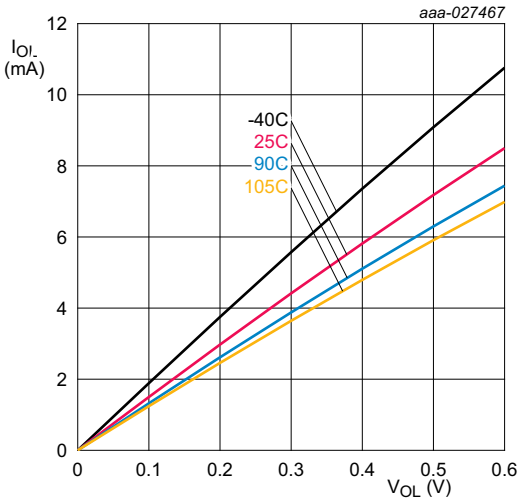
Conditions: V_{DD} = 1.8 V; on pins PIO0_10 and PIO0_11.

Conditions: V_{DD} = 3.3 V; on pins PIO0_10 and PIO0_11.

Fig 24. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

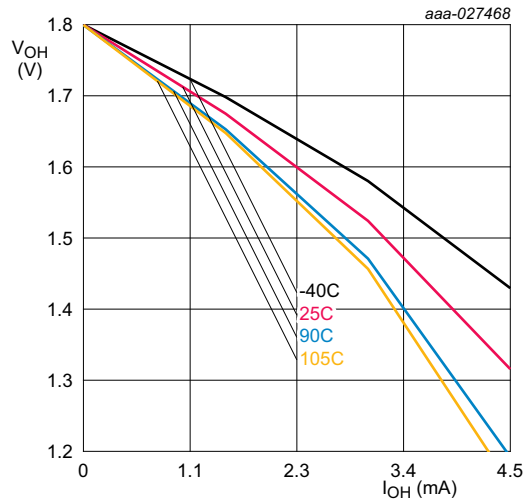


Conditions: V_{DD} = 1.8 V; standard port pins and high-drive pin PIO0_12.

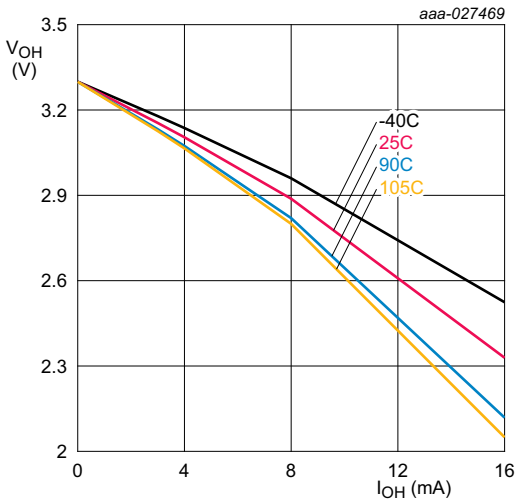


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pin PIO0_12.

Fig 25. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

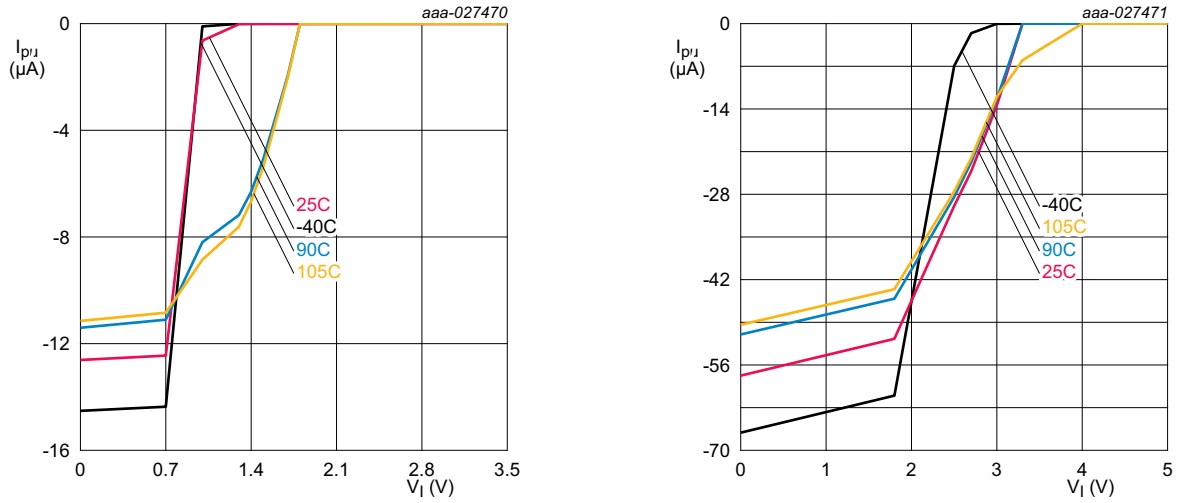


Conditions: V_{DD} = 1.8 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

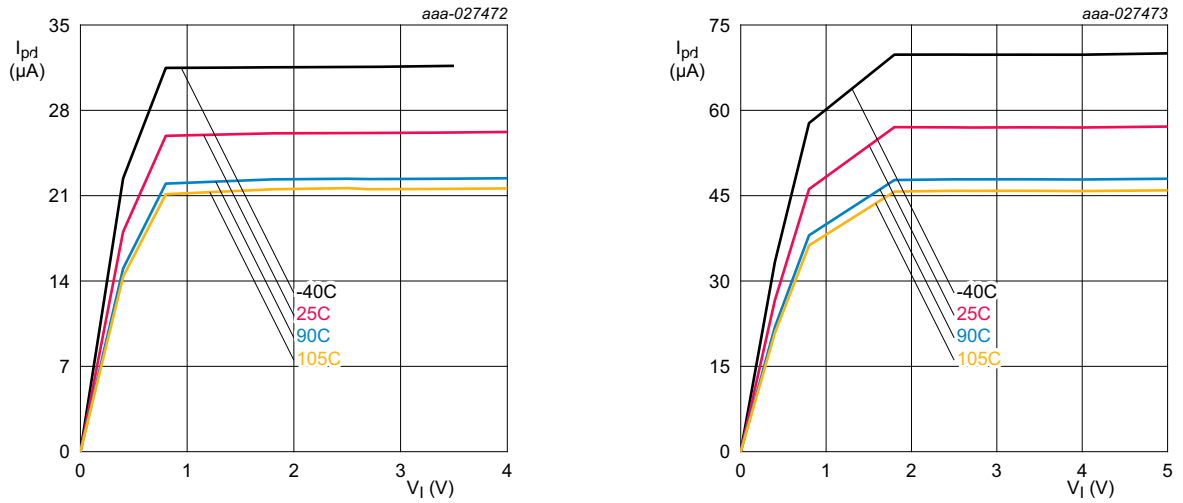
Fig 26. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 27. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8 V; standard port pins.

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical pull-down current I_{PD} versus input voltage V_I

12. Dynamic characteristics

12.1 Flash memory

Table 16. Flash characteristics

T_{amb} = −40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	20	-	years
		not powered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 64 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC84x user manual*).

12.2 FRO

Table 17. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Min	Typ[1]	Max	Unit
FRO clock frequency; Condition: 0 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	18 -1 %	18	18 +1 %	MHz
$f_{osc(RC)}$	24 -1 %	24	24 +1 %	MHz
$f_{osc(RC)}$	30 -1 %	30	30 +1 %	MHz
FRO clock frequency; Condition: −20 °C ≤ T_{amb} ≤ 70 °C				
$f_{osc(RC)}$	18 -2 %	18	18 +1 %	MHz
$f_{osc(RC)}$	24 -2 %	24	24 +1 %	MHz
$f_{osc(RC)}$	30 -2 %	30	30 +1 %	MHz
FRO clock frequency; Condition: −40 °C ≤ T_{amb} ≤ 105 °C				
$f_{osc(RC)}$	18 -3.5 %	18	18 +2.5 %	MHz
$f_{osc(RC)}$	24 -3.5 %	24	24 +2.5 %	MHz
$f_{osc(RC)}$	30 -3.5 %	30	30 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Table 18. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the LPC84x *user manual.*

12.3 I/O pins

Table 19. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.4 WKTCLKIN pin (wake-up clock input)

Table 20. Dynamic characteristics: WKTCLKIN pin

T_{amb} = −40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Max	Unit
f_{clk}	clock frequency	deep power-down mode and power-down mode	[1]	-	1	MHz
		deep-sleep, sleep, and active mode	[1]	-	10	MHz
t_{CHCX}	clock HIGH time	-		50	-	ns
t_{CLCX}	clock LOW time	-		50	-	ns

[1] Assuming a square-wave input clock.

12.5 SCTimer/PWM output timing

Table 21. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated skew (over process, voltage, and temperature) of any two SCT output signals routed to standard I/O pins; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	6	ns

12.6 I²C-bus

Table 22. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; values guaranteed by design.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

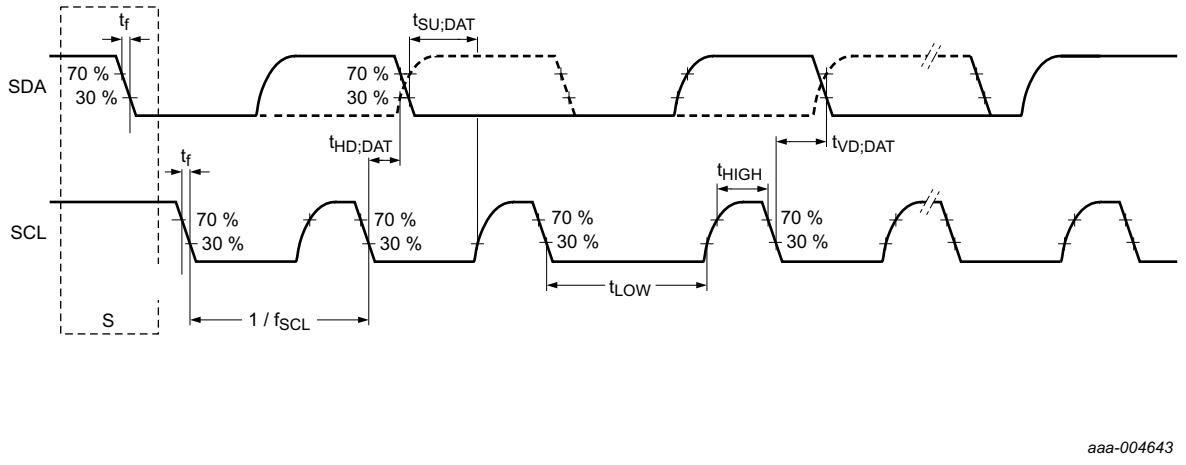


Fig 29. I^2C-bus pins clock timing

12.7 SPI interfaces

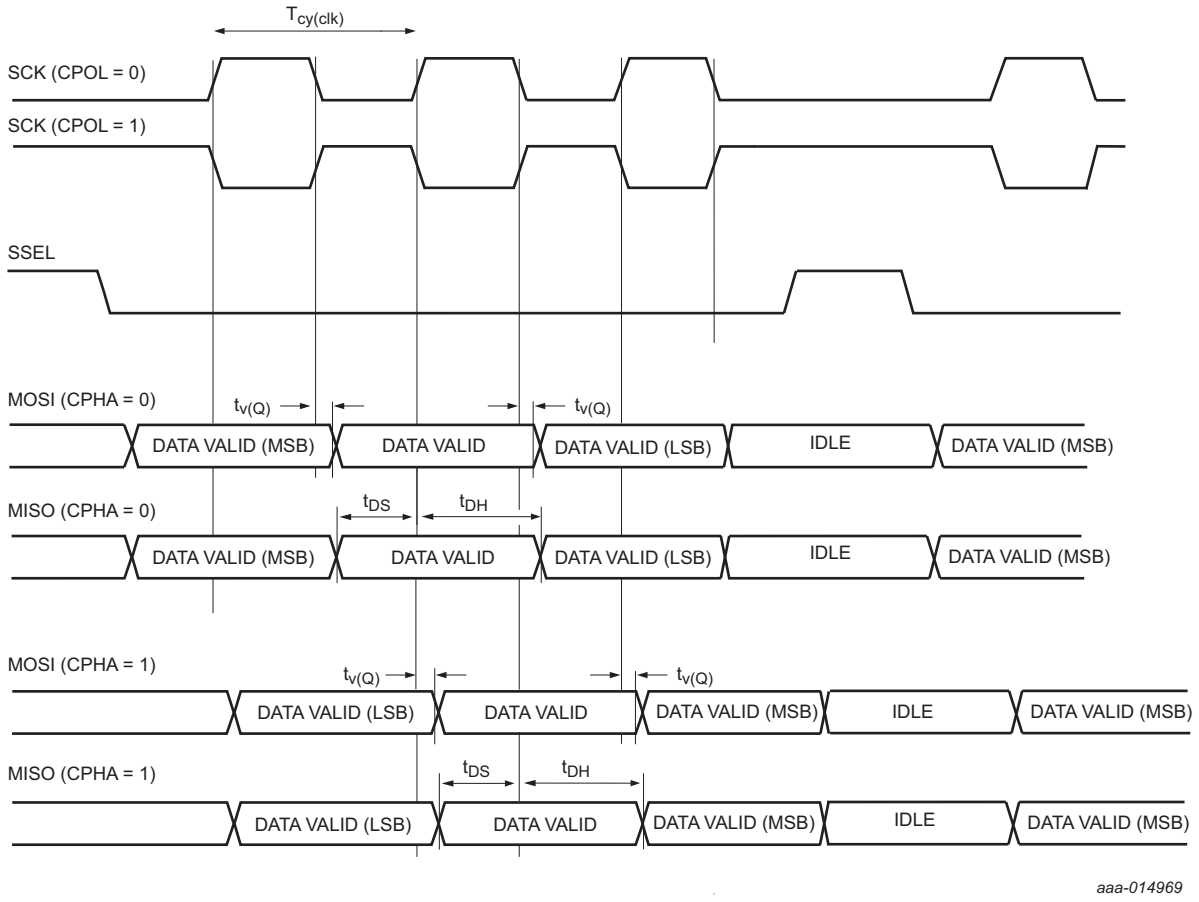
The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 30 Mbit/s, and the maximum supported bit rate for SPI slave mode is 1/(2 x 26 ns) = 19 Mbit/s at 3.0v ≤ VDD ≤ 3.6v and 1/(2 x 42 ns) = 12 Mbit/s at 1.8v ≤ VDD < 3.0v.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 23. SPI dynamic characteristics

T_{amb} = −40 °C to 105 °C; C_L = 20 pF; input slew = 1 ns. Simulated parameters sampled at the 30 % and 70 % level of the rising or falling edge; values guaranteed by design. Delays introduced by the external trace or external device are not considered.

Symbol	Parameter	Conditions	Min	Max	Unit
SPI master					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	3	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	0	-	ns
$t_{v(Q)}$	data output valid time	1.8 V <= V_{DD} <= 3.6 V	0	5	ns
SPI slave					
t_{DS}	data set-up time	1.8 V <= V_{DD} <= 3.6 V	4	-	ns
t_{DH}	data hold time	1.8 V <= V_{DD} <= 3.6 V	1	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	26	ns
		1.8 V <= V_{DD} < 3.0 V	0	42	ns



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the LPC84x *User manual*.

Fig 30. SPI master timing

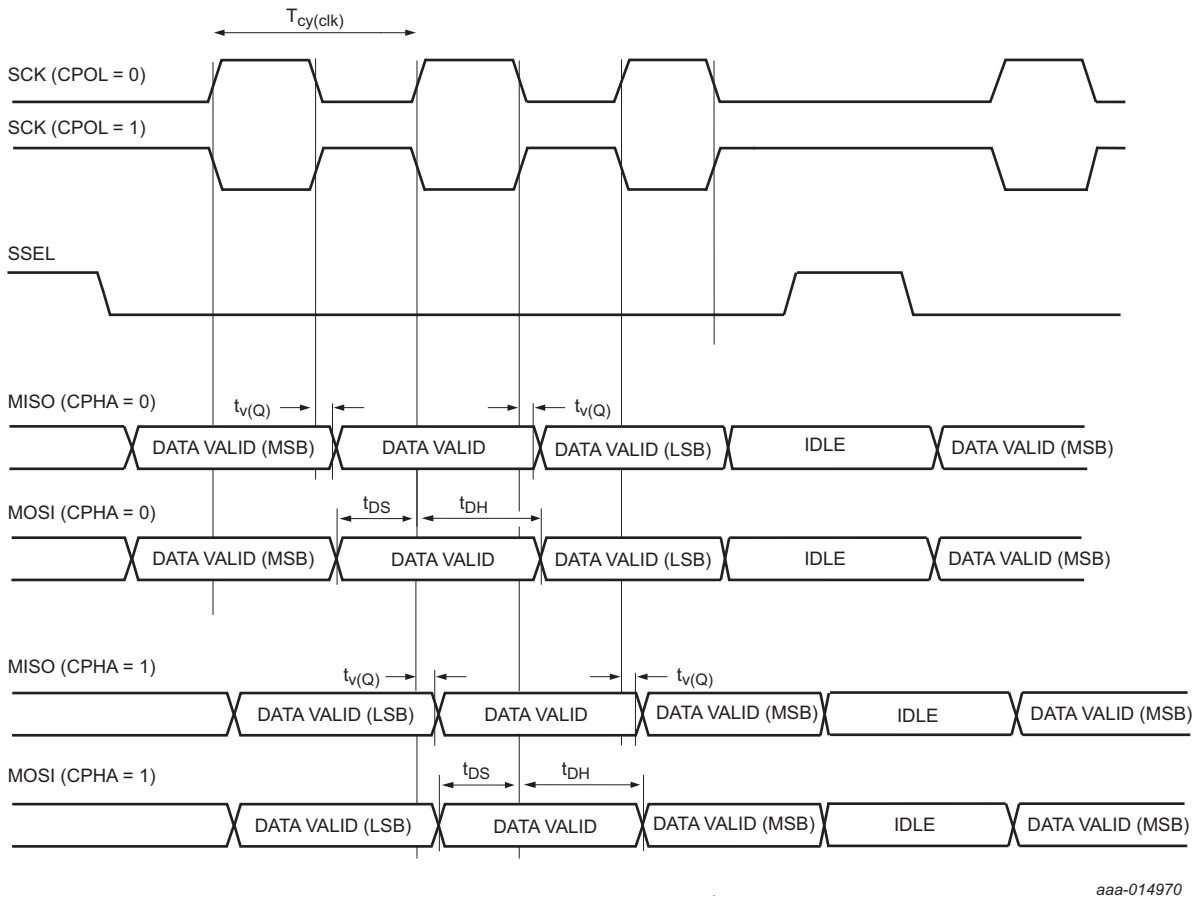


Fig 31. SPI slave timing

12.8 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 10 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 10 Mbit/s.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 24. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.8 V <= V_{DD} <= 3.6 V unless noted otherwise; C_L = 10 pF; input slew = 10 ns. Simulated parameters sampled at the 30 %/70 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time	3.0 V <= V_{DD} <= 3.6 V	31	-	ns
		1.8 V <= V_{DD} < 3.0 V	42		
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		0	7	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		5	-	ns
$t_{v(Q)}$	data output valid time	3.0 V <= V_{DD} <= 3.6 V	0	35	ns
		1.8 V <= V_{DD} < 3.0 V	0	46	ns

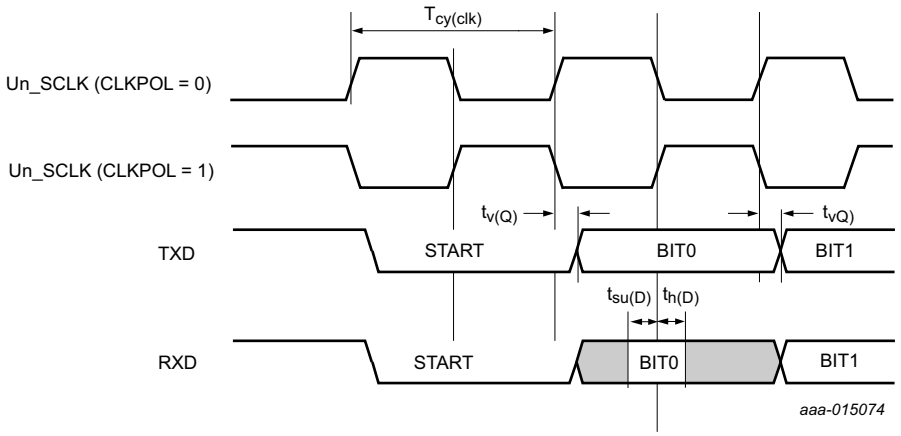


Fig 32. USART timing

12.9 Wake-up process

Table 25. Dynamic characteristic: Typical wake-up times from low power modes

V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO (12MHz) as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	2.4	-	µs
		from deep-sleep mode	[2]	-	2.5	-	µs
		from power-down mode	[2]	-	50	-	µs
		from deep power-down mode; WKT disabled; using $\overline{\text{RESET}}$ pin.	[4]	-	250	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler. ISR is located in SRAM.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] WKT disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

13. Characteristics of analog peripherals

13.1 BOD

Table 26. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1					
		assertion		-	2.25	-	V
		de-assertion		-	2.38	-	V
		interrupt level 2					
		assertion		-	2.55	-	V
		de-assertion		-	2.66	-	V
		interrupt level 3					
		assertion		-	2.84	-	V
		de-assertion		-	2.92	-	V
		reset level 0					
		assertion		-	1.84	-	V
		de-assertion		-	1.97	-	V
		reset level 1					
		assertion		-	2.05	-	V
		de-assertion		-	2.18	-	V
		reset level 2					
		assertion		-	2.35	-	V
		de-assertion		-	2.47	-	V
		reset level 3					
		assertion		-	2.63	-	V
		de-assertion		-	2.76	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *the* LPC84x *user manual*. Interrupt level 0 is reserved.

13.2 ADC

Table 27. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = V_{DDA} = 2.4 V to 3.6 V; VREFP = V_{DD} = V_{DDA}; VREFN = V_{SS}.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
V_{ref}	reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	26	pF
$f_{clk(ADC)}$	ADC clock frequency		[2]	-	-	30	MHz
f_s	sampling frequency		[2]	-	-	1.2	Msamples/s
E_D	differential linearity error		[5][4]	-	±3.0	-	LSB
$E_{L(adj)}$	integral non-linearity		[6][4]	-	±2.0	-	LSB
E_O	offset error		[7][4]	-	±3.5	-	LSB
$V_{err(fs)}$	full-scale error voltage		[8][4]	-	0.1	-	%
Z_i	input impedance	f_s = 1.2 Msamples/s	[1][9][10]	0.1	-	-	MΩ

[1] The input resistance of ADC channel 0 is higher than for all other channels. See Figure 33.

[2] In the ADC TRM register, set VRANGE = 0 (default).

[3] In the ADC TRM register, set VRANGE = 1.

[4] Based on characterization. Not tested in production.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 34.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 34.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 34.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 34.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 1.2 Msamples/s and analog input capacitance C_{ia} = 26 pF.

[10] Input impedance Z_i (See Section 13.2.1 “ADC input impedance”) is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 13 for C_{io}.

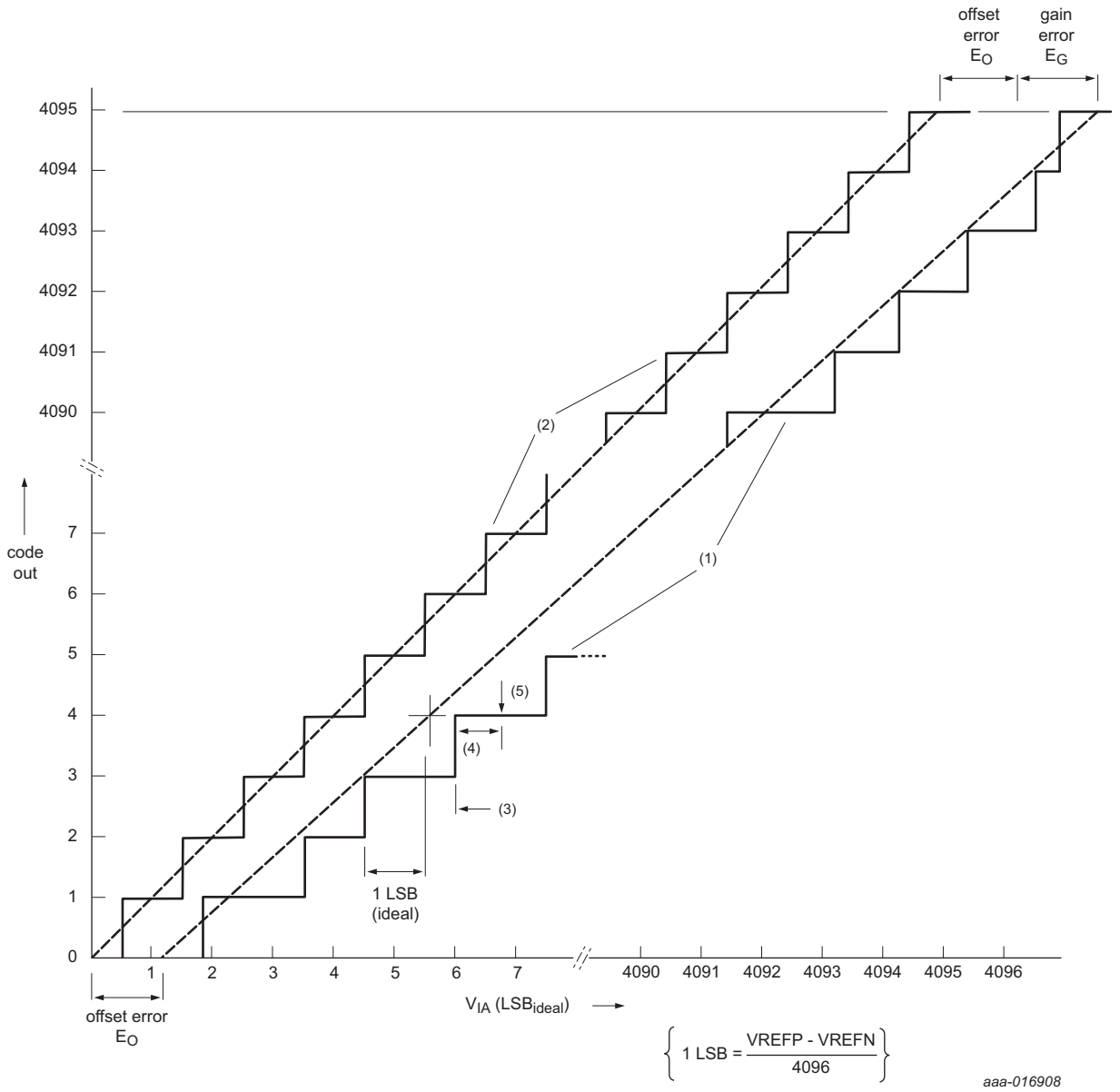


Fig 33. 12-bit ADC characteristics

13.2.1 ADC input impedance

Figure 34 shows the ADC input impedance. In this figure:

- ADCx represents ADC input channel 0.
- ADCy represents ADC input channels 1 to 11.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If ADC input channel 0 is selected, the ADC input signal goes through $R_1 + R_{sw}$ to the sampling capacitor (C_{ia}).
- If ADC input channels 1 to 11 are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 2.5 kΩ, R_{sw} = 25 Ω
- See Table 11 for C_{io}.
- See Table 27 for C_{ia}.

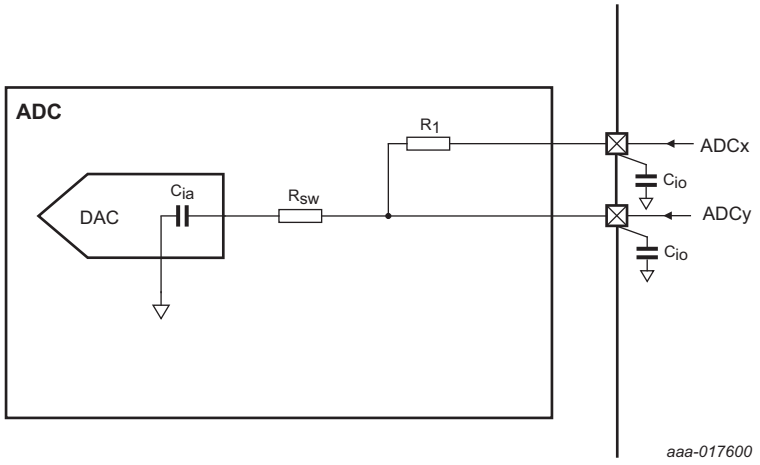


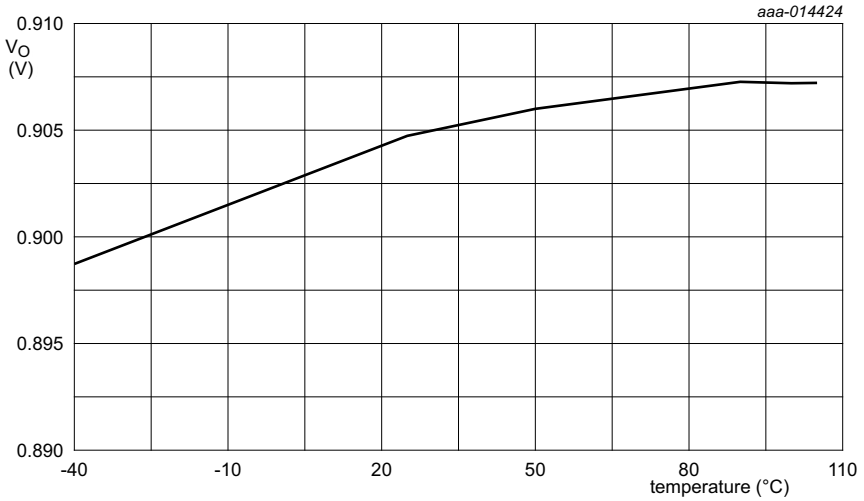
Fig 34. ADC input impedance

13.3 Comparator and internal voltage reference

Table 28. Internal voltage reference static and dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 3.3 V; hysteresis disabled in the comparator CTRL register.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage	T_{amb} = 25 °C to 105°C		860	-	940	mV
		T_{amb} = 25 °C			904		mV



V_{DD} = 3.3 V; characterized through bench measurements on typical samples.

Fig 35. Typical internal voltage reference output voltage

Table 29. Comparator characteristics

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{ref(cmp)}$	comparator reference voltage	pin $ACMPV_{REF}$		1.5	-	3.6	V
I_{DD}	supply current	VP > VM; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	90	-	µA
		VM > VP; T_{amb} = 25 °C; V_{DD} = 3.3 V	[2]	-	60	-	µA
V_{IC}	common-mode input voltage			0	-	V_{DD}	V
DV_O	output voltage variation			0	-	V_{DD}	V
V_{offset}	offset voltage	V_{IC} = 0.1 V; V_{DD} = 3.0 V	[2]	-	3	-	mV
		V_{IC} = 1.5 V; V_{DD} = 3.0 V	[2]	-	3	-	mV
		V_{IC} = 2.9 V; V_{DD} = 3.0V	[2]	-	6	-	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; V_{DD} = 3.3 V; T_{amb} = 25 °C		-	13	-	µs

Table 29. Comparator characteristics *...continued*

T_{amb} = −40 °C to +105 °C unless noted otherwise; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	HIGH to LOW; V_{DD} = 3.0 V; T_{amb} = 105 °C			150		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	250	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	150	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	170	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	180	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	70	-	ns
t_{PD}	propagation delay	LOW to HIGH; V_{DD} = 3.0 V; T_{amb} = 105 °C			260		
		V_{IC} = 0.1 V; 100 mV overdrive input	[1][2][4]	-		-	ns
		V_{IC} = 0.1 V; rail-to-rail input	[1][2]	-	90	-	ns
		V_{IC} = 1.5 V; 100 mV overdrive input	[1][2][4]	-	270	-	ns
		V_{IC} = 1.5 V; rail-to-rail input	[1][2]	-	220	-	ns
		V_{IC} = 2.9 V; 100 mV overdrive input	[1][2][4]	-	190	-	ns
		V_{IC} = 2.9 V; rail-to-rail input	[1][2]	-	700	-	ns
V_{hys}	hysteresis voltage	positive hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[3]	-	6	-	
		5 mV					mV
		10 mV		-	12	-	mV
		20 mV		-	22	-	mV
V_{hys}	hysteresis voltage	negative hysteresis; V_{DD} = 3.0 V; V_{IC} = 1.5 V; T_{amb} = 105 °C; settings:	[1][3]		7		
		5 mV		-		-	mV
		10 mV		-	13	-	mV
		20 mV		-	23	-	mV
R_{lad}	ladder resistance	-		-	1	-	MΩ

[1] C_L = 10 pF

[2] Characterized on typical samples, not tested in production.

[3] Input hysteresis is relative to the reference input channel and is software programmable.

[4] 100 mV overdrive corresponds to a square wave from 50 mV below the reference (V_{IC}) to 50 mV above the reference.

Table 30. Comparator voltage ladder dynamic characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	17	-	µs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1]	-	18	-	µs

[1] Characterized on typical samples, not tested in production.

Table 31. Comparator voltage ladder reference static characteristics

V_{DD} = 1.8 V to 3.6 V. T_{amb} = -40 °C to + 105 °C; external or internal reference.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$E_{V(O)}$	output voltage error	decimal code = 00	[2]	-	±6	-	mV
		decimal code = 08		-	±1	-	%
		decimal code = 16		-	±1	-	%
		decimal code = 24		-	±1	-	%
		decimal code = 30		-	±1	-	%
		decimal code = 31		-	±1	-	%

[1] Characterized though limited samples. Not tested in production.

[2] All peripherals except comparator, temperature sensor, and FRO turned off.

13.4 DAC

Table 32. 10-bit DAC electrical characteristics

V_{DD} = V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +105 °C unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
E_D	differential linearity error	[1][2]	-	0.4	-	LSB
$E_{L(adj)}$	integral non-linearity	[1][2]	-	6.0	-	LSB
E_O	offset error	[1][2]	-	±57.0	-	mV
E_G	gain error	[1][2]	-	±36.0	-	mV
C_L	load capacitance		-	200	-	pF
R_{OUT}	PIO0_17/DACOUT_0 pin resistance	[3]	-	90	200	Ω
R_{OUT}	PIO0_29/DACOUT_1 pin resistance	[3]	-	2	5	kΩ
V_{OUT}	Output voltage range		0.175	-	V_{DDA}-0.175	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C) and V_{DD} = V_{DDA} = 3.6 V.

[2] Characterized through bench measurements, not tested in production.

[3] DAC output voltage depends on the voltage divider ratio of the R_{OUT} and external load resistance.

14. Application information

14.1 Start-up behavior

Figure 36 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

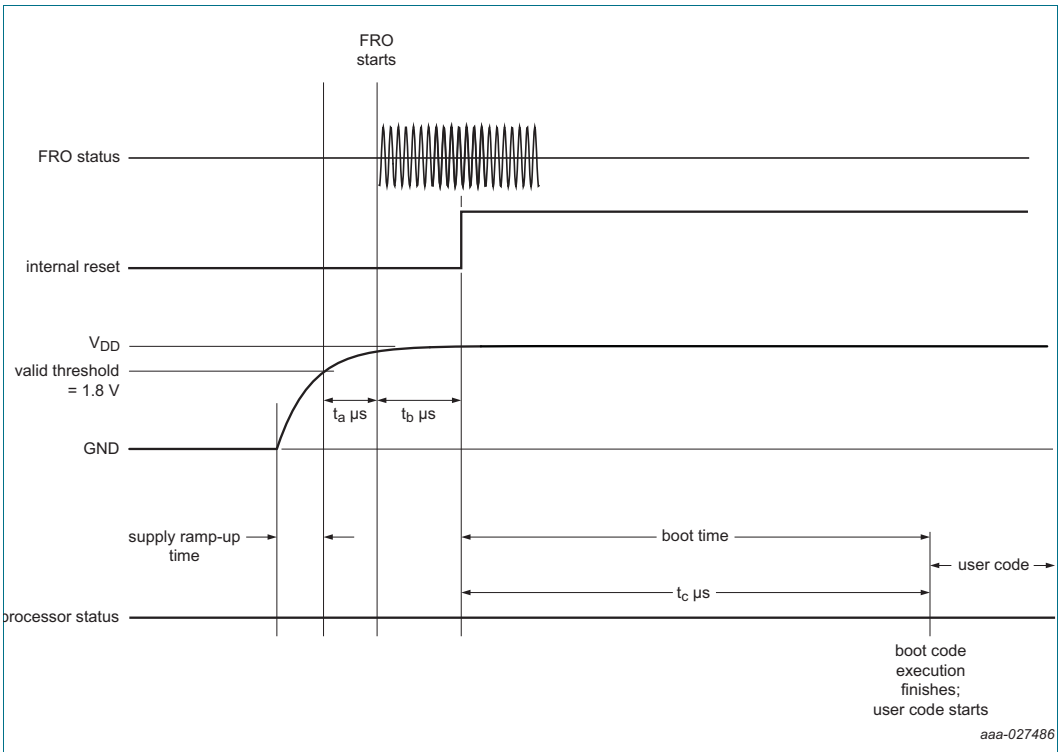


Fig 36. Start-up timing

Table 33. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 26 µs
t_b	Internal reset de-asserted	101 µs
t_c	Boot time	51 µs

14.2 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 37.

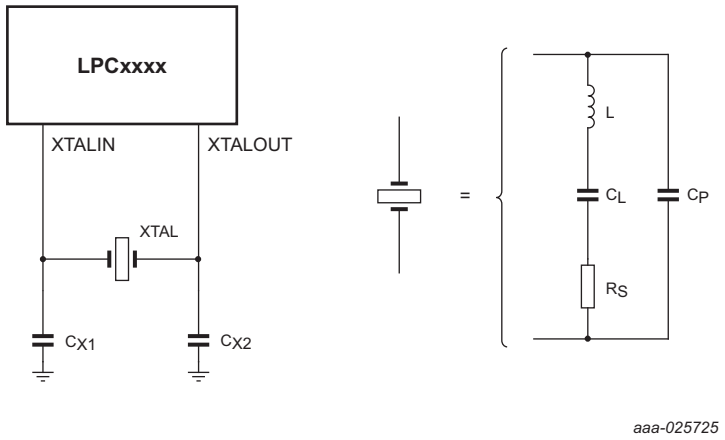


Fig 37. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

14.2.1 XTAL Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

14.2.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.95 V. If the oscillator is driven by a clock in slave mode, it is recommended to couple the input through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

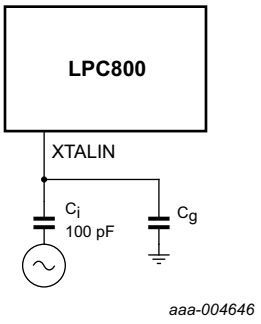
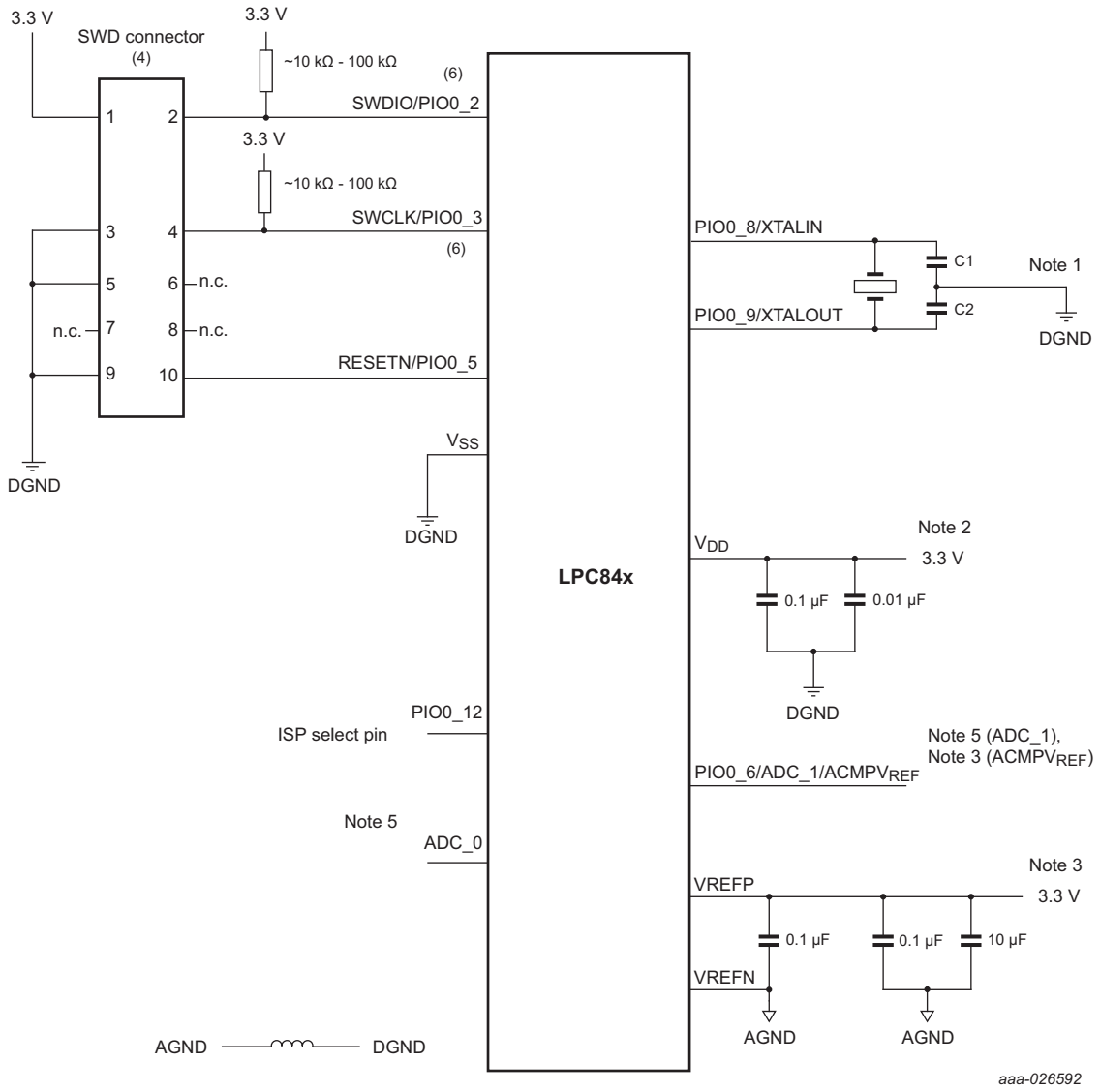


Fig 38. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled with a capacitor of 100 pF (Figure 38), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

14.3 Connecting power, clocks, and debug functions

Figure 39 shows the basic board connections used to power the LPC84x, connect the external crystal, and provide debug capabilities via the serial wire port.



(1) See Section 14.2 “XTAL oscillator” for the values of C1 and C2.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DD} pins. The 10 µF bypass capacitor filters the power line. Tie VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the Arm 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 4.

(6) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default.

Fig 39. Power, clock, and debug connections

14.4 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 15 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 15, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 15 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

14.5 Termination of unused pins

Table 34 shows how to terminate pins that are **not** used in the application. In many cases, unused pins may should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 34. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_5	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

14.6 Pin states in different power modes

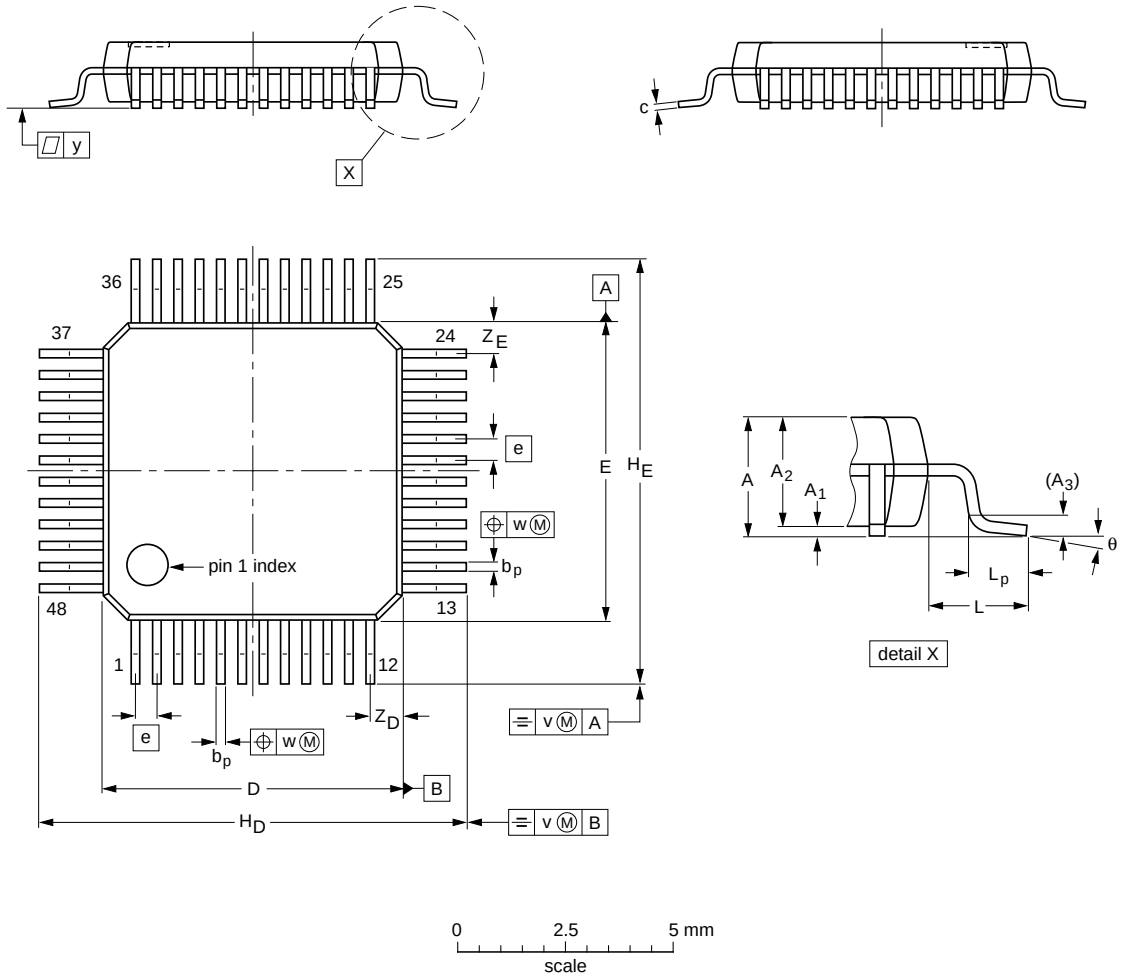
Table 35. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
Open-drain I2C-bus pins	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
$\overline{\text{WAKEUP}}$	As configured in the IOCON[1]. $\overline{\text{WAKEUP}}$ function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

15. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

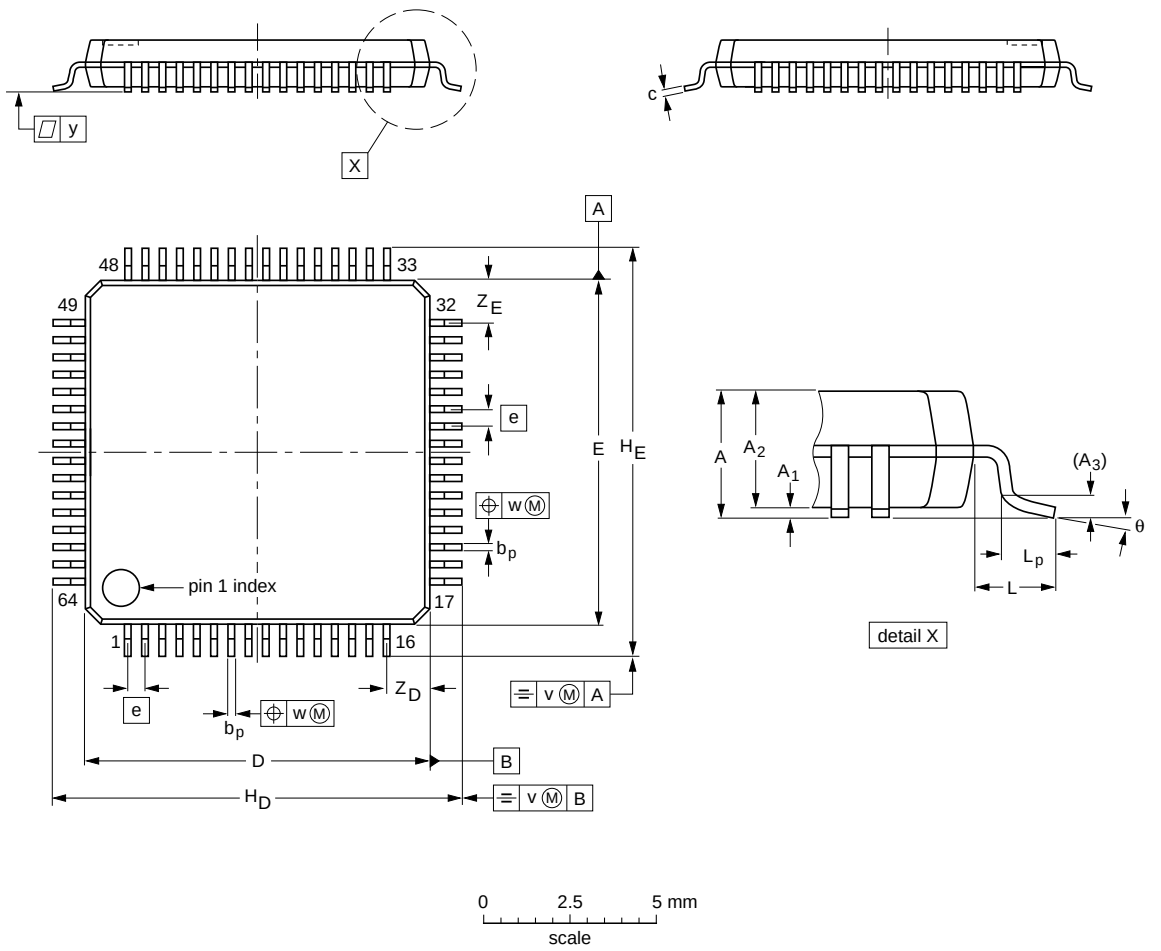
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 40. Package outline SOT313-2 (LQFP48)

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

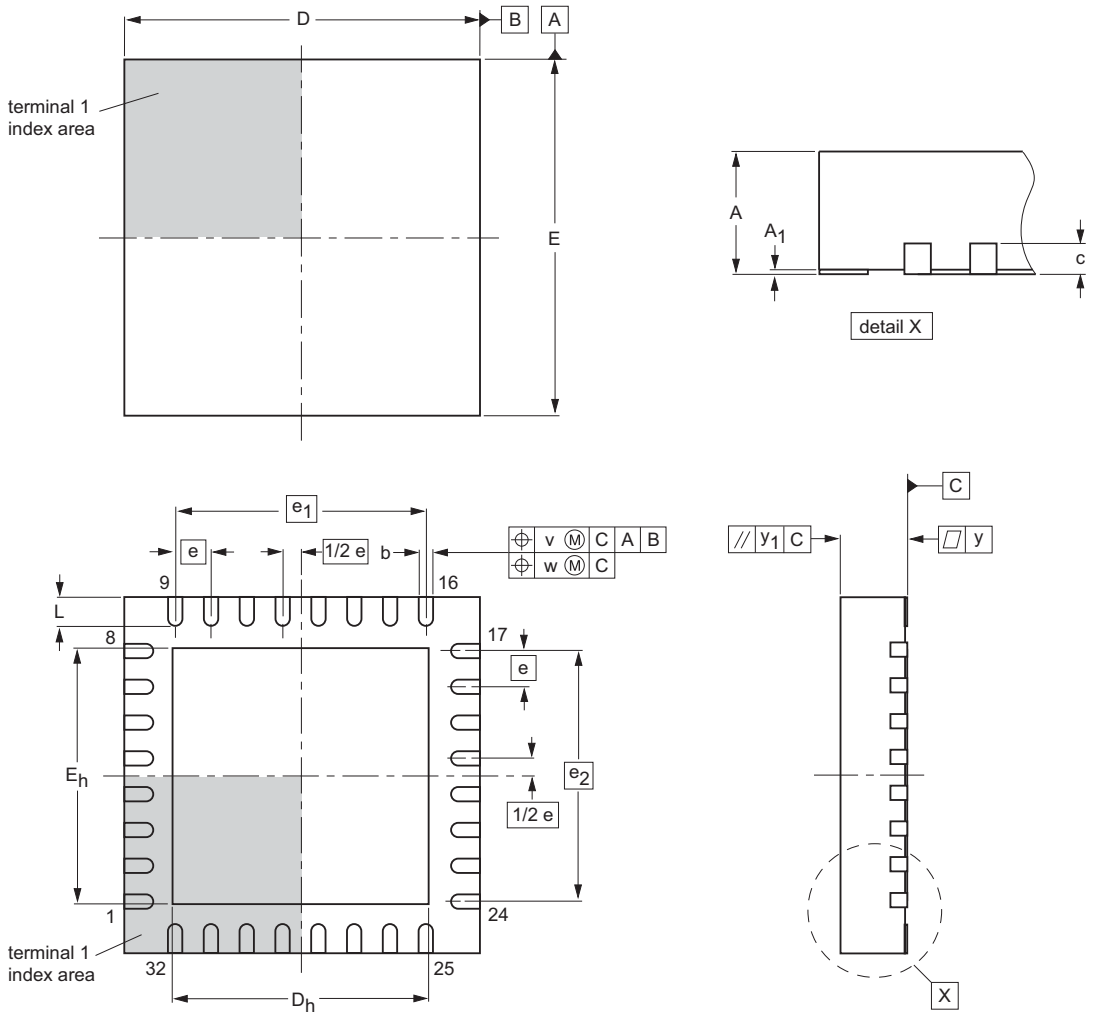
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 41. Package outline SOT314-2 (LQFP64)

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	A_1	b	c	D[1]	D_h	E[1]	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max		0.05	0.30		5.1	3.75	5.1	3.75				0.5				
	nom	0.85			0.2					0.5	3.5	3.5		0.1	0.05	0.05	0.1
	min		0.00	0.18		4.9	3.45	4.9	3.45				0.3				

Note

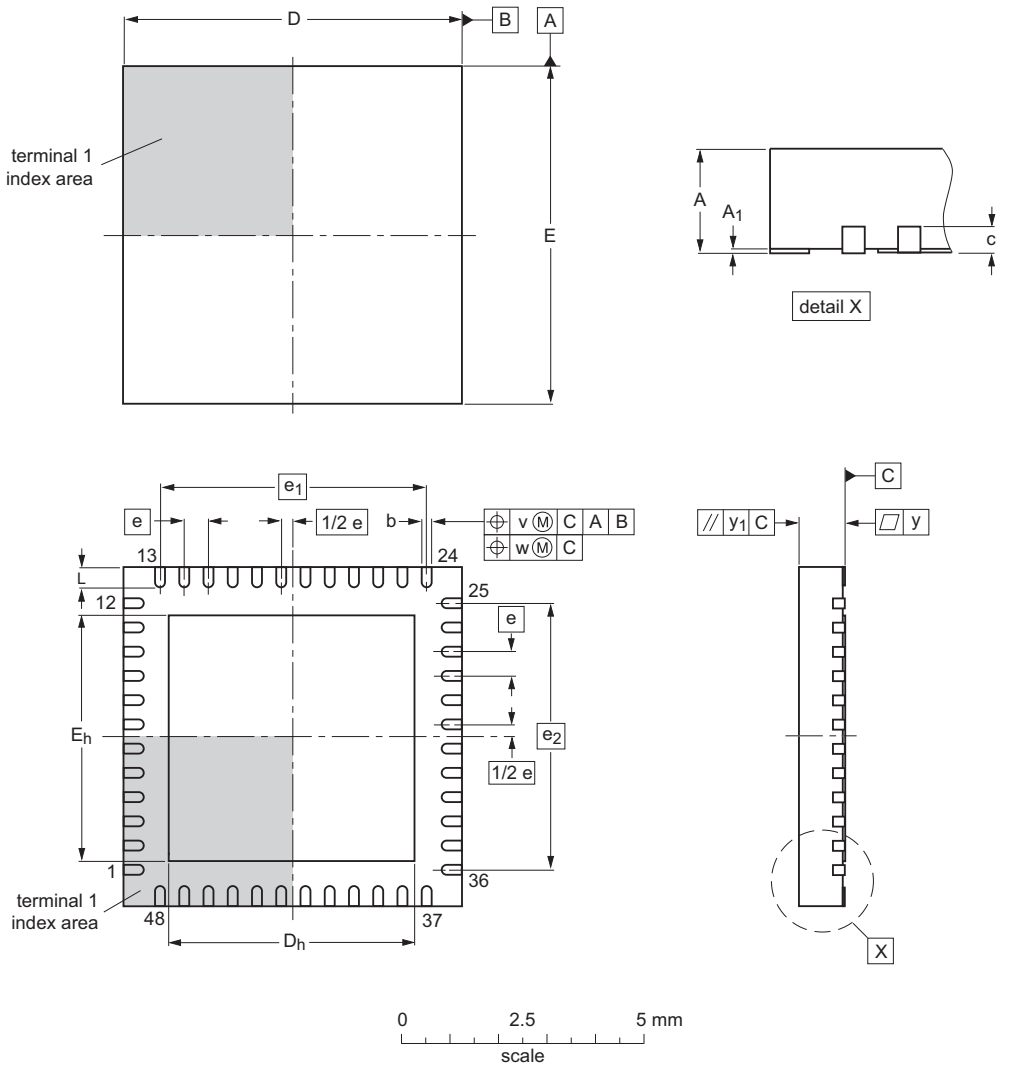
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

hvqfn33f_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		MO-220				~~11-10-11~~ 11-10-17

Fig 42. Package outline HVQFN33 (5 x 5 x 0.85 mm)

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	b	C	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.30		7.1	5.25	7.1	5.25				0.5				
	nom	0.85	0.02	0.21	0.2	7.0	5.10	7.0	5.10	0.5	5.5	5.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		6.9	4.95	6.9	4.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

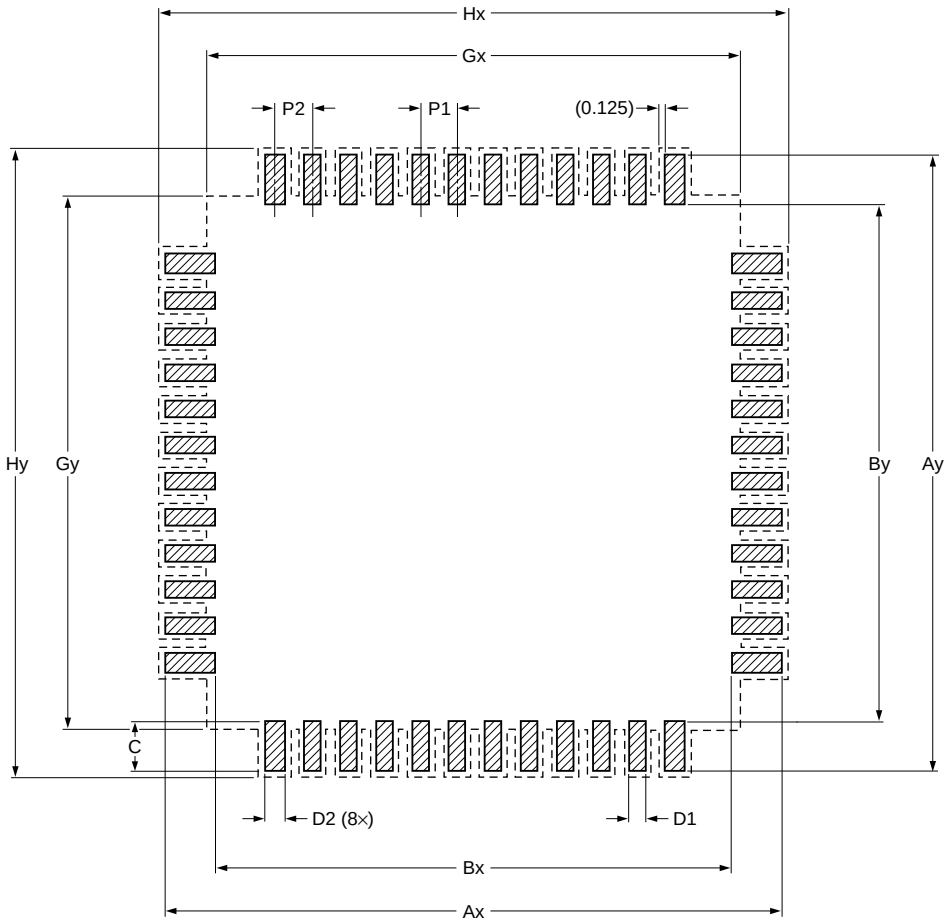
sot619-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT619-1		MO-220				~~02-10-18~~ 12-11-22

Fig 43. Package outline HVQFN48 7 x 7x 0.85 mm (SOT619-1)

16. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

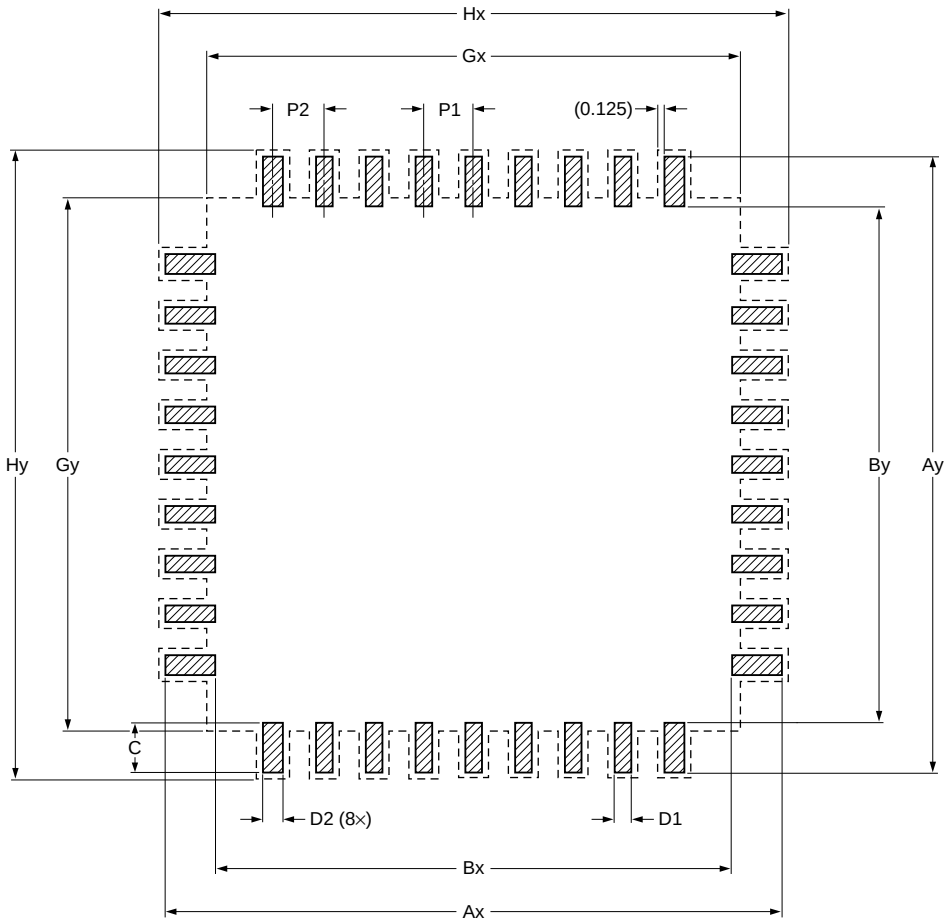
DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 44. Reflow soldering for the LQFP48 package

Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

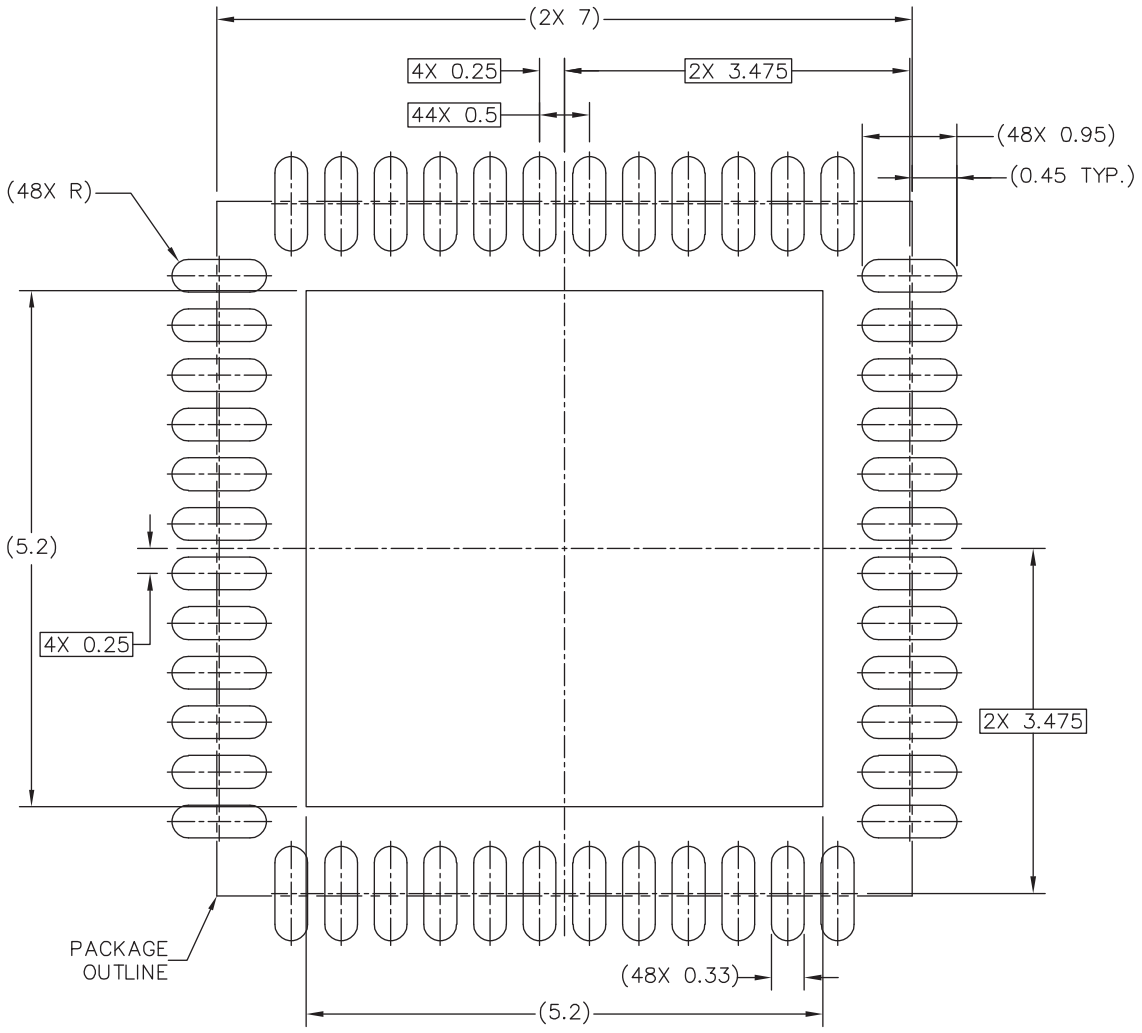
occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

sot314-2_fr

Fig 45. Reflow soldering for the LQFP64 package



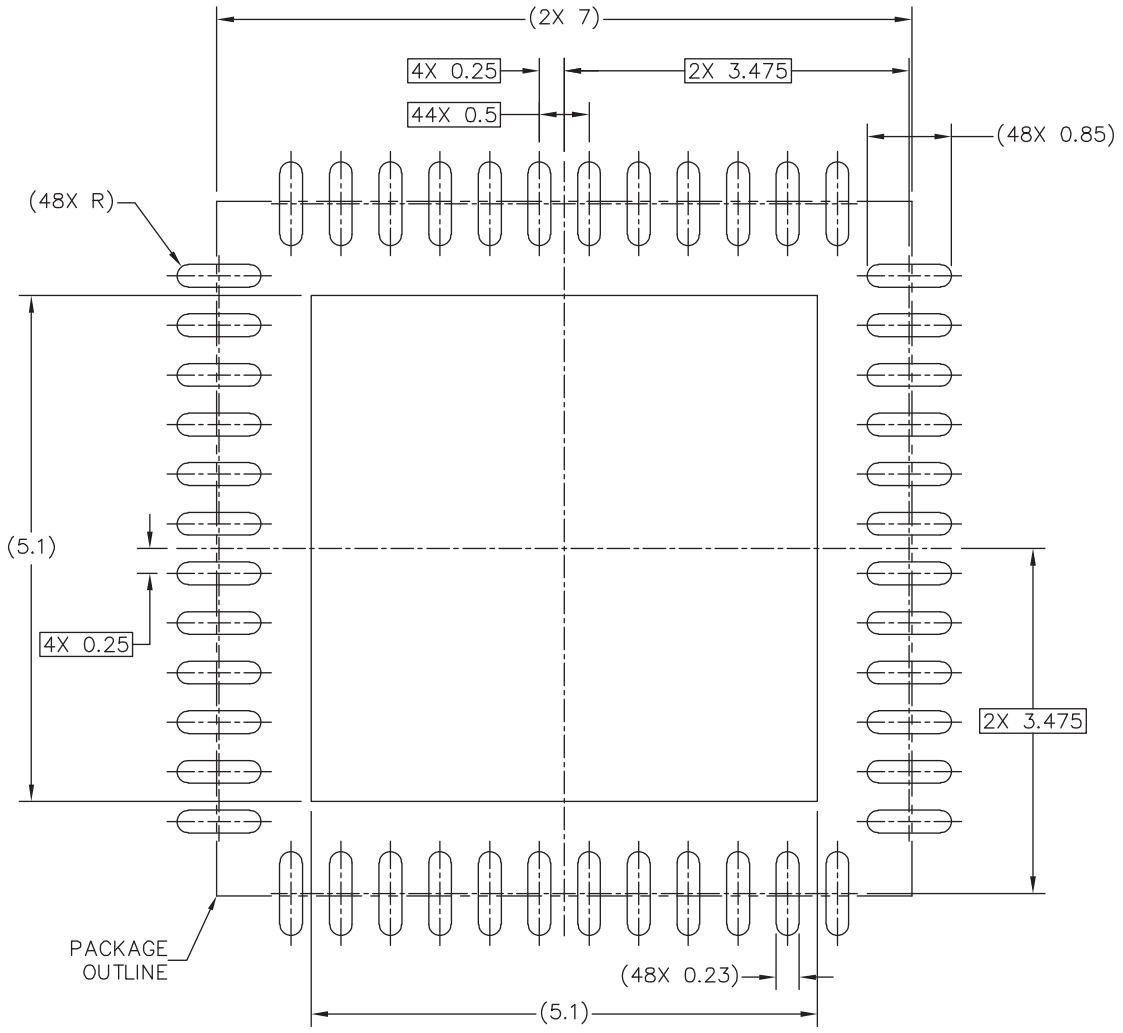
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–1	REVISION: 0	

Fig 46. Reflow soldering of the HVQFN48 package (7x7) 1 of 3



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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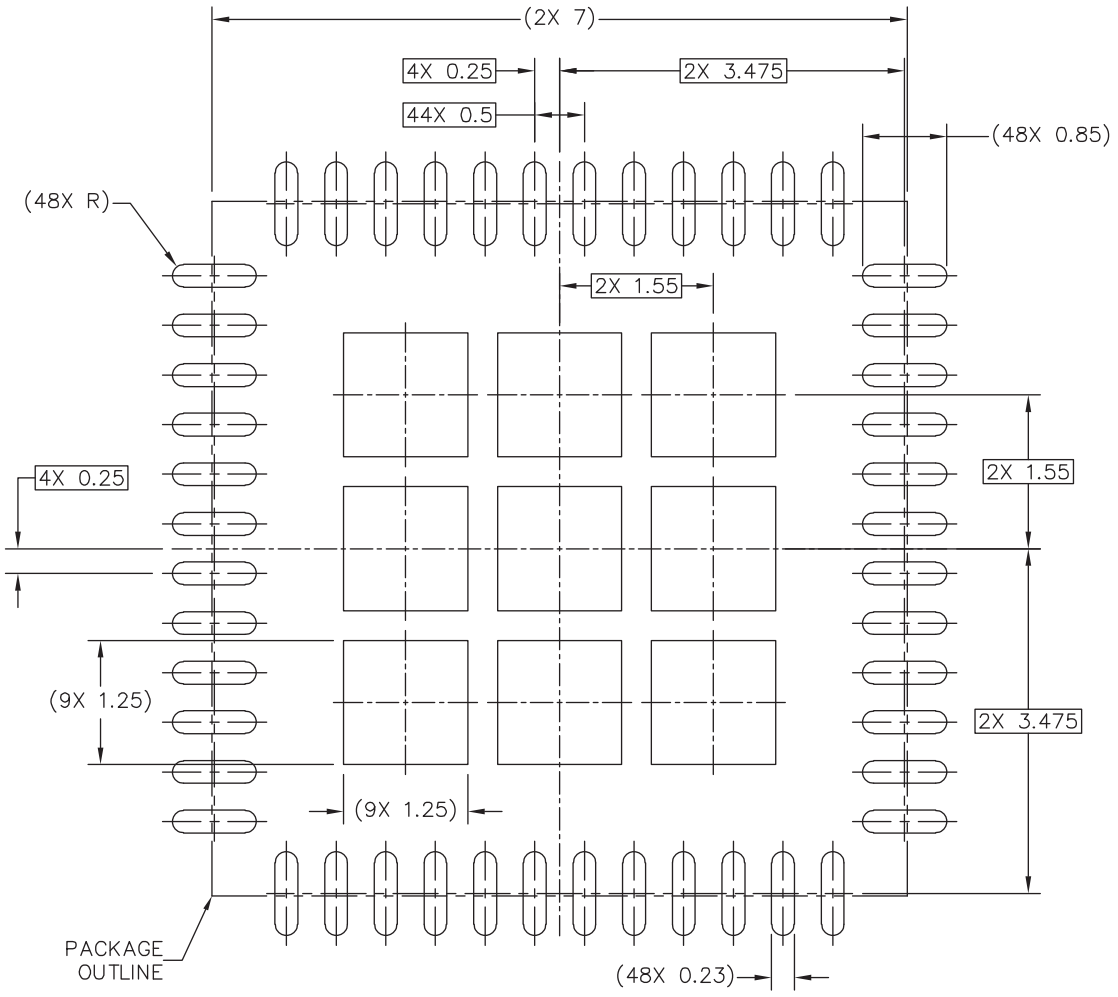
 DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619–1	REVISION: 0	

Fig 47. Reflow soldering of the HVQFN48 package (7x7) 2 of 3



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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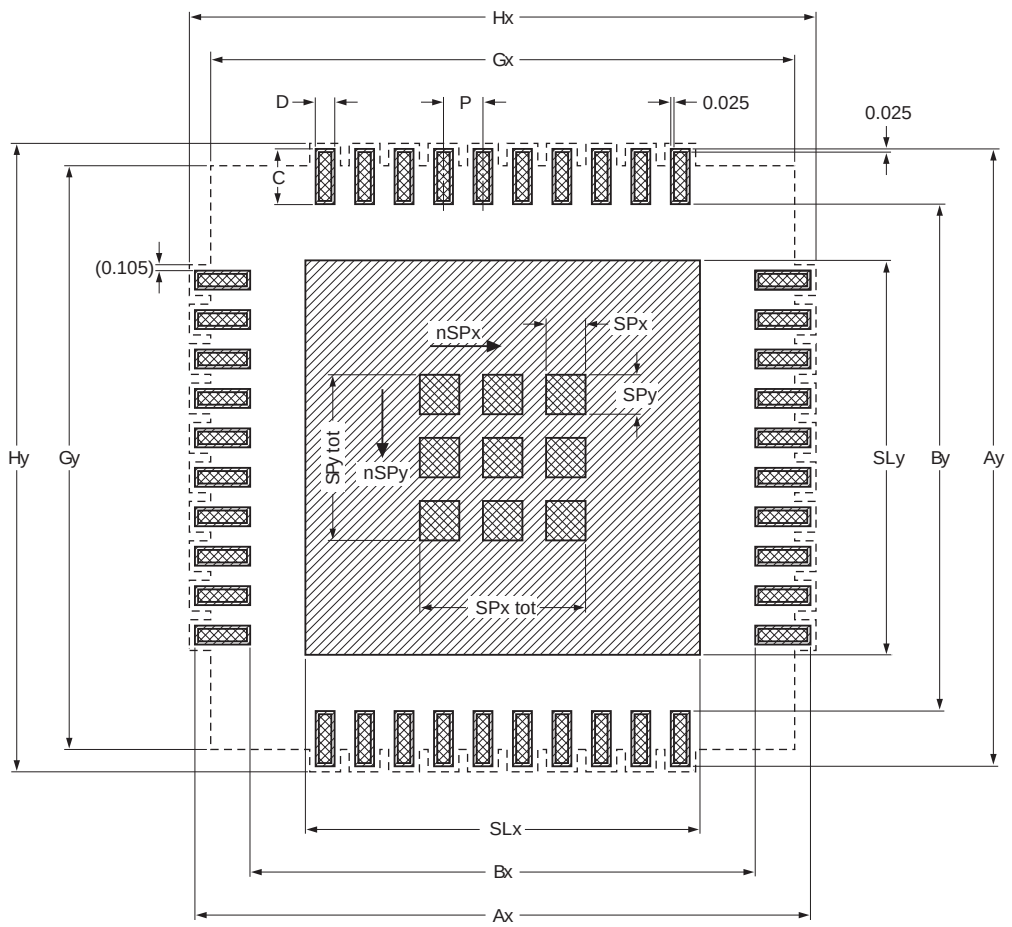
DATE: 13 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT619-1	REVISION: 0	

Fig 48. Reflow soldering of the HVQFN48 package (7x7) 3 of 3

Footprint information for reflow soldering of HVQFN48 package SOT619-1



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
3	3

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	8.000	8.000	6.200	6.200	0.900	0.290	5.100	5.100	3.000	3.000	0.750	0.750	7.300	7.300	8.250	8.250

Issue date ~~07-05-07~~ 09-06-15

sot619-1_fr

Fig 49. Reflow soldering of the HVQFN48 package (7x7)

17. Abbreviations

Table 36. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] LPC84x User manual UM11029:

[2] LPC84x Errata sheet:

[3] I2C-bus specification *UM10204*.

[4] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

19. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC84X v.1.7	20180227	Product data sheet	-	LPC84X v.1.6
Modifications:	• Updated Table 17 “Dynamic characteristic: FRO”: Max values: FRO clock frequency; Condition: –20 °C ≤ T_{amb} ≤ 70 °C and FRO clock frequency; Condition: –40 °C ≤ T_{amb} ≤ 105 °C.			
LPC84X v.1.6	20180216	Product data sheet	-	LPC84X v.1.5
Modifications:	• Updated reflow soldering of the HVQFN48 package to add three figures: Figure 46 “Reflow soldering of the HVQFN48 package (7x7) 1 of 3”, Figure 47 “Reflow soldering of the HVQFN48 package (7x7) 2 of 3” and Figure 48 “Reflow soldering of the HVQFN48 package (7x7) 3 of 3”.			
LPC84X v.1.5	20171214	Product data sheet	-	LPC84X v.1.4
Modifications:	• Updated Table 25 “Dynamic characteristic: Typical wake-up times from low power modes”. • Removed remark from Section 8.17 “Capacitive Touch Interface”: **Remark:** Evaluation kits and software packages for Capacitive Touch will be available in late Q3-2017.			
LPC84X v.1.4	20171128	Product data sheet	-	LPC84X v.1.3
Modifications:	• Updated Table 17 “Dynamic characteristic: FRO”. Added conditions: –20 °C ≤ T_{amb} ≤ 70 °C and –40 °C ≤ T_{amb} ≤ 105 °C. • Updated Figure 8 “LPC84x AHB Memory mapping”. • Updated table notes: Table 15 “Static characteristics, pin characteristics”. • Updated Table 14 “Power consumption for individual analog and digital blocks”: FRO Typical supply current in µA is 89.			
LPC84X v.1.3	20170809	Product data sheet	-	LPC84X v.1.2
Modifications:	• Updated Table 9 “Limiting values”: Added max values for supply and ground pins for LQFP48, HVQFN48, and HVQFN33 packages. • Updated Table 1 “Ordering information”: Description of part number LPC844M201JHI48 and package name, HVQFN48.			
LPC84X v.1.2	20170801	Product data sheet	-	LPC84X v.1.1
Modifications:	• Updated Table 7 “Peripheral configuration in reduced power modes” and Table 8 “Wake-up sources for reduced power modes”: Cap Touch interrupt can wake up from power down mode. • Updated Table 2 “Ordering options”. LPC845M301JHI33 does not have Capacitive Touch.			
LPC84X v.1.1	20170623	Product data sheet	-	LPC84X v.1
Modifications:	• Updated Table 27 “12-bit ADC static characteristics”. • Added a remark to Section 8.17 “Capacitive Touch Interface”: Evaluation kits and software packages for Capacitive Touch will be available in late Q3-2017.			
LPC84X v.1	20170619	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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