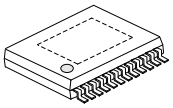
2.6W STEREO AUDIO AMPLIFIER



HTSSOP-24

■ DESCRIPTION

The UTC **PA3332** is a stereo audio power amplifier.

When the device is idle, it enters SHDN mode for some low current consumption applications. The current dissipation is thus reduced below 5μA. Mute function is included to mute the output.

Operating on a 5V power supply, the UTC **PA3332** is capable of driving a 4.0 Ω BTL load at a continuous average RMS output of 2.0W per channel with a less than 1% THD. %

There are two input paths, therefore, two different gain loops can be set in the same PCB. We could choose one of the two gain paths through the logic level of $\overline{IN}$/IN pin. This increases the flexibility of the hardware design. In order to prevent the speakers from burned-out, the UTC **PA3332** also has a function of maximum output power clamping is designed.

■ FEATURES

* Including de-pop circuit
* Output power at 1% THD+N, VDD=5V
  2.0W/CH (TYP.) into a 4Ω Load
  1.3W/CH (TYP.) into a 8Ω Load
* Output power at 10% THD+N, VDD=5V
  2.6W/CH (typical) into a 4Ω Load
  1.6W/CH (typical) into a 8Ω Load
* BTL mode (Bridge-Tied Load)
* Maximum output power clamping circuitry contained
* Mute and shutdown control available
* Stereo input MUX
* Halogen Free

■ ORDERING INFORMATION

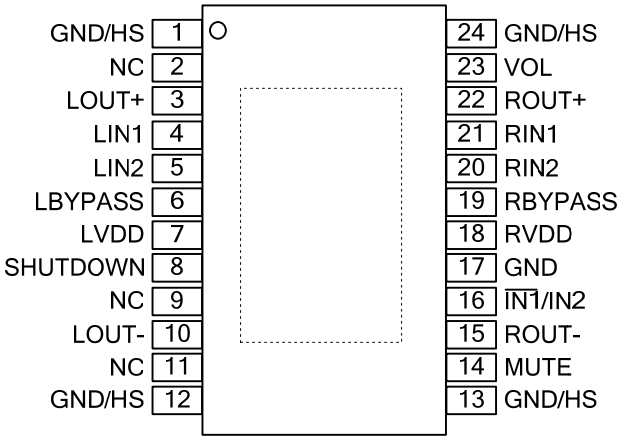
Ordering Number		Package	Packing
Lead Free	Halogen Free		
PA3332L-N24-T	PA3332G-N24-T	HTSSOP-24	Tube
PA3332L-N24-R	PA3332G-N24-R	HTSSOP-24	Tape Reel

PA3332L-N24-T
(1)Packing Type
(2)Package Type
(3)Lead Free

(1) R: Tape Reel, T: Tube
(2) N24: HTSSOP-24
(3) G: Halogen Free, L:Lead Free

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■ PIN CONFIGURATION

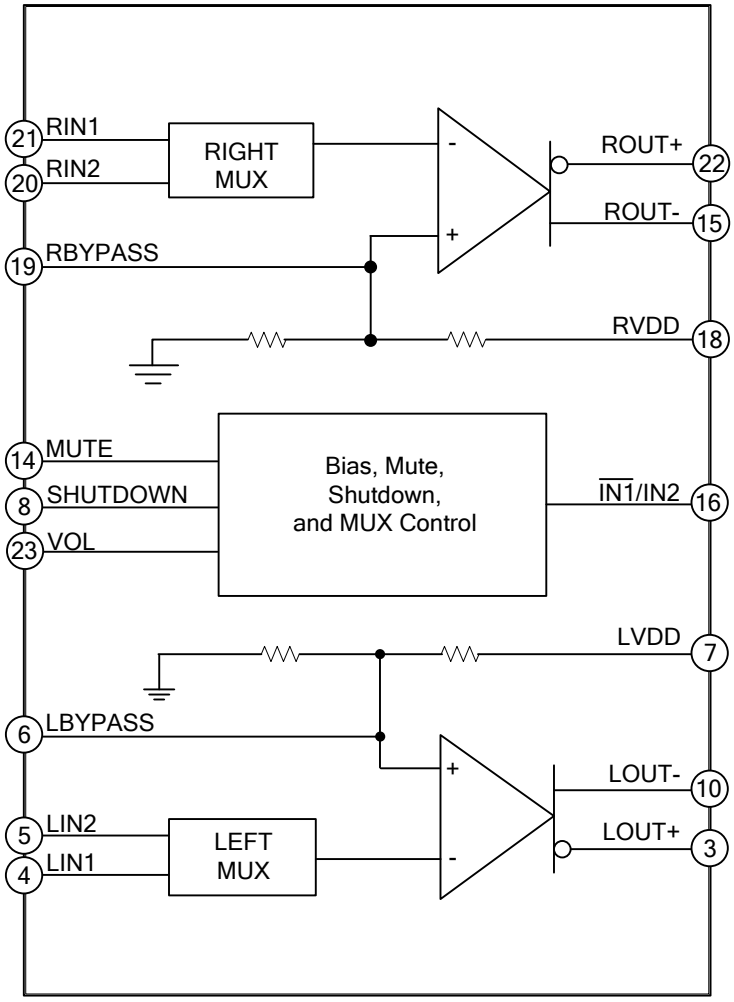


Note: Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1, 12, 13, 24	GND/HS	Ground connection for circuitry, directly connected to thermal pad.
2, 9, 11	NC	Embedded test mode pin, please keep it floating.
3	LOUT+	Left channel + output in BTL mode
4	LIN1	Left channel IN1 input, selected when $\overline{IN1}$ /IN2 pin is held low.
5	LIN2	Left channel IN2 input, selected when $\overline{IN1}$ /IN2 pin is held high.
6	LBPASS	Connect to voltage divider for left channel internal mid-supply bias.
7	LVDD	Supply voltage input for left channel and for primary bias circuits.
8	SHUTDOWN	Shutdown mode control signal input, places entire IC in shutdown mode when held high, I_{DD}< 5μA.
10	LOUT-	Left channel - output in BTL mode.
14	MUTE	Mode control signal input, hold low for activation, hold high for mute.
15	ROUT-	Right channel - output in BTL mode
16	$\overline{IN1}$/IN2	MUX control input, hold high to select in2 inputs (5,20), hold low to select in1 inputs (4,21).
17	GND	Ground connection for circuitry.
18	RVDD	Supply voltage input for right channel.
19	RBYPASS	Connect to voltage divider for right channel internal mid-supply bias.
20	RIN2	Right channel in2 input, selected when $\overline{IN1}$ /IN2 pin is held high.
21	RIN1	Right channel in1 input, selected when $\overline{IN1}$ /IN2 pin is held low.
22	ROUT+	Right channel + output in BTL mode
23	VOL	The output power can be clamped by setting a low bound voltage to this pin. The high bound voltage will be generated internally. The output voltage will be clamped between high/low bound voltages. Then the output power is lim-ited. It is weakly pull-low internally, let this pin floating or tied to GND can deactivate this function.
Thermal Pad		Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{DD}	6	V
Input Voltage		V_{IN}	-0.3~V_{DD}+0.3	V
Operating Ambient Temperature		T_A	-40 ~ +85	°C
Junction Temperature		T_J	150	°C
Storage Temperature		T_{STG}	-65 ~ +150	°C
Reflow Temperature (soldering, 10sec)			260	°C
Power Dissipation (Note 2)	$T_A \le 25°C$	P_D	2.7	W
	$T_A \le 70°C$		1.7	
	$T_A \le 85°C$		1.4	
Electrostatic Discharge Human Body Mode		V_{ESD}	-3000 ~ 3000 (Note 3)	V

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Recommended PCB Layout
3. Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC Electrical Characteristics (T_A=+25°C)							
Supply Current in Mute Mode	$I_{DD(MTE)}$	V_{DD} =3.3V	Stereo BTL		7	13	mA
		V_{DD} = 5V	Stereo BTL		8	16	
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2			5	50	mV
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V			2	5	μA
AC Operation Characteristics (V_{DD} = 5.0V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)							
Output Power (Note 1)	P_{OUT}	THD = 1%, BTL, R_L = 4Ω			2.0		W
		THD = 1%, BTL, R_L = 8Ω			1.3		
		THD = 10%, BTL, R_L = 4Ω			2.6		
		THD = 10%, BTL, R_L = 8Ω			1.6		
Total Harmonic Distortion Plus Noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω			100		m%
		P_O = 1W, BTL, R_L = 8Ω			60		
		V_I = 1V, R_L = 10KΩ, G = 1			10		
Max Output Power Bandwidth	B_{OM}	G = 1, THD = 1%			20		kHz
Phase Margin		R_L = 4Ω, Open Load			60		°
Power Supply Ripple Rejection	PSRR	f = 120Hz			65		dB
Mute Attenuation					90		dB
Channel-To-Channel Output Separation		f = 1kHz			80		dB
$\overline{IN1}$/IN2 Input Separation					80		dB
Input Impedance	Z_I				2		MΩ
Signal-To-Noise Ratio		P_O = 500mW, BTL			90		dB
Output Noise Voltage	V_n	Output noise voltage			55		μV(rms)
AC Operation Characteristics (V_{DD} =3.3V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)							
Output Power (Note 1)	P_{OUT}	THD = 1%, BTL, R_L = 4Ω			0.85		W
		THD = 1%, BTL, R_L = 8Ω			0.55		
		THD = 10%, BTL, R_L = 4Ω			1.1		
		THD = 10%, BTL, R_L = 8Ω			0.7		
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.7W, BTL, R_L = 4Ω			270		m%
		P_O = 0.45W, BTL, R_L = 8Ω			100		
		V_I = 1V, R_L = 10KΩ, G = 1			10		
Max Output Power Bandwidth	B_{OM}	G = 1, THD = 1%			20		kHz
Phase Margin		R_L = 4Ω, Open Load			60		°
Power Supply Ripple Rejection	PSRR	f = 120Hz			65		dB
Mute Attenuation					90		dB
Channel-To-Channel Output Separation		f = 1kHz			80		dB
$\overline{IN1}$/IN2 Input Separation					80		dB
Input Impedance	Z_I				2		MΩ
Signal-To-Noise Ratio		P_O = 500mW, BTL			90		dB
Output Noise Voltage	V_n	Output noise voltage			55		μV(rms)

Note 1: Output power is measured at the output terminals of the IC at 1kHz.

■ APPLICATION INFORMATION

Input MUX Operation

For the UTC **PA3332**, there exist two input signal paths (IN1 and IN2). Thus, for different input sources, the UTC **PA3332** has different gains with this prompt setting. When the IN1 / IN2 pin is in active high, this device operates in IN2 input source; when it is in active low, this device operates in IN1 input source.

Bridged-Tied Load Mode Operation

The following figure A shows the BTL (Bridged-Tied Load) mode operation. The two linear amplifiers drive both ends of the speaker load.

There are several advantages for using the BTL mode: first of all, the differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. The voltage swing on the load is two times that on a ground reference load. In this mode, the peak-to-peak voltage V_O(PP) on the load will be double a ground reference configuration. 4 times output power on the load will be generated at the same power supply rail and loading due to the voltage on the load is doubled. Further more, this BTL operation can cancel the dc offsets which save the using of dc coupling capacitor that is needed to cancel dc offsets in the ground reference configuration. Then the input network and speaker responses can only limit the low-frequency performance. Moreover, the saving of dc coupling capacitors can minimize PCB space and the cost.

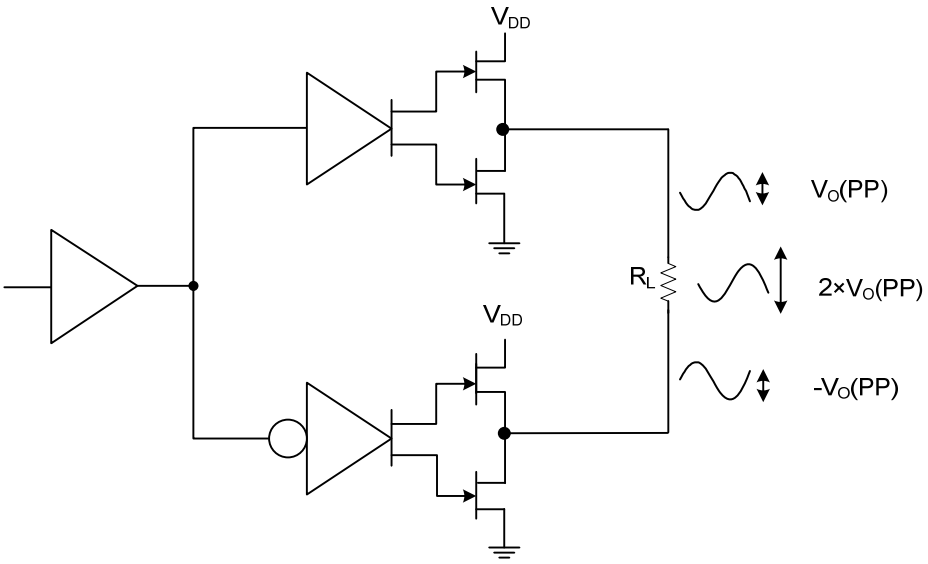


Figure A.

MUTE and SHUTDOWN Mode Operations

Circuits with mute and shutdown functions are contained in the UTC **PA3332**, which is designed to reduce I_{DD} (supply current) to the absolute minimum level during nonuse periods for battery-power conservation.

When pulling the shutdown pin (pin 8) high, all linear amplifiers will be deactivated to mute the amplifier outputs. Then the device enters an extremely low current consumption condition, the supply current is less than 5μA. When the mute pin (pin 14) is pulled high, it will force the activated linear amplifier to supply the VDD/2 dc voltage on the output & shutdown the second linear amplifiers to mute the AC performance. The current dissipation will be smaller in the mute mode operation than that in the BTL mode.

It is not allowed to leave the shutdown and mute pins floating, or unexpected conditions would occur for the amplifier operations.

Maximum Power Clampping Function

The UTC **PA3332** incorporated the maximum power clamping function that effectively reduces damage the speaker due to the larger power through the speaker. The Vol pin (pin 23) is weakly pull-low internally. If a non-zero voltage applies in the Vol pin, the UTC **PA3332** will generate a high boundary voltage which the difference between the VDD/2 and the high boundary voltage is the same as the difference between the VDD/2 and the low boundary voltage. (i.e. V_{OH} – VDD/2 = VDD/2 – V_{OL}). Then the outputs of linear amplifiers will be effectively limited between the high/low boundary voltage, the maximum output power is clamped. Thus, the maximum power is controlled perfectively by means of setting the value of Vol,

Note that if this function is not used, the Vol pin should be connected to the GND or be floated.

Optimizing DEPOP Operation

The UTC **PA3332** contains a circuit that can reduce poping to minimum during the power-up or shutdown mode. The poping can be generated as long as a voltage step is applied to the speaker and the differential voltage generated at the two ends of the speaker.

To get a minimum poping, the bypass capacitor is critical, $1/(C_B x 100k\Omega) \leqq 1/(C_I*(R_I+R_F))$. (Where C_B is the mid-rail bypass capacitor, 100kΩ is the output impedance of the mid-rail generator, R_I is the input impedance, C_I is the input coupling capacitor, R_F is the gain setting impedance which is on the feedback path. C_B is the most important capacitor. It can be applied in reducing the poping together with determining the rate at which the amplifier starts up during startup or recovery from shutdown mode.)

The Figure B shows the de-poping circuit for the UTC **PA3332**. The PNP transistor effectively controls the voltage drop across the 50kΩ by slewing the internal node slowly when power is applied.

At start-up, the voltage at BYPASS capacitor is zero. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an RC circuit.

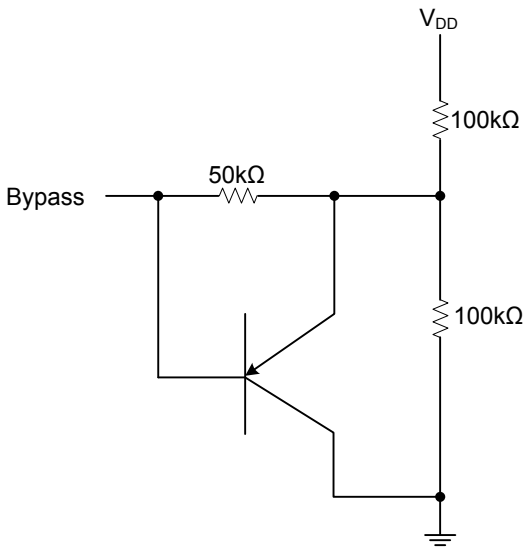
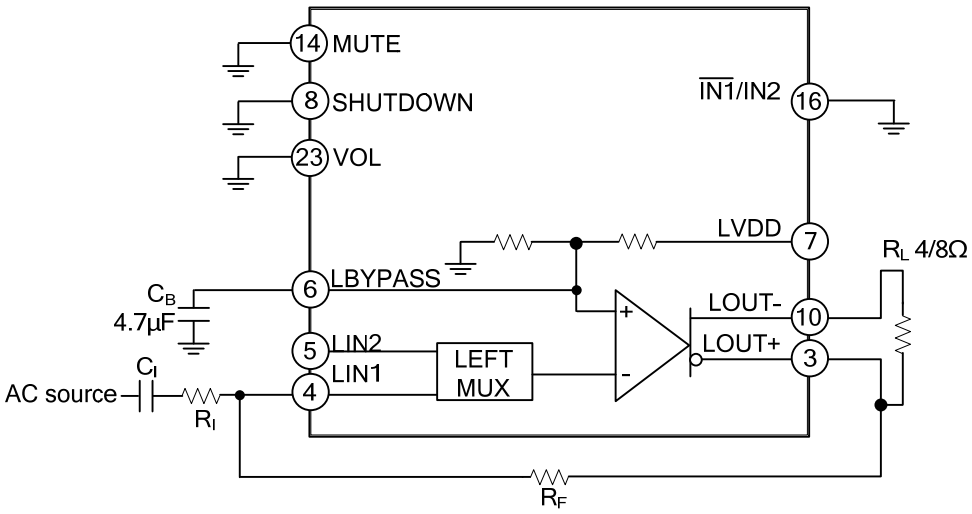


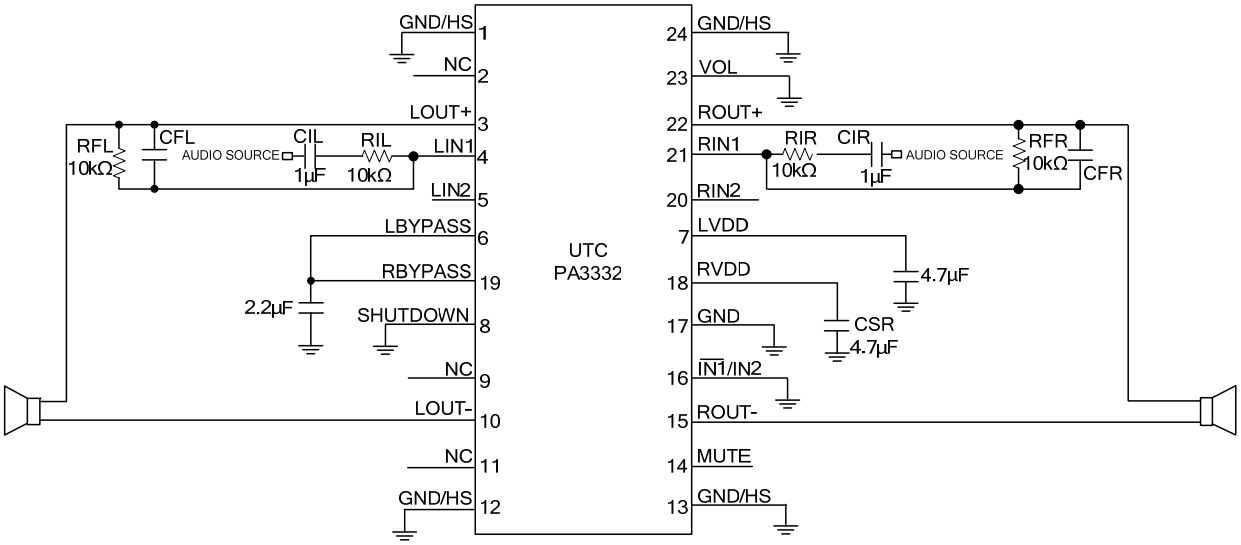
Figure B.

■ TEST CIRCUIT



BTL Mode Test circuit

■ TYPICAL APPLICATION CIRCUIT



Logical Truth Table

OUTPUT						
Mute	1IN /IN2	Shutdown	Input	L/R Out+	L/R Out-	Mode
X	X	High	X	-	-	Shutdown (Mute)
Low	Low	Low	L/R IN1	Output	Output	BTL
Low	High	Low	L/R IN2	Output	Output	BTL
High	Low	Low	L/R IN1	Output	-	Mute
High	High	Low	L/R IN2	Output	-	Mute

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