MAX5991A/MAX5991B

IEEE 802.3af-Compliant, High-Efficiency, Class 1/Class 2, Powered Devices with Integrated DC-DC Converter

General Description

The MAX5991A/MAX5991B provide a complete power-supply solution as IEEE® 802.3af-compliant Class 1/ Class 2 Powered Devices (PDs) in a Power-over-Ethernet (PoE) system. The devices integrate the PD interface with an efficient DC-DC converter, offering a low external part count PD solution. The devices also include a low-drop-out regulator, MPS, sleep, and ultra-low power modes.

The PD interface provides a detection signature and a Class 1/Class 2 classification signature with a single external resistor. The PD interface also provides an isolation power MOSFET, a 60mA (max) inrush current limit, and a 321mA (typ) operating current limit.

The integrated step-down DC-DC converter uses a peak current-mode control scheme and provides an easy-to-implement architecture with a fast transient response. The step-down converter operates in a wide input voltage range from 8.7V to 60V and supports up to 6.49W of input power at 1.3A load. The DC-DC converter operates at a fixed 430kHz switching frequency, with an efficiency-boosting frequency foldback that reduces the switching frequency by half at light loads.

The devices feature an input undervoltage-lockout (UVLO) with wide hysteresis and long deglitch time to compensate for twisted-pair cable resistive drop and to assure glitch-free transition during power-on/-off conditions. The devices also feature overtemperature shutdown, short-circuit protection, output overvoltage protection, and hiccup current limit for enhanced performance and reliability.

All devices are available in a 20-pin, 4mm x 4mm, TQFN power package and operate over the -40°C to +85°C temperature range.

Applications

- IEEE 802.3af-Powered Devices
- IP Phones
- Wireless Access Nodes
- IP Security Cameras
- WiMAX® Base Stations

Benefits and Features

- High Integration Saves Space and BOM Cost
  - Efficient, Integrated DC-DC Converter (with Integrated Switches)
  - Built-In Output-Voltage Monitoring
  - Protects Against Overload, Output Short Circuit, Output Overvoltage, and Overtemperature
  - Integrated TVS Diode Withstands Cable Discharge Event (CDE)
  - Internal LDO Regulator with Up to 100mA Load
- IEEE 802.3af-Compliant Features Reduce Design Time
  - PoE Class 1/Class 2 Classification Set with Single Resistor
  - Intelligent Maintain Power Signature (MPS) Complies with IEEE 802.3af Specification
  - Simplified Wall Adapter Interface
  - Pass 2kV, 200m CAT-6 Cable Discharge Event
- High Efficiency During Light Loads Reduces Power Consumption
  - Sleep and Ultra-Low-Power Mode
  - Frequency Foldback for High-Efficiency Light-Load Operation
  - Back-Bias Capability to Optimize the Efficiency
- Robust Performance
  - 8.7V to 60V Wide Input Voltage Range
  - Hiccup-Mode Runaway Current Limit
  - 49mA (typ) Inrush Current Limit
  - Open-Drain $\overline{\text{RESET}}$ Output
- Easy to Design With
  - 3.2V to 14V Programmable Output Voltage Range
  - Internal Compensation
  - Fixed 430kHz Switching Frequency

***Ordering Information* appears at end of data sheet.**

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19-6529; Rev 2; 1/15

Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)
V_{DD} to GND ..... -0.3V to +70V
(100V, 100ms, R_{TEST} = 3.3kΩ) (Note 1)
V_{CC}, WAD, RREF to GND ..... -0.3V to (V_{DD} + 0.3V)
AUX, LDO_IN, LED to GND ..... -0.3V to 16V
LDO_OUT to GND ..... -0.3V to (LDO_IN + 0.3V)
LDO_FB to GND ..... -0.3V to +6V
LX to GND ..... -0.3V to (V_{CC} + 0.3V)
LDO_OUT, VDRV, FB, $\overline{RESET}$, $\overline{WK}$, $\overline{SL}$, $\overline{ULP}$, MPS, CLASS2 to GND ..... -0.3V to +6V
VDRV to V_{DD} ..... -0.3V to (V_{DD} + 0.3V)
PGND to GND ..... -0.3V to +0.3V
LX Total RMS Current 1.6A
Continuous Power Dissipation (T_A = + 70°C)
TQFN (derate 28.6mW/°C above +70°C) 2285.7mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: See Figure 1, Test Circuit.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2.7°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 48V, R_{SIG} = 24.9kΩ, LED, V_{CC}, $\overline{SL}$, $\overline{ULP}$, $\overline{WK}$, $\overline{RESET}$, LDO_OUT unconnected, WAD = LDO_EN = LDO_IN = PGND = GND, C1 = 68nF, C2 = 10µF, C3 = 1µF (see Figure 3), V_{FB} = V_{AUX} = 0V, LX unconnected, CLASS2 = 0V, MPS = 0V. All voltages are referenced to GND, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER DEVICE (PD) INTERFACE							
DETECTION MODE							
Input Offset Current	I_{OFFSET}	V_{VDD} = 1.4V to 10.1V (Note 4)				8	µA
Effective Differential Input Resistance	dR	V_{VDD} = 1.4V to 10.1V with 1V step, (Note 5)		23.95		25.5	kΩ
CLASSIFICATION MODE							
Classification Enable Threshold	$V_{TH,CLS,EN}$	V_{DD} rising		10.2	11.42	12.5	V
Classification Disable Threshold	$V_{TH,CLS,DIS}$	V_{DD} rising		22	23	23.8	V
Classification Stability Time					2		ms
Classification Current	I_{CLASS}	V_{DD} = 12.6V to 20V	CLASS2 = GND	9.12	10.5	11.88	mA
			CLASS2 = VDRV	16.1	18	20.9	
POWER MODE							
V_{DD} Supply Voltage Range	V_{DD}					60	V
V_{DD} Supply Current	I_{DD}	V_{DD} = 60V			4.8	6.6	mA
V_{DD} Turn-On Voltage	V_{ON}	V_{DD} rising		37.2	38.7	40	V
V_{DD} Turn-Off Voltage	V_{OFF}	V_{DD} falling		30	31.4		V

Electrical Characteristics (continued)

(V_{DD} = 48V, R_{SIG} = 24.9kΩ, LED, V_{CC}, $\overline{SL}$, $\overline{ULP}$, $\overline{WK}$, $\overline{RESET}$, LDO_OUT unconnected, WAD = LDO_EN = LDO_IN = PGND = GND, C1 = 68nF, C2 = 10µF, C3 = 1µF (see Figure 3), V_{FB} = V_{AUX} = 0V, LX unconnected, CLASS2 = 0V, MPS = 0V. All voltages are referenced to GND, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Turn-On/Off Hysteresis	V_{HYST_UVLO}	(Note 6)			7.3		V
V_{DD} Deglitch Time	t_{OFF_DLY}	V_{DD} falling from 40V to 20V (Note 5)			150		µs
Inrush to Operating Mode Delay	t_{DELAY}	t_{DELAY} = time after (V_{DD} - V_{CC}) from 1.5V to 0V			115		ms
Isolation Power MOSFET On-Resistance	R_{ON_ISO}	I_{VCC} = 100mA	T_J = +25°C		1.2		Ω
			T_J = +85°C		1.5		
MAINTAIN POWER SIGNATURE (MPS = VDRV)							
PoE MPS Current Rising Threshold	I_{MPS_RISE}			18	28.7	40	mA
PoE MPS Current Falling Threshold	I_{MPS_FALL}			14	24	35	mA
PoE MPS Current Threshold Hysteresis	I_{MPS_HYS}				4.3		mA
PoE MPS Output Average Current	I_{MPS_AVE}				4.8		mA
PoE MPS Peak Output Current	I_{MPS_PEAK}			10	12.6		mA
PoE MPS Time High	I_{MPS_HIGH}				95		ms
PoE MPS Time Low	I_{MPS_LOW}				190		ms
CURRENT LIMIT							
Inrush Current Limit	I_{INRUSH}	During initial turn-on period, V_{DD} - V_{CC} = 4V, measured at V_{CC}		39	49	60	mA
Current Limit During Normal Operation	I_{LIM}	After inrush completed, V_{CC} = V_{DD} - 1.5V, measured at V_{CC}		290	321	360	mA
LOGIC							
WAD Detection Rising Threshold	V_{WAD_RISE}					8.8	V
WAD Detection Falling Threshold	V_{WAD_FALL}			5.8			V
WAD Detection Hysteresis					0.6		V
WAD Input Current	I_{WAD}	V_{WAD} = 24V			125		µA
CLASS2, MPS Voltage Rising Threshold						2.9	V
CLASS2, MPS Voltage Falling Threshold				0.4			V
$\overline{RESET}$ Output Voltage Low		I_{SINK} = 1mA				0.2	V
$\overline{RESET}$, CLASS2, MPS Leakage				-1		+1	µA

Electrical Characteristics (continued)

(V_{DD} = 48V, R_{SIG} = 24.9kΩ, LED, V_{CC}, $\overline{SL}$, $\overline{ULP}$, $\overline{WK}$, $\overline{RESET}$, LDO_OUT unconnected, WAD = LDO_EN = LDO_IN = PGND = GND, C1 = 68nF, C2 = 10µF, C3 = 1µF (see Figure 3), V_{FB} = V_{AUX} = 0V, LX unconnected, CLASS2 = 0V, MPS = 0V. All voltages are referenced to GND, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REGULATOR WITH BACK BIAS						
V_{AUX} Input Voltage Range	V_{AUX}	Inferred from V_{AUX} input current	4.75		14	V
V_{AUX} Input Current		V_{AUX} from 4.75V to 14V	0.65		3.1	mA
V_{DRV} Output Voltage			4.2		5.5	V
SLEEP MODE						
$\overline{WK}$ and $\overline{ULP}$ Logic Threshold	V_{TH}	$V_{\overline{WK}}$ falling and $V_{\overline{ULP}}$ rising and falling	1.6		2.9	V
$\overline{SL}$ Logic Threshold		Falling	0.55		0.8	V
$\overline{SL}$ Current		$V_{\overline{SL}}$ = 0V		62		µA
LED Current Amplitude	I_{LED}	$R_{\overline{SL}}$ = 60.4kΩ, V_{LED} = 6.5V	9.2	10.6	12	mA
		$R_{\overline{SL}}$ = 30.2kΩ, V_{LED} = 6.5V	19.2	21.2	23.5	
		$R_{\overline{SL}}$ = 30.2kΩ, V_{LED} = 3.5V		21.2		
LED Current Programmable Range	I_{RANGE}		10		20	mA
LED Current with Grounded $\overline{SL}$		$V_{\overline{SL}}$ = 0V	20.6	26	31.4	mA
LED Current Frequency	f_{ILED}	Sleep and ultra-low power modes		250		Hz
LED Current Duty Cycle	D_{ILED}	Sleep and ultra-low power modes		25		%
V_{DD} Current Amplitude	I_{VDD}	Sleep mode, V_{LED} = 6.5V	10	12	14.5	mA
Internal Current Duty Cycle	D_{IVDD}	Sleep and ultra-low power modes		75		%
Internal Current Enable Time	t_{MPS}	Ultra-low power mode	76	88	98	ms
Internal Current Disable Time	t_{MPDO}	Ultra-low power mode	205	237	265	ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SD}	T_J rising		151		°C
Thermal Shutdown Hysteresis	$T_{SD,HYS}$			16		°C
LDO						
Input Voltage Range		Inferred from line regulation	4.5		14	V
Output Voltage		LDO_FB = V_{DRV}		3.3		V
Max Output Voltage Setting		With external divider to LDO_FB			5.5	V
LDO Quiescent Current		V_{LDO_IN} = 4.5V		4		µA
LDO FB Regulation Voltage			1.20	1.227	1.25	V
LDO FB Leakage Current			-1		+1	µA
Dropout		V_{LDO_IN} = 5V, V_{LDO_FB} = V_{DRV}, I_{LOAD} = 80mA		265		mV
Load Regulation		I_{LOAD} from 1mA to 80mA		0.5		mV/mA
Line Regulation		V_{LDO_IN} from 4.5V to 14V		1.4		mV/V
Overcurrent Limit			85			mA

Electrical Characteristics (continued)

(V_{DD} = 48V, R_{SIG} = 24.9kΩ, LED, V_{CC}, $\overline{SL}$, $\overline{ULP}$, $\overline{WK}$, $\overline{RESET}$, LDO_OUT unconnected, WAD = LDO_EN = LDO_IN = PGND = GND, C1 = 68nF, C2 = 10µF, C3 = 1µF (see Figure 3), V_{FB} = V_{AUX} = 0V, LX unconnected, CLASS2 = 0V, MPS = 0V. All voltages are referenced to GND, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO_FB Rising Threshold					3.3	3.7	V
LDO_FB Hysteresis					2.4		V
DC-DC CONVERTER INPUT SUPPLY							
V_{DD} Voltage Range	$V_{DD,RISING}$	V_{CC} = V_{DD} = V_{WAD} - 0.3V, rising		8		60	V
	$V_{DD,FALLING}$	V_{CC} = V_{DD} = V_{WAD} - 0.3V, falling		7.7		60	
WAD Detection Rising Threshold	$V_{WAD,RISE}$	(Note 7)				8.8	V
WAD Detection Falling Threshold	$V_{WAD,FALL}$	(Note 7)		5.8			V
WAD Detection Hysteresis					0.6		V
POWER MOSFETs							
High-Side pMOS On-Resistance	R_{DSON-H}	I_{LX} = 0.5A (sourcing)			0.54		Ω
Low-Side nMOS On-Resistance	R_{DSON-L}	I_{LX} = 0.5A (sinking)			0.14		Ω
LX Leakage Current	I_{LX-LKG}	V_{DD} = V_{CC} = 28V, V_{LX} = (V_{PGND} + 1V) to (V_{CC} - 1V)		-5		+5	µA
SOFT-START (SS)							
Soft-Start Time	t_{SS-TH}				10		ms
FEEDBACK (FB)							
FB Regulation Voltage	V_{FB-RG}			1.203	1.226	1.252	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.224V			10	200	nA
OUTPUT VOLTAGE							
Output Voltage Range	V_{OUT}	MAX5991A		3.0		5.6	V
		MAX5991B		5.4		14	
Cycle by Cycle Overvoltage Protection	V_{OUT-OV}	Rising (Note 8)		101		108	%
		Falling (Note 8)		98.5		104	
INTERNAL COMPENSATION NETWORK							
Compensation Network Zero-Resistance	R_{ZERO}				200		kΩ
Compensation Network Zero-Capacitance	C_{ZERO}				150		pF
CURRENT LIMIT							
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$	MAX5991A	CLASS2 = GND	1.45	1.64		A
			CLASS2 = VDRV	1.66	1.79		
		MAX5991B	CLASS2 = GND	0.75	0.81		
			CLASS2 = VDRV	0.85	0.94		

Electrical Characteristics (continued)

(V_{DD} = 48V, R_{SIG} = 24.9kΩ, LED, V_{CC}, $\overline{SL}$, $\overline{ULP}$, $\overline{WK}$, $\overline{RESET}$, LDO_OUT unconnected, WAD = LDO_EN = LDO_IN = PGND = GND, C1 = 68nF, C2 = 10µF, C3 = 1µF (see Figure 3), V_{FB} = V_{AUX} = 0V, LX unconnected, CLASS2 = 0V, MPS = 0V. All voltages are referenced to GND, unless otherwise noted. T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$	MAX5991A	CLASS2 = GND		1.9		A
			CLASS2 = VDRV		2.1		
		MAX5991B	CLASS2 = GND		0.93		
			CLASS2 = VDRV		1.07		
Valley Current-Limit Threshold	$I_{VALLEY-LIMIT}$	MAX5991A			1.45		A
		MAX5991B			0.75		
ZX Threshold	I_{ZX}				25		mA
TIMINGS							
Switching Frequency	f_{SW}			380	430	475	kHz
Frequency Foldback	$f_{SW-FOLD}$			195	215	238	kHz
Consecutive ZX Events for Entering Foldback					8		Events
Consecutive ZX Events for Exiting Foldback					8		Events
V_{OUT} Undervoltage Trip Level to Cause HICCUP	$V_{OUT-HICF}$	After soft-start completed (Note 8)		55	60	65	%
HICCUP Timeout					77		ms
Minimum On-Time	t_{ON-MIN}				113	140	ns
LX Dead Time					14		ns
$\overline{RESET}$							
V_{FB} Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling (Note 8)		87	90	93	%
V_{FB} Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising (Note 8)		91.5	95	98	%
V_{LDO_FB} Threshold for $\overline{RESET}$ Assertion	V_{LDO_FB-OKF}	V_{LDO_FB} falling, LDO_FB = V_{DRV} (Note 9)			90		%
V_{FB} Threshold for $\overline{RESET}$ Deassertion		V_{FB} rising			95		%
$\overline{RESET}$ Deassertion Delay					2.4		ms

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 4: The input offset current is illustrated in Figure 2.
Note 5: Effective differential input resistance is defined as the differential resistance between V_{DD} and GND, see Figure 2.
Note 6: A 20V glitch on input voltage, which takes V_{DD} below V_{ON} shorter than or equal to t_{OFF_DLY} does not cause the device to exit power-on mode.
Note 7: The WAD detection rising and falling thresholds control the isolation power MOS transistor. To turn the DC-DC on in WAD mode, the WAD must be detected and the V_{DD} must be within the V_{DD} voltage range.
Note 8: Referred to feedback regulation voltage.
Note 9: Referred to LDO feedback regulation voltage.

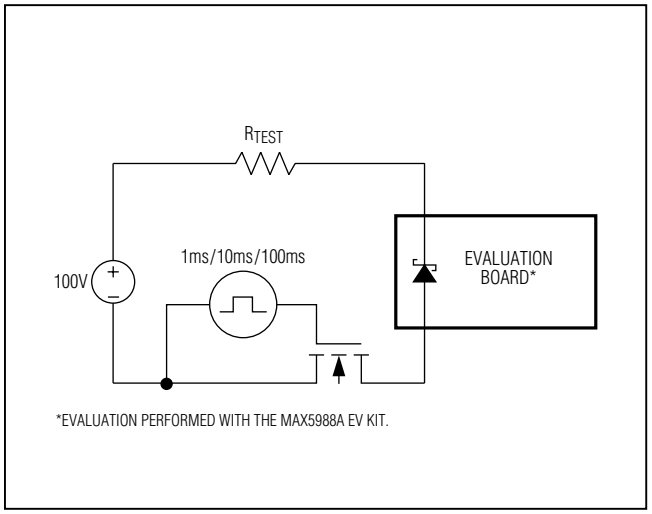


Figure 1. MAX5991A/MAX5991B Internal TVS Test Setup

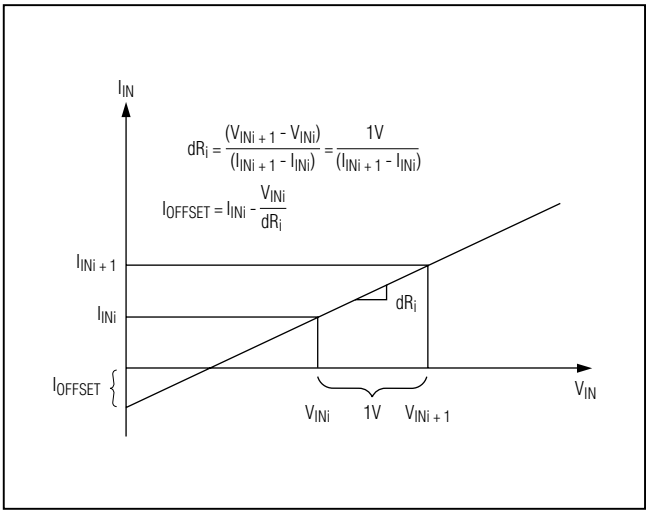
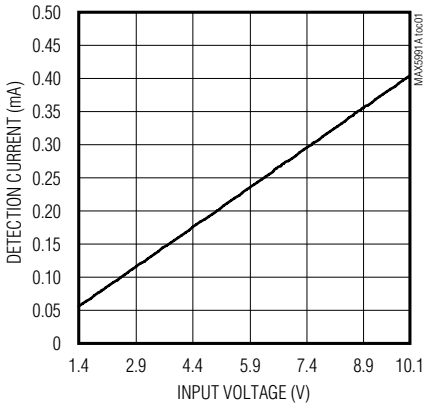


Figure 2. Effective Differential Resistance and Offset Current

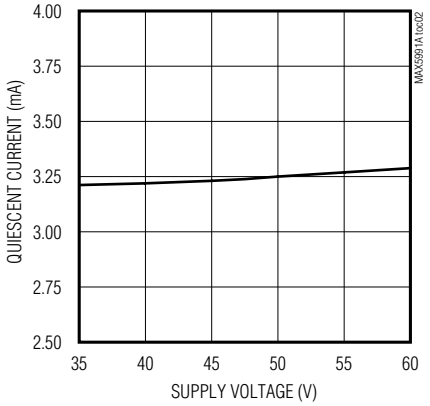
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

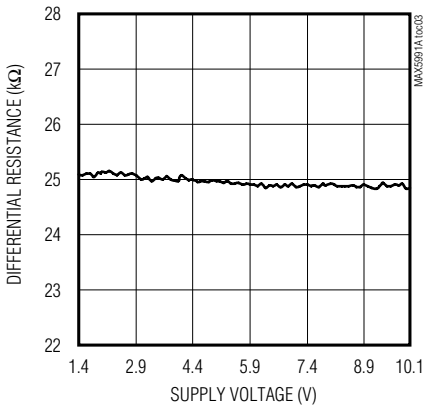
DETECTION CURRENT vs. INPUT VOLTAGE



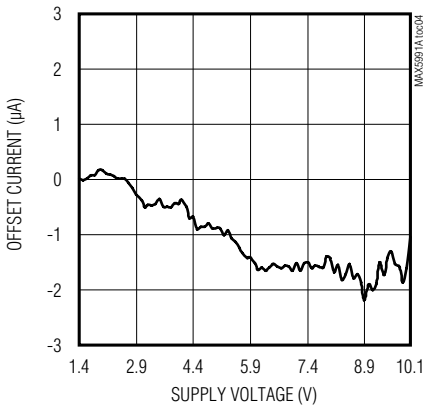
QUIESCENT CURRENT vs. SUPPLY VOLTAGE (ULTRA-LOW POWER MODE)



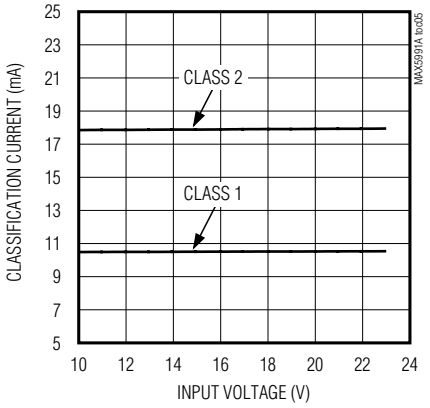
SIGNATURE RESISTANCE vs. SUPPLY VOLTAGE



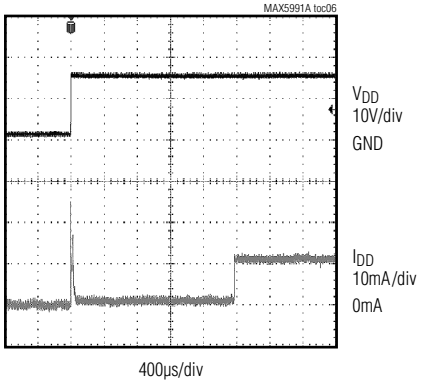
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



CLASSIFICATION CURRENT vs. INPUT VOLTAGE



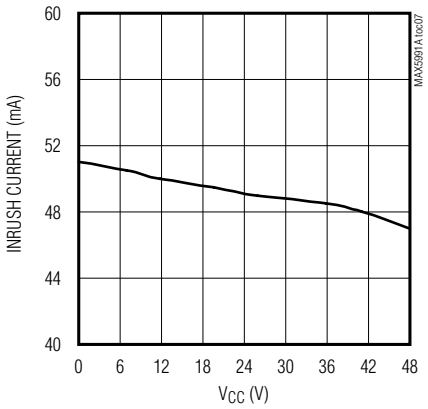
CLASSIFICATION SETTLING TIME



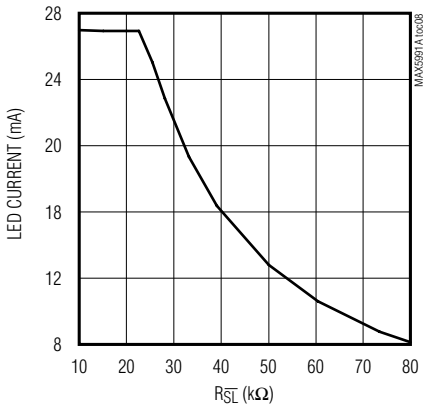
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

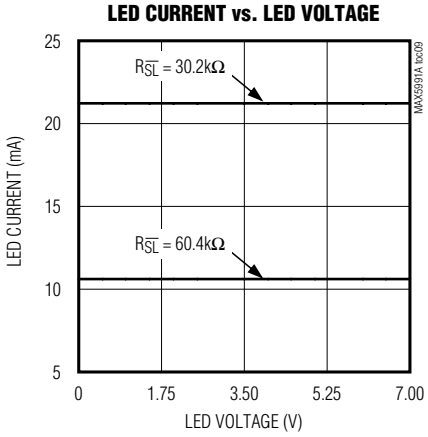
INRUSH CURRENT LIMIT vs. V_{CC} VOLTAGE



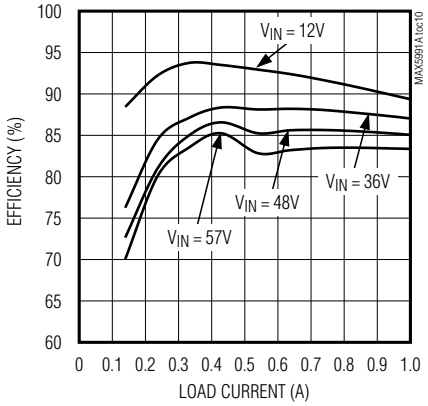
LED CURRENT vs. $R_{\overline{SL}}$



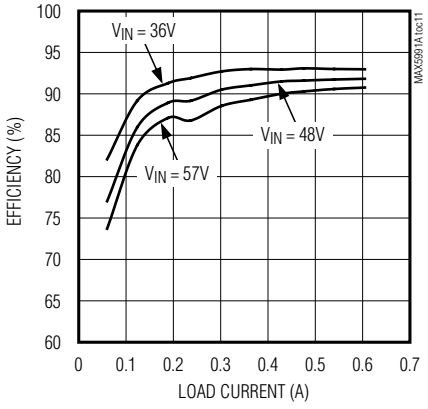
LED CURRENT vs. LED VOLTAGE



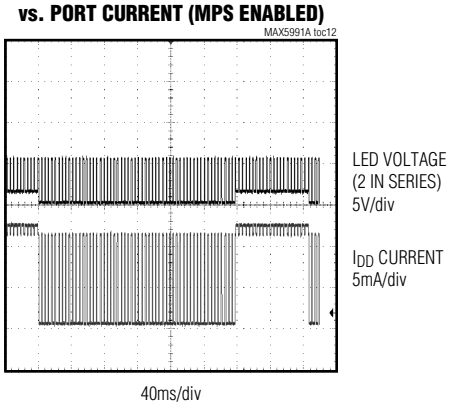
EFFICIENCY vs. LOAD CURRENT (MAX5991A, V_{OUT} = 5V)



EFFICIENCY vs. LOAD CURRENT (MAX5991B, V_{OUT} = 12V)



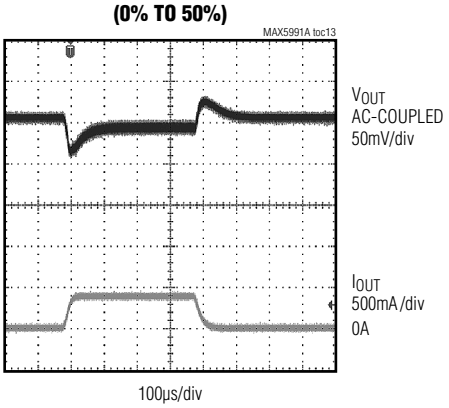
LED VOLTAGE vs. PORT CURRENT (MPS ENABLED)



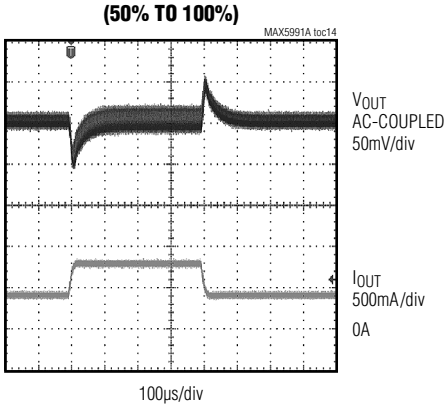
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

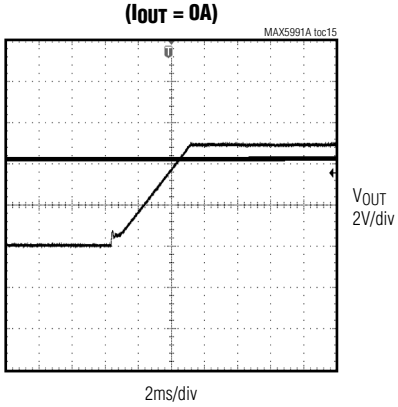
5V LOAD TRANSIENT (0% TO 50%)



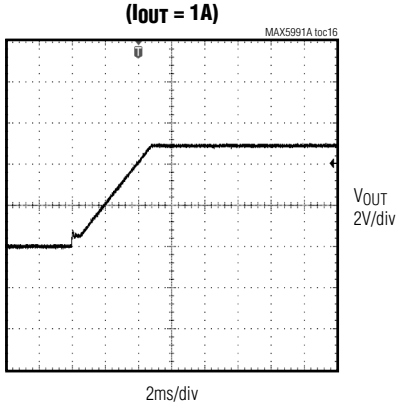
5V LOAD TRANSIENT (50% TO 100%)



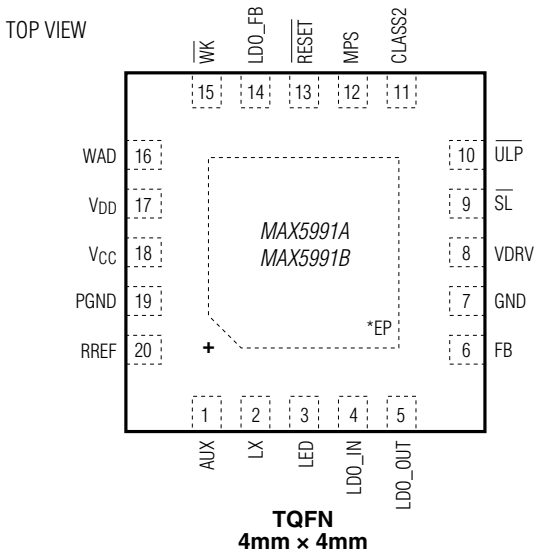
DC-DC CONVERTER STARTUP (I_{OUT} = 0A)



DC-DC CONVERTER STARTUP (I_{OUT} = 1A)



Pin Configurations



TQFN
4mm × 4mm

*EP = EXPOSED PAD. CONNECT EP TO GND.

Pin Description

PIN	NAME	FUNCTION
1	AUX	Auxiliary Voltage Input. Auxiliary input to the internal regulator, VDRV. Connect AUX to the output of the buck converter if the output voltage is greater than 4.75V to back bias the internal circuitry and increase efficiency. Connect to a clean ground when not used.
2	LX	Inductor Connection. Inductor connection for the internal DC-DC converter.
3	LED	LED Driver Output. In sleep mode, LED sources a periodic current (I_{LED}) at 250Hz with 25% duty cycle.
4	LDO_IN	LDO Input Voltage. Connect LDO_IN to the output of the DC-DC converter when used; otherwise, connect to GND. Connect a minimum 1µF bypass capacitor between LDO_IN and GND.
5	LDO_OUT	LDO Output Voltage. Connect a minimum 1µF output capacitor between LDO_OUT and GND.
6	FB	Feedback. Feedback input for the DC-DC buck converter. Connect FB to a resistive divider from the output to GND to adjust the output voltage.
7	GND	Ground. Reference rail for the device. It is also the “quiet” ground for all voltage reference (e.g., FB is referenced to this GND).
8	VDRV	Internal 5V Regulator Voltage Output. The internal voltage regulator provides 5V to the MOSFET driver and other internal circuits. VDRV is referenced to GND. Do not use VDRV to drive external circuits. Connect a 1µF bypass capacitor between VDRV and GND.

Pin Description (continued)

PIN	NAME	FUNCTION
9	$\overline{SL}$	Sleep Mode Enable Input. A falling edge on $\overline{SL}$ brings the device into sleep mode. An external resistor ($R_{\overline{SL}}$) connected between $\overline{SL}$ and GND sets the LED current (I_{LED}).
10	$\overline{ULP}$	Ultra-Low Power-Mode Enable Input. $\overline{ULP}$ has an internal 50kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{SL}$ while $\overline{ULP}$ is asserted low enables ultra-low power mode. When ultra-low power mode is enabled, the power consumption of the device is reduced even lower than sleep mode to comply with ultra-low power sleep power requirements while still supporting MPS.
11	CLASS2	Class 2 Selection Pin. Connect to VDRV for Class 2 operation. Connect to GND for Class 1 operation.
12	MPS	MPS Enable Pin. Connect to VDRV to turn the MPS function on. Connect to GND to turn the MPS function off.
13	$\overline{RESET}$	Open-Drain Reset Output. The $\overline{RESET}$ output is driven low if either LDO_OUT or FB drops below 90% of its set value. $\overline{RESET}$ goes high 100µs after both LDO_OUT and FB rise above 95% of their set values. Leave unconnected when not used.
14	LDO_FB	LDO Regulator Feedback Input. Connect to VDRV to get the preset LDO output voltage of 3.3V, or connect to a resistive divider from the LDO_OUT to GND for an adjustable LDO output voltage.
15	$\overline{WK}$	Wake Mode Enable Input. $\overline{WK}$ has an internal 50kΩ pullup resistor to the internal 5V bias rail. A falling edge on $\overline{WK}$ brings the device out of sleep mode and into the normal operating mode (wake mode).
16	WAD	Wall Power Adapter Detector Input. Wall adapter detection is enabled when the voltage from WAD to GND is greater than 8.8V. When a wall power adapter is present, the isolation p-channel power MOSFET turns off. Connect WAD directly to GND when the wall power adapter or other auxiliary power source is not used.
17	V_{DD}	Positive Supply Input. Connect a 68nF (min) bypass capacitor between V_{DD} and PGND.
18	V_{CC}	DC-DC Converter Power Input. V_{DD} is connected to V_{CC} by an isolation p-channel MOSFET. Connect a 10µF capacitor in parallel with a 1µF ceramic capacitor between V_{CC} and PGND.
19	PGND	Power Ground. Power ground of the DC-DC converter power stage. Connect PGND to GND with a star connection. Do not use PGND as reference for sensitive feedback circuit.
20	RREF	Signature Resistor Connection. Connect a 24.9kΩ resistor (R_{SIG}) to GND.
—	EP	Exposed Pad. Connect the exposed pad to ground.

Detailed Description

PD Interface

The MAX5991A/MAX5991B include complete interface functions for a PD to comply with the IEEE 802.3af standard as a Class 1/Class 2 PD. The devices provide the detection and classification signatures using a single external signature resistor. An integrated MOSFET provides isolation from the buck converter when the PSE has not applied power. The devices guarantee a leakage current offset of less than 8µA during the detection phase. The devices feature power-mode undervoltage-lockout (UVLO) with wide hysteresis and long deglitch time to compensate for twisted-pair-cable resistive drop and to ensure glitch-free transitions between detection, classification, and power-on/-off modes.

Operating Modes

The devices operate in three different modes depending on V_{DD}. The three modes are detection mode, classification mode, and power mode. The device is in detection mode when V_{DD} is between 1.4V and 10.1V, classification mode when V_{DD} is between 12.6V and 20V, and power mode when the input voltage exceeds V_{ON}.

Detection Mode ($1.4V \le V_{DD} \le 10.1V$)

In detection mode, the devices provide a signature differential resistance to V_{DD}. During detection, the power-sourcing equipment (PSE) applies two voltages to V_{DD}, both between 1.4V and 10.1V with a minimum 1V increment. The PSE computes the differential resistance to ensure the presence of the 24.9kΩ signature resistor. Connect the 24.9kΩ signature resistor (R_{SIG}) from RREF to GND for proper signature detection. The device applies V_{DD} to RREF when in detection mode, and the V_{DD} offset current due to the device is less than 8µA. The DC offset due to protection diodes does not significantly affect the signature resistance measurement.

Classification Mode ($12.6V \le V_{DD} \le 20V$)

In classification mode, the devices sink a Class 1/Class 2 classification currents. The PSE applies a classification voltage between 12.6V and 20V, and measures the classification currents. The devices use the external 24.9kΩ resistor (R_{SIG}) and the CLASS2 pin to set the classification current at 10.5mA (Class 1, CLASS1 = GND) or 18mA (Class 2, CLASS2 = VDRV). The PSE uses this to determine the maximum power to deliver. The classification current includes current drawn by the supply current of the device so the total current drawn by the PD is within the IEEE 802.3af standard. The classification current is turned off when the device leaves classification mode.

Power Mode ($V_{DD} \ge V_{ON}$)

In power mode, the devices have the isolation MOSFET between V_{DD} and V_{CC} fully on. The devices have the buck regulator enabled and the LDO enabled. The devices can be in either wake mode, sleep mode, or ultra-low power mode. The buck regulator and LDO are only enabled in wake mode.

The devices enter power mode when V_{DD} rises above the undervoltage lockout threshold (V_{ON}). When V_{DD} rises above V_{ON}, the device turns on the internal p-channel isolation MOSFET to connect V_{CC} to V_{DD} with inrush current limit internally set to 49mA (typ). The isolation MOSFET is fully turned on when V_{CC} is near V_{DD} and the inrush current is below the inrush limit. Once the isolation MOSFET is fully turned on, the device changes the current limit to 321mA. The buck converter turns on 115ms after the isolation MOSFET turns on fully.

Undervoltage Lockout

The devices operate with up to a 60V supply voltage with a turn-on UVLO threshold (V_{ON}) at 38.7V (typ), and a turn-off UVLO threshold (V_{OFF}) at 31.4V (typ). When the input voltage is above V_{ON}, the device enters power mode and the internal isolation MOSFET is turned on. When the input voltage is below V_{OFF} for more than t_{OFF_DLY}, the MOSFET and the buck converter are off.

LED Driver

The devices drive an LED, or multiple LEDs in series, with a maximum LED voltage of 6.5V. In sleep mode and ultra-low power mode, the LED current is pulse width modulated with a duty cycle of 25% and the amplitude is set by $R_{\overline{SL}}$. The LED driver current amplitude is programmable from 10mA to 20mA using $R_{\overline{SL}}$ according to the formula:

$$I_{LED} = 646/R_{\overline{SL}}\ (mA)$$

where $R_{\overline{SL}}$ is in kΩ.

Sleep and Ultra-Low Power Modes

The devices feature a sleep mode and an ultra-low power mode in which the internal p-channel isolation MOSFET is kept on and the buck regulator is off. In sleep mode, the LED driver output (LED) pulse width modulates the LED current with a 25% duty cycle. The peak LED current (I_{LED}) is set by an external resistor $R_{\overline{SL}}$. To enable sleep mode, apply a falling edge to $\overline{SL}$ with $\overline{ULP}$ disconnected or high impedance. Sleep mode can only be entered from wake mode.

Ultra-low power mode allows the devices to reduce power consumption lower than sleep mode, while maintaining the power signature of the IEEE standard. The ultra-low power-mode enable input $\overline{ULP}$ is internally held high with a 50kΩ pullup resistor to the internal 5V bias of the device. To enable ultra-low power mode, apply a falling edge to $\overline{SL}$ with $\overline{ULP}$ = LOW. Ultra-low power mode can only be entered from wake mode.

To exit from sleep mode or ultra-low power mode and resume normal operation, apply a falling edge on the wake-mode enable input ($\overline{WK}$).

Thermal-Shutdown Protection

If the devices' die temperature reaches 151°C, an overtemperature fault is generated and the device shuts down. The die temperature must cool down below +127°C to remove the overtemperature fault condition. After a thermal shutdown condition clears, the device is reset.

WAD Description

For applications where an auxiliary power source such as a wall power adapter is used to power the PD, the devices feature wall power adapter detection.

The wall power adapter is connected from WAD to PGND. The devices detect the wall power adapter when the voltage from WAD to PGND is greater than 8.8V. When a wall power adapter is detected, the internal isolation MOSFET is turned off, classification current is disabled.

Connect the auxiliary power source to WAD, connect a diode from WAD to V_{DD}, and connect a diode from WAD to V_{CC}. See the typical application circuit in Figures 3 and 4.

The application circuit must ensure that the auxiliary power source can provide power to V_{DD} and V_{CC} by means of external diodes. The voltage on V_{DD} must be within the V_{DD} voltage range to allow the DC-DC to operate. To allow operation of the DC-DC converter, the V_{DD} and V_{CC} voltage must be greater than 8V, on the rising edge, while on the falling edge the V_{DD} and V_{CC} may fall down to 7.7V keeping the DC-DC converter on.

Note: When operating solely with a wall power adapter, the WAD voltage must be able to meet the condition V_{DD} > 8V, that likely results in WAD > 8.8V.

Internal Linear Regulator and Back Bias

An internal voltage regulator provides VDRV to internal circuitry. The VDRV output is filtered by a 1µF capacitor connected from VDRV to GND. The regulator is for internal use only and cannot be used to provide power to external circuits. VDRV can be powered by either V_{DD} or V_{AUX}, depending on V_{AUX}. The internal regulator is used for both PD and buck converter operations.

V_{OUT} can be used to back bias the VDRV voltage regulator if V_{OUT} is greater than 4.75V. Back biasing VDRV increases device efficiency by drawing current from V_{OUT} instead of V_{DD}. If V_{OUT} is used as back bias, connect AUX directly to V_{OUT}. In this configuration, the VDRV source switches from V_{DD} to V_{AUX} after the buck converter's output has reached its regulation voltage.

Cable Discharge Event Protection (CDE)

A 70V voltage clamp is integrated to protect the internal circuits from a cable discharge event.

DC-DC Buck Converter

The DC-DC buck converter uses a PWM, peak current-mode, fixed-frequency control scheme providing an easy-to-implement architecture without sacrificing a fast transient response. The buck converter operates in a wide input voltage range from 8V to 60V and supports up to 6.49W of output power at 1.3A load. The devices provide a wide array of protection features including UVLO, overtemperature shutdown, short-circuit protection with hiccup runaway current limit, cycle-by-cycle peak current protection, and cycle-by-cycle output overvoltage protection, for enhanced performance and reliability. A frequency foldback scheme is implemented to reduce the switching frequency to half at light loads to increase the efficiency.

Frequency Foldback Protection for High-Efficiency Light-Load Operation

The devices enter frequency foldback mode when eight consecutive inductor current zero-crossings occur. The switching frequency is 430kHz under loads large enough that the inductor current does not cross zero. In frequency foldback mode, the switching frequency is reduced

to 215kHz to increase power conversion efficiency. The device returns to normal mode when the inductor current does not cross zero for eight consecutive switching periods. Frequency foldback mode is forced during startup until 50% of the soft-start is completed.

Hiccup Mode

The devices include a hiccup protection feature. When hiccup protection is triggered, the devices turn off the high-side and turn on the low-side MOSFET until the inductor current reaches the valley current limit. The control logic waits 77ms until attempting a new soft-start sequence. Hiccup mode is triggered if the current in the high-side MOSFET exceeds the runaway current-limit threshold, both during soft-start and during normal operating mode. Hiccup mode can also be triggered in normal operating mode in the case of an output undervoltage event. This happens if the regulated feedback voltage drops below 60% (typ).

$\overline{\text{RESET}}$ Output

The devices feature an open-drain $\overline{\text{RESET}}$ output that indicates if either the LDO or the switching regulator drop out of regulation. The $\overline{\text{RESET}}$ output goes low if either regulator drops below 92% of its regulated feedback value. $\overline{\text{RESET}}$ goes high impedance 100µs after both regulators are above 95% of their value.

Maintain Power Signature (MPS)

The devices feature the MPS to comply with the IEEE 802.3af standard. It is able to maintain a minimum current (10mA) of the port to avoid the power disconnection from the PSE. The devices enter MPS mode when the port current is lower than 14mA and also exit the MPS mode when the port current is greater than 40mA. The feature is enabled by connecting the MPS pin to VDRV, or disabled by connecting the MPS pin to GND.

Applications Information

Operation with Wall Adapter

For applications where an auxiliary power source such as a wall power adapter is used to power the PD, the devices feature wall power adapter detection. The device gives priority to the WAD supply over V_{DD} supply, and smoothly switches the power supply to WAD when it is detected. The wall power adapter is connected from WAD to PGND. The devices detect the wall power adapter when the voltage from WAD to PGND is greater than 8.8V. When a wall power adapter is detected, the internal isolation MOSFET is turned off, classification current is disabled and the device draws power from the auxiliary power source through V_{CC}. Connect the auxiliary power source to WAD, connect a diode from WAD to V_{CC}. See the typical application circuit in Figures 3 and 4.

Adjusting LDO Output Voltage

An uncommitted LDO regulator is available to provide a supply voltage to external circuits. A preset voltage of 3.3V is set by connecting LDO_FB directly to VDRV. For different output voltages connect a resistor divider from LDO_OUT and LDO_FB to GND. The total feedback resistance should be in the range of 100kΩ. The maximum output current is 85mA and thermal considerations must be taken to prevent triggering thermal shutdown. The LDO regulator can be powered by VOUT, a different power supply, or grounded when not used. The LDO is enabled once the buck converter has reached the regulation voltage. The LDO is disabled when the buck converter is turned off or not regulating.

Adjusting Buck Converter Output Voltage

The buck converter output voltage is set by changing the feedback resistor-divider ratio. The output voltage can be set from 3.0V to 5.6V (MAX5991A) or 5.4V to 14V (MAX5991B). The FB voltage is regulated to 1.226V. Keep the trace from the FB pin to the center of the resistive divider short, and keep the total feedback resistance around 100kΩ.

Inductor Selection

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_S \times V_{IN} \times L_{IR} \times I_{OUT(MAX)}}$$

where L_{IR} is the ratio of the inductor ripple current to full load current at the minimum duty cycle. Choose LIR between 20% to 40% for best performance and stability. Use an inductor with the lowest possible DC resistance that fits in the allotted dimensions. Powdered iron ferrite core types are often the best choice for performance. With any core material, the core must be large enough not to saturate at the current limit of the devices.

V_{CC} Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The total input capacitance must be equal or greater than the value given by the following equation to keep the input-ripple voltage within specification and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN_MIN} = \frac{D \times T_S \times I_{OUT}}{V_{IN-RIPPLE}}$$

where $V_{IN-RIPPLE}$ is the maximum allowed input ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage. D is the duty cycle (V_{OUT}/V_{IN}) and T_S is the switching period ($1/f_S$).

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source, but are instead shunted through the input capacitor. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} is the input RMS ripple current.

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output-voltage ripple due to the output capacitance, ESR, and ESL:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL$$

or

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$$

or whichever is larger. The peak-to-peak inductor current (I_{P-P})

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial output capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output-voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

Load-transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x I_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value.

Table 1. Design Selection Table

OUTPUT (V)	C_{IN}		C_{OUT}	L	CLASS
	CERAMIC	ELECTROLYTIC	CERAMIC		
3.3	2.2µF/100V	10µF/63V	2 x 22µF/6.3V	15µH/1.7A	1
5	2.2µF/100V	10µF/63V	2 x 22µF/6.3V	22µH/1.7A	1 or 2
12	2.2µF/100V	10µF/63V	2 x 10µF/16V	100µH/0.8A	1 or 2

PCB Layout

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX5991A EV kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
2) Place capacitors on V_{DD}, V_{CC}, AUX, VDRV as close as possible to the IC and its corresponding pin using direct traces. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect V_{DD}, V_{CC}, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
6) Route high-speed switching nodes, such as LX, away from sensitive analog areas (FB).
7) Place enough vias in the pad for the EP of the devices so that heat generated inside can be effectively dissipated by the PCB copper. The recommended spacing for the vias is 1mm to 1.2mm pitch. The thermal vias should be plated (1oz copper) and have a small barrel diameter (0.3mm to 0.33mm).

Typical Application Circuits

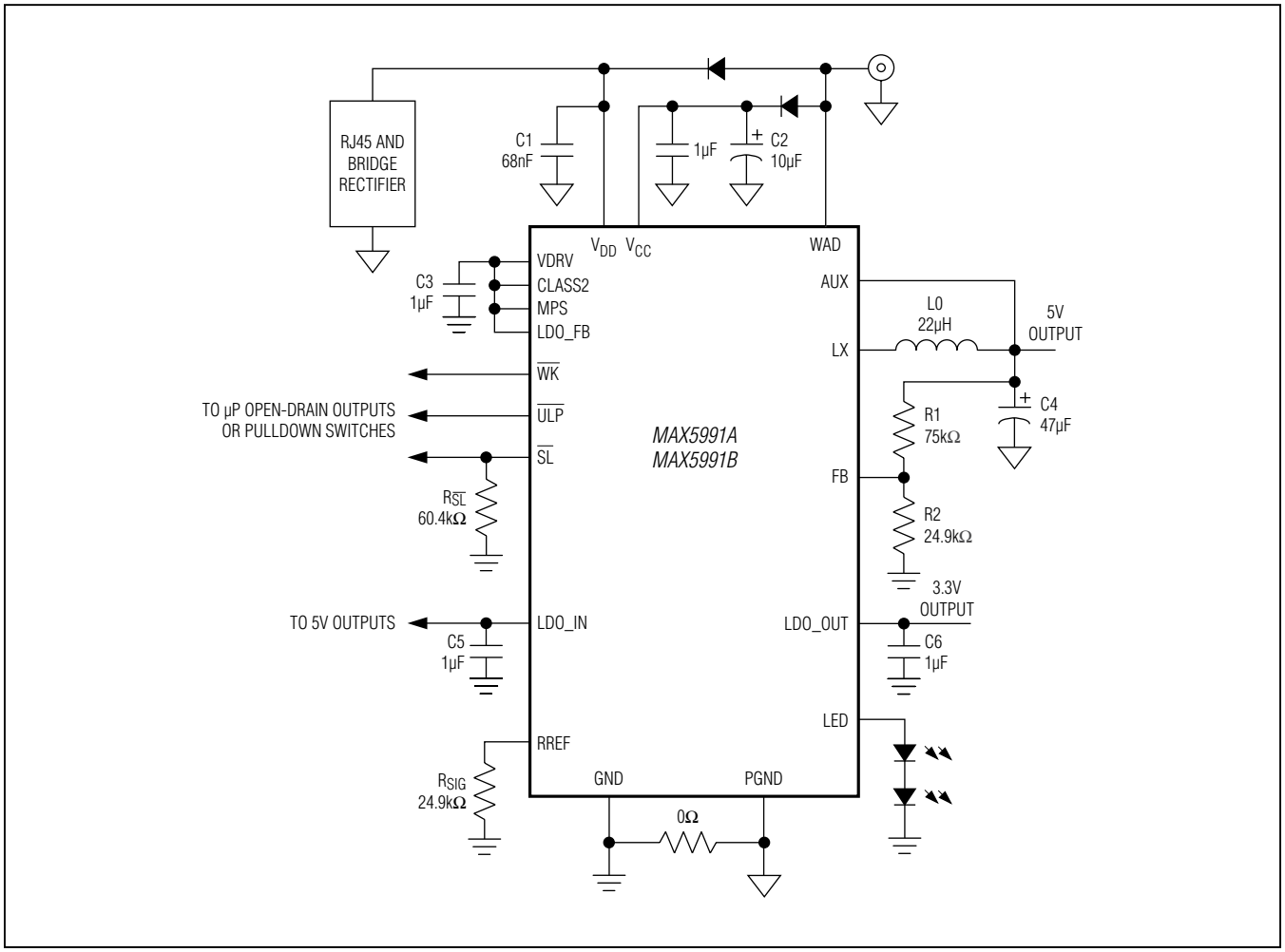


Figure 3. MAX5991A/MAX5991B 5V Buck Regulator and Fixed LDO Output

Typical Application Circuits (continued)

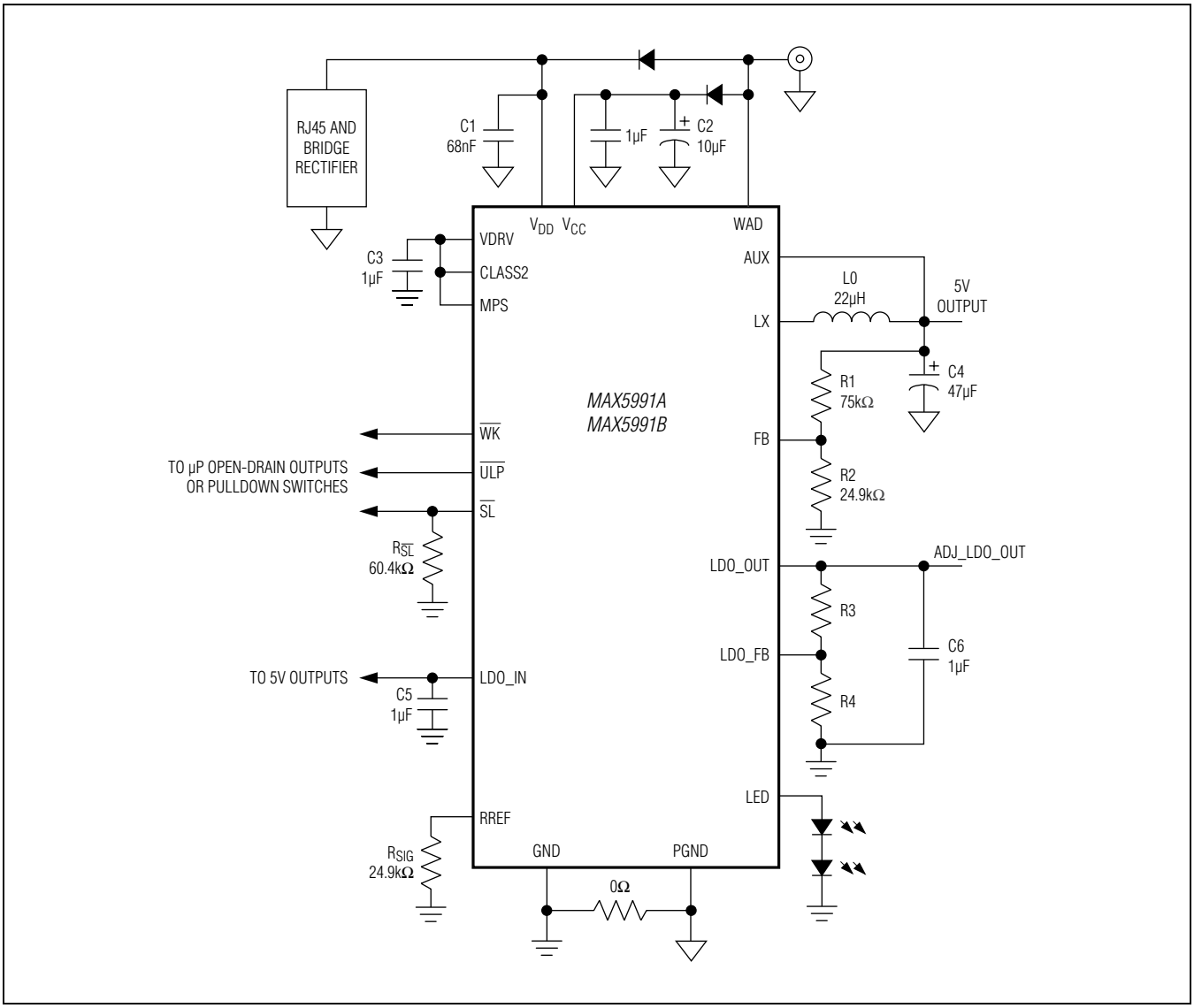
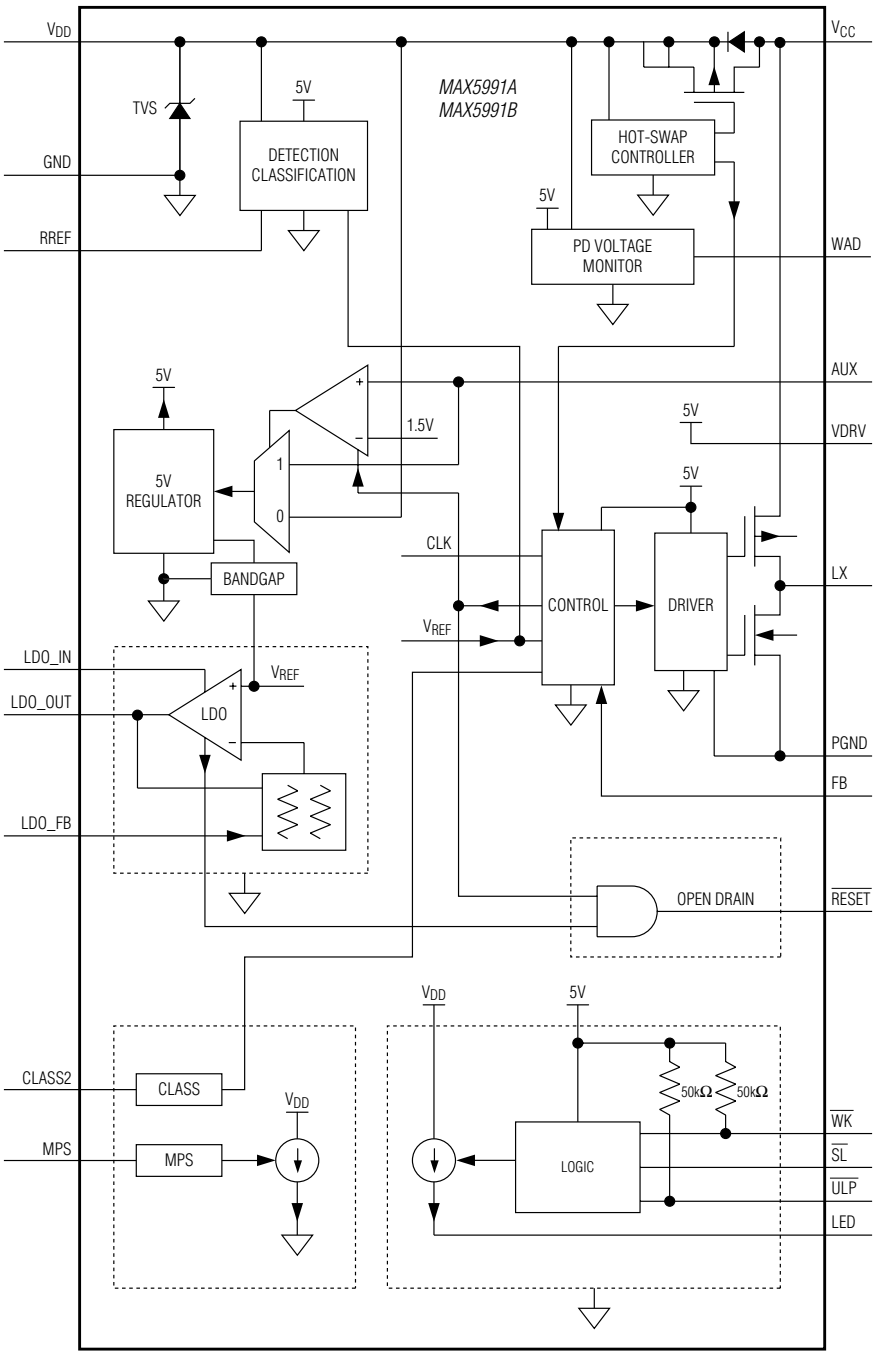


Figure 4. MAX5991A/MAX5991B 5V Buck Regulator and Adjustable LDO Output

Functional Diagram



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP	T2044+4	21-0139	90-0409

Ordering Information

PART	PIN-PACKAGE	SLEEP/ULP MODE	LDO	UVLO (V)	$\overline{\text{RESET}}$	MPS/CLASS2	$\text{OUTPUT}_{\text{ADJ}}$
MAX5991AETP+	20 TQFN-EP*	Yes	Yes	38.7	Yes	Yes	Yes
MAX5991BETP+	20 TQFN-EP*	Yes	Yes	38.7	Yes	Yes	Yes

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/12	Initial release	—
1	1/13	Changed land pattern number	21
2	1/15	Updated *Benefits and Features* section	1

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