

Programmable Quick Turn Clock™

FEATURES

- · Advanced programmable PLL design
- Very low Jitter and Phase Noise (30-70ps Pk-Pk typical)
- Up to 2 programmable outputs
- Output frequency up to 35MHz CMOS.
- Accepts Crystal clock input
 - o Fundamental crystal: 10MHz-30MHz
 - o Reference input: Up to 100MHz
- Single 2.5V or 3.3V ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin SOT Green/RoHS compliant Pkg.

DESCRIPTION

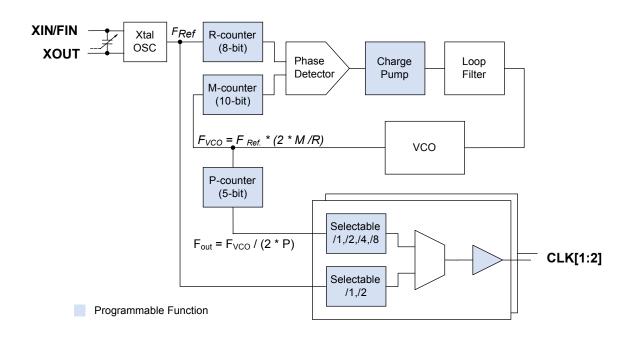
The PL611-05 is a low-cost general purpose frequency synthesizer and a member of PhaseLink's Programmable 'Quick Turn Clock (QTC)' family. PhaseLink's PL611-05 offers generating two system clock frequencies of up to 35MHz form a 10-30MHz fundamental crystal or a Reference clock source. Cascading of the ICs to produce additional clock frequencies is also supported.

PIN DESCRIPTION

PIN CONFIGURATION

Name	Pin #	Туре	Description
CLK1	1	0	Programmable Clock Output
GND	2	Р	GND connection
XIN/FIN	3	1	Crystal or Ref. input pin
XOUT	4	0	Crystal output pin
CLK2	5	В	Programmable Clock or Reference Output
VDD	6	Р	VDD connection

BLOCK DIAGRAM





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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	4.6	V
Input Voltage Range	Vı	-0.5	V _{DD} +0.5	V
Output Voltage Range	Vo	-0.5	V _{DD} +0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	Ts	-65	150	°C
Ambient Operating Temperature		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

AC SPECIFICATIONS

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency(XIN)	Fundamental Crystal	10		30	MHz
Input (FIN) Frequency				100	MHz
Input (FIN) Signal Amplitude	Internally AC coupled	0.9		VDD	Vpp
Settling Time	At power-up (after VDD increases over 1.62V)			10	ms
Output Dies Tiese	15pF Load, 10/90%VDD, Standard drive		2.5	3.5	ns
Output Rise Time	15pF Load, 10/90%VDD, High drive		1.0	1.5	ns
Output Fall Time	15pF Load, 90/10%VDD, Standard drive		2.5	3.5	ns
	15pF Load, 90/10%VDD, High drive		1.0	1.5	ns
Duty Cycle	At VDD/2	45	50	55	%
Period Jitter, peak-to-peak* (measured from 10,000 samples)	With capacitive decoupling between VDD and GND. Operating only one output.		70		ps

^{*} Note: Jitter performance depends on the programming parameters.



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DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Outputs	I _{DD}	At 10MHz, load=15pF			15	mA
Operating Voltage	V_{DD}		2.25		3.63	V
Output Low Voltage	V _{OL}	I _{OL} = +4mA Standard drive			0.4	V
Output High Voltage	Vон	I _{OH} = -4mA Standard drive	V _{DD} – 0.4			V
Output Current, Standard drive	losp	V _{OL} = 0.4V, V _{OH} = 2.4V			10.7	mA
Output Current, High drive	Гонд	V _{OL} = 0.4V, V _{OH} = 2.4V			24	mA
Short-circuit Current	Is			±50		mA

CRYSTAL SPECIFICATIONS

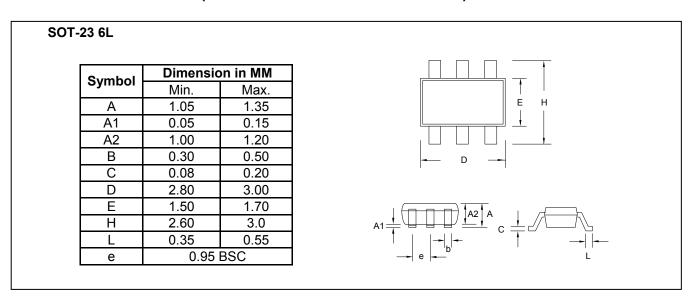
PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Fundamental Crystal Resonator Frequency	Fxin	10		30	MHz
Crystal Loading Rating (The IC can be programmed for any value in this range.)	C _{L (xtal)}	5	16*	20	pF
Maximum Sustainable Drive Level				500	μW
Operating Drive Level			100		μW
Crystal Shunt Capacitance	C0			6	pF
Effective Series Resistance, Fundamental, 10-30MHz	ESR			30	Ω

Note: C_L = 16pF is used when not specified. A detailed crystal specification document is also available for this part.

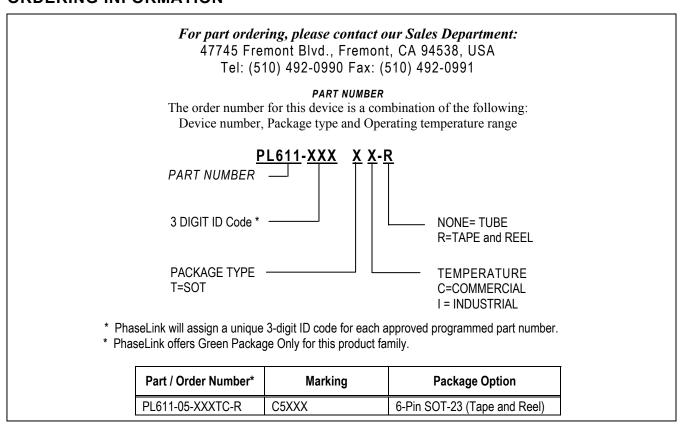


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PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)



ORDERING INFORMATION



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