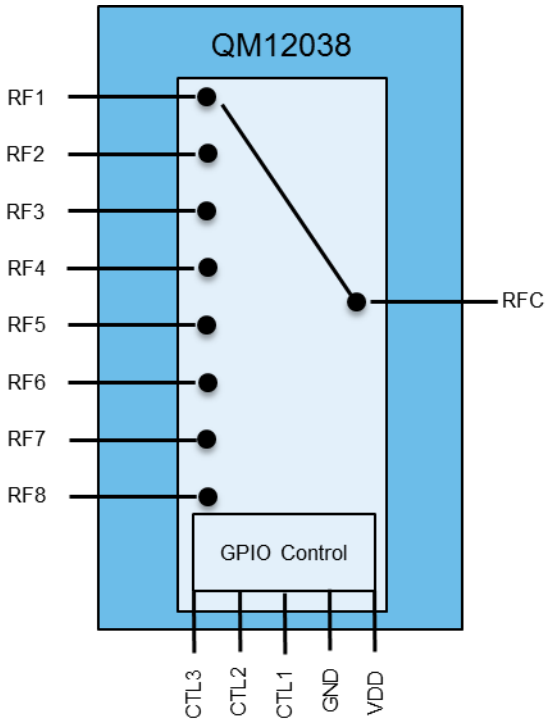
QM12038

SP8T Switch For 3G/4G Applications

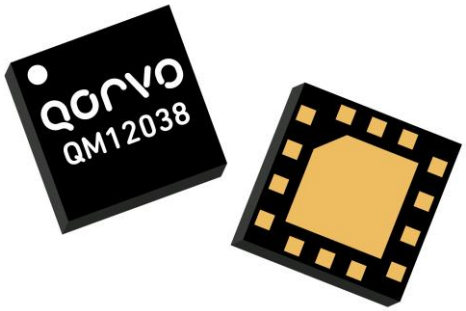
Product Description

The QM12038 is a low loss, high isolation SP8T switch with performance optimized for CDMA, WCDMA & LTE applications requiring high linearity. The QM12038 is compatible with +1.3V control logic, which is a key requirement for most cellular transceivers. This part is packaged in a compact 2mm x 2mm, 15-pin, Module package which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram



Top View



15 Pin 2 x 2 x 0.57 mm Module Package

Feature Overview

- Excellent insertion loss and isolation performance
  - 0.5dB Typ IL, Band 5
  - 40dB Typ Isolation, Band 5
- Multi-Band operation 700MHz to 2700MHz
- GPIO compatible to 1.8V typ (1.3V min)
- Power handling +32dBm, 50Ω
- Compact 2mm x 2mm, Module package
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

Applications

- Cellular Handset Applications
- Cellular Modems and USB Devices
- Multi-Mode WCDMA, and LTE Applications

Ordering Information

PART NO.	DESCRIPTION
QM12038SB	5-pc Sample Bag
QM12038SR	100-pc, 7” Reel
QM12038TR13-5K	5000-pc, 13” Reel
QM12038PCK410	Fully Assembled EVB and 5-pc Sample Bag

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-45 to +125 °C
Operating Temperature	-30 to +90°C
V_{DD}	6.0 V
C_{TL1}, C_{TL2}, C_{TL3}	3.0 V
Maximum Input Power	
Momentary Infrequent Occurrence	35 dBm, 1:1 VSWR 33 dBm, 6:1 VSWR
Continuous Operation	32 dBm, 1:1 VSWR 30 dBm, 6:1 VSWR

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD} Supply Voltage	2.4	2.85	4.5	V
V_{DD} Supply Current		80	120	µA
C_{TL} Logic Low Voltage	0.00	0.00	0.45	V
C_{TL} Logic High Voltage	1.3	1.8	2.7*	V
C_{TL} Logic High Current		0.1	5	µA
Turn-On Time		4		µs
Switching Speed			2	µs

* V_{DD} Must be > V_{CTL} at all times

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{DD} = 2.85V, V_{HIGH}/V_{LOW} = 1.8V/0V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RFx to RFC	698MHz to 960MHz		0.52		dB
RFx to RFC	1710MHz to 1980MHz		0.68		dB
RFx to RFC	2110MHz to 2170MHz		0.71		dB
RFx to RFC	2300MHz to 2690MHz		0.85		dB
Harmonics					
Low Band, 2fo	Pin = +28dBm, 50Ω, fo= 824MHz		-98		dBc
Low Band, 3fo	Pin = +28dBm, 50Ω, fo= 824MHz		-84		dBc
Mid Band, 2fo	Pin = +28dBm, 50Ω, fo= 1980MHz		-98		dBc
Mid Band, 3fo	Pin = +28dBm, 50Ω, f_o= 1980MHz		-84		dBc
High Band, 2fo	Pin = +28dBm, 50Ω, fo= 2570MHz		-97		dBc
High Band, 3fo	Pin = +28dBm, 50Ω, f_o= 2570MHz		-80		dBc
IIP2					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 1840 MHz at -15dBm Measured RX frequency @ 942.5MHz		117		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 3840 MHz at -15dBm Measured RX frequency @ 1960MHz		118		dBm
IIP3					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 852.5MHz at -15dBm Measured RX frequency @ 942.5MHz		68		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 1800MHz at -15dBm Measured RX frequency @ 1960MHz		67		dBm
VSWR	698MHz to 2690MHz		1.1		:1

Isolation Matrix Low Band (698MHz – 960MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		42	32	44	43	45	44	41
RF2	RF2	42		43	32	45	42	41	44
RF3	RF3	32	43		45	34	46	42	42
RF4	RF4	44	32	45		46	33	42	42
RF5	RF5	43	45	34	46		47	40	43
RF6	RF6	45	42	46	33	47		43	40
RF7	RF7	44	41	42	42	40	43		43
RF8	RF8	41	44	42	42	43	40	43	
RF1	RFC		43	42	41	41	41	34	33
RF2	RFC	42		42	41	41	41	34	33
RF3	RFC	42	43		41	41	41	34	33
RF4	RFC	42	43	42		41	41	34	33
RF5	RFC	42	43	42	41		41	34	33
RF6	RFC	42	43	42	41	41		34	33
RF7	RFC	42	43	42	41	41	41		33
RF8	RFC	42	43	42	41	41	41	34	

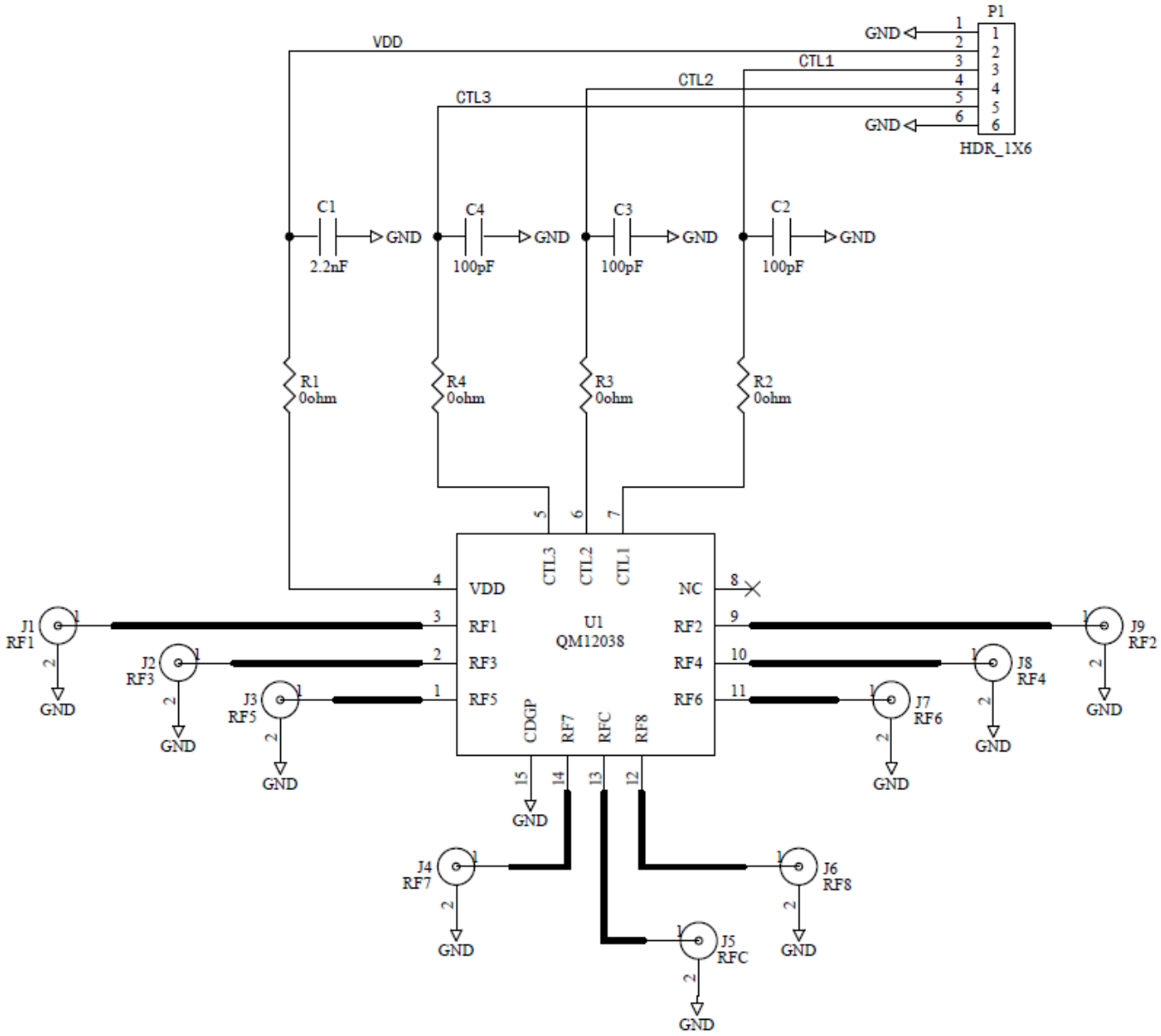
Isolation Matrix Mid Band (1710MHz – 2170MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		30	23	31	31	33	33	31
RF2	RF2	30		31	23	33	31	31	33
RF3	RF3	23	31		32	24	30	32	31
RF4	RF4	31	23	32		34	24	31	32
RF5	RF5	31	33	24	34		34	29	32
RF6	RF6	33	31	30	24	34		32	29
RF7	RF7	33	31	32	31	29	32		32
RF8	RF8	31	33	31	32	32	29	32	
RF1	RFC		33	32	32	32	31	25	25
RF2	RFC	31		32	32	32	31	25	25
RF3	RFC	31	33		32	32	31	25	25
RF4	RFC	31	33	32		32	31	25	25
RF5	RFC	31	33	32	32		31	25	25
RF6	RFC	31	33	32	32	32		25	25
RF7	RFC	31	33	32	32	32	31		25
RF8	RFC	31	33	32	32	32	31	25	

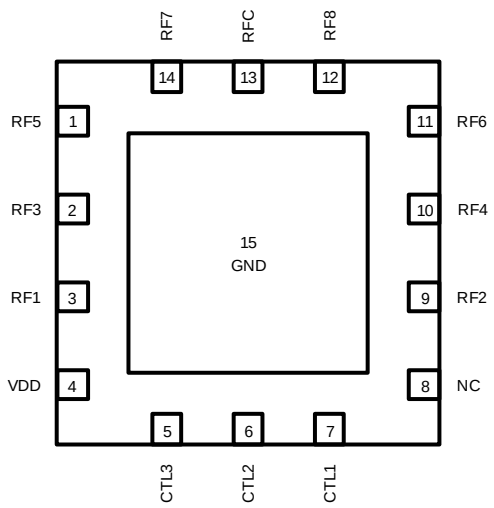
Isolation Matrix High Band (2300MHz – 2690MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		28	21	29	28	29	31	29
RF2	RF2	28		28	21	30	28	28	31
RF3	RF3	21	28		30	22	30	30	29
RF4	RF4	29	21	30		30	22	29	30
RF5	RF5	28	30	22	30		31	26	30
RF6	RF6	29	28	30	22	31		30	26
RF7	RF7	31	28	30	29	26	30		29
RF8	RF8	29	31	29	30	30	26	29	
RF1	RFC		30	29	28	29	29	21	21
RF2	RFC	30		29	28	29	29	21	21
RF3	RFC	30	30		28	29	29	21	21
RF4	RFC	30	30	29		29	29	21	21
RF5	RFC	30	30	29	28		29	21	21
RF6	RFC	30	30	29	28	29		21	21
RF7	RFC	30	30	29	28	29	29		21
RF8	RFC	30	30	29	28	29	29	21	

Application Circuit Schematic



Pin Configuration and Description



Top View

PIN NO.	LABEL	DESCRIPTION
1	RF5	RF Input / Output
2	RF3	RF Input / Output
3	RF1	RF Input / Output
4	V_{DD}	Power Supply
5	C_{TL3}	Control Logic #3
6	C_{TL2}	Control Logic #2
7	C_{TL1}	Control Logic #1
8	NC	No Connect
9	RF2	RF Input / Output
10	RF4	RF Input / Output
11	RF6	RF Input / Output
12	RF8	RF Input / Output
13	RFC	RF Common Input / Output
14	RF7	RF Input / Output
15	GND	RF and DC Ground

Control Logic

The Switch is controlled by C_{TL1}, C_{TL2}, and C_{TL3}.

LOGIC STATE	C_{TL1}	C_{TL2}	C_{TL3}
RF1-RFC	Low	Low	High
RF2-RFC	Low	Low	Low
RF3-RFC	High	High	Low
RF4-RFC	High	High	High
RF5-RFC	Low	High	Low
RF6-RFC	Low	High	High
RF7-RFC	High	Low	Low
RF8-RFC	High	Low	High

Power On and Off Sequence

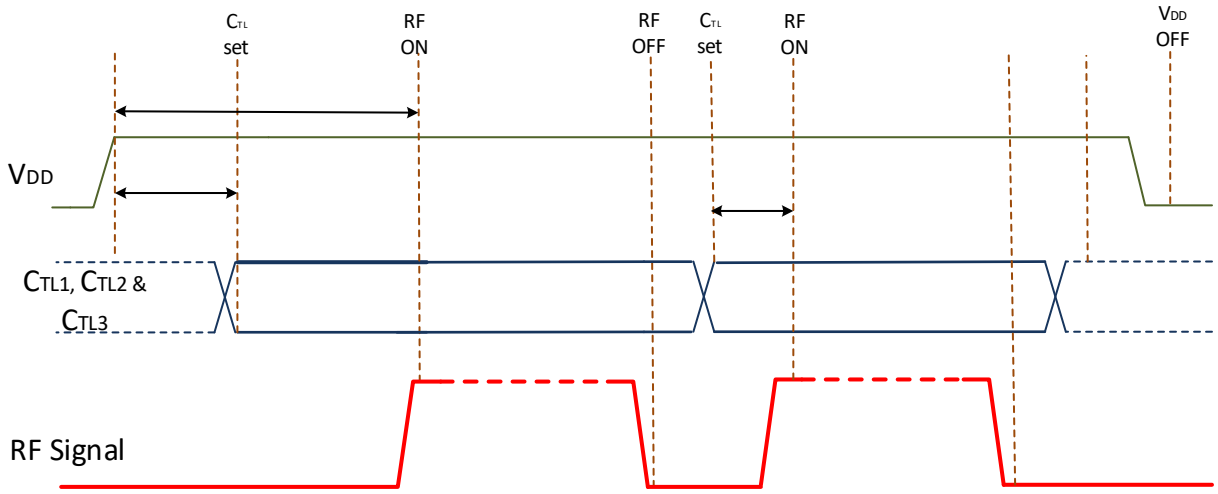
It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the part. First apply V_{DD} before applying a high to C_{TL1}, C_{TL2}, or C_{TL3}.

Power On –

1. Apply voltage supply – V_{DD}
2. Apply Logic signal – C_{TL1}, C_{TL2}, C_{TL3}
3. Apply the RF signal

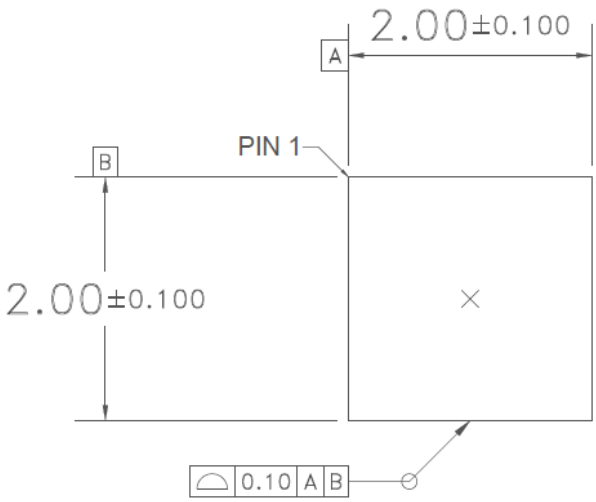
Power Off –

1. Remove the RF signal
2. Remove the logic signal – – C_{TL1}, C_{TL2}, C_{TL3}
3. Remove the voltage supply – V_{DD}

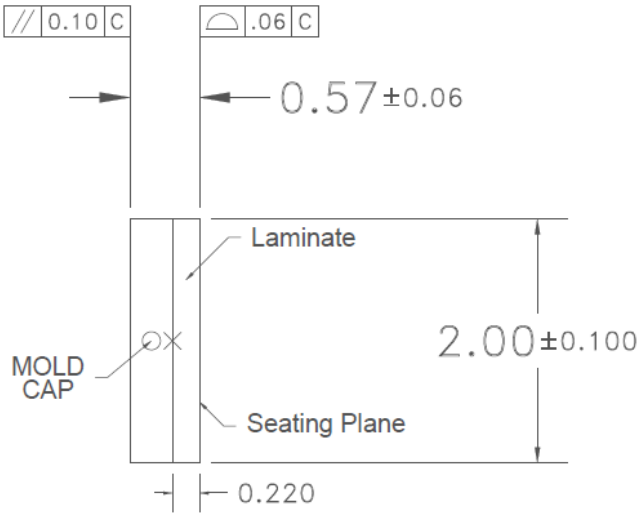


Mechanical Information

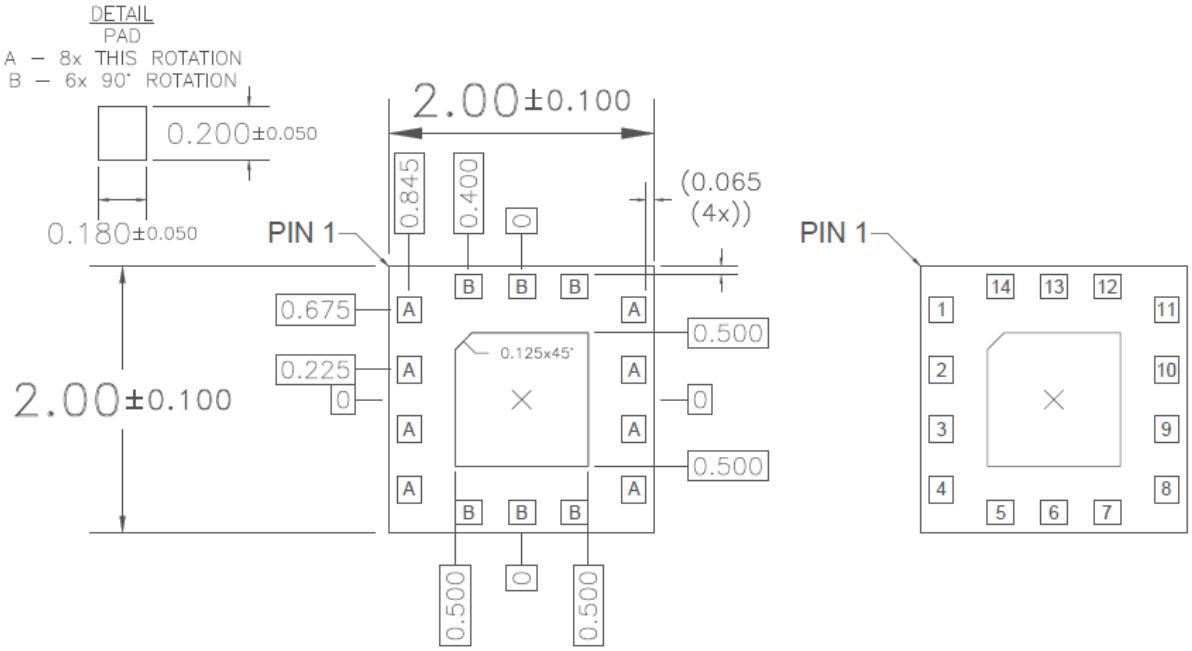
Package Drawing



Top View

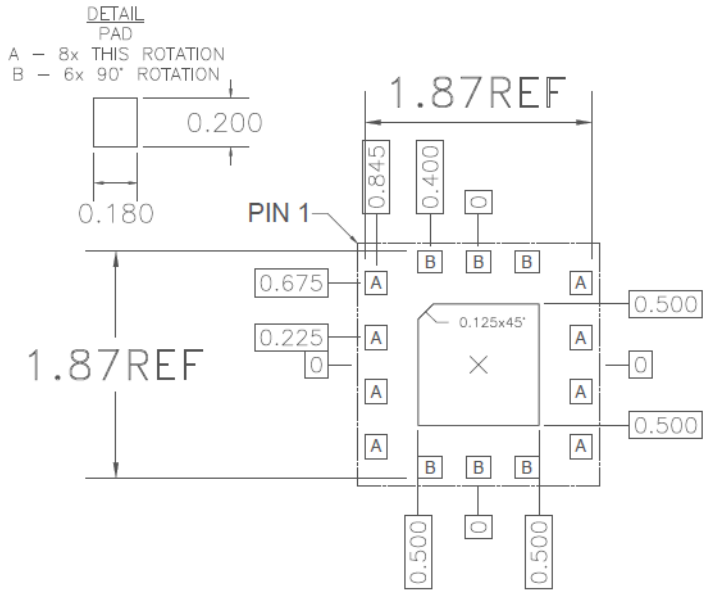


Side View

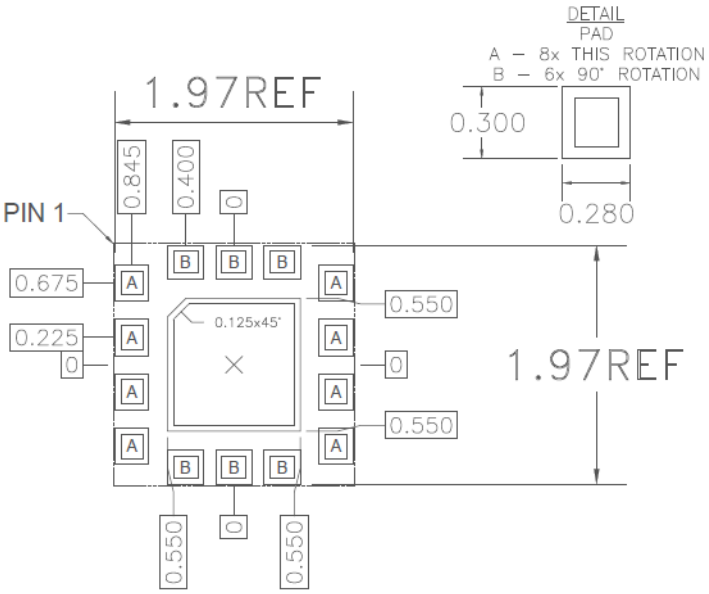


Top View X-Ray

PCB Design Requirements



Recommended Land Pattern



Recommended Land Pattern Mask

Notes:

1. All dimensions are in milimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 2	ESDA/JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Revision History

Revision Code	Date	Comments
B	03/01/2018	Initial Production Release
C	02/19/2020	Added Not Recommended For New Designs marks
D	06/15/2020	Removing NRND Marks

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
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