Low Noise Regulated Charge Pump DC-DC Converter

Description

The W-5200−5 are switched capacitor boost converters that deliver a low noise, regulated output voltage.

W-5200−5 gives a fixed regulated 5 V output.

The constant frequency 2 MHz charge pump allows small 1μF ceramic capacitors to be used.

Maximum output loads of up to 100 mA can be supported over a wide range of input supply voltages (2.7 V to 4.5 V) making the device ideal for battery−powered applications.

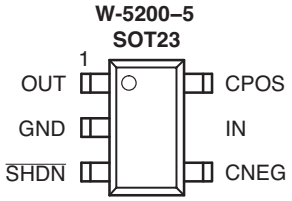
A shutdown control input allows the device to be placed in power−d own mode, reducing the supply current to less than 1μA.

In the event of short circuit or overload conditions, the device is fully protected by both foldback current limiting and thermal overload detection. In addition, a soft start, slew rate control circuit limits inrush current during power−up.

The W-5200−5 is a 6−lead, 1 mm max thin SOT23 package.

TSOT−23

PIN CONFIGURATIONS



(Top Views)

ORDERING INFORMATION

Device	Package	Shipping
W-5200TDI−GT3 (Note 1)	TSOT23−6 (Pb−Free)	3,000 / Tape & Reel

1. NiPdAu Plated Finish (RoHS−compliant).

Features

- Constant High Frequency (2 MHz) Operation
- 100 mA Output Current
- Regulated Output Voltage (5 V Fixed)
- Low Quiescent Current (1.7 mA Typ.)
- Input Voltage Operation down to 2.7 V
- Soft Start, Slew Rate Control
- Thermal Overload Shutdown Protection
- Low Value External Capacitors (1μF)
- Foldback Current Overload Protection
- Shutdown Current less than 1μA
- Low Profile (1 mm Thin) 6−l ead TSOT−2 3 Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

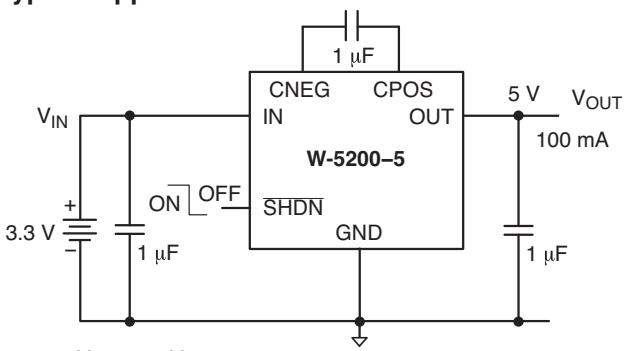
Applications

- 3 V to 5 V Boost Conversion
- White LED Driver
- USB On−The−Go 5 V Supply
- Local 5 V Supply from Lower Rail
- Battery Backup Systems
- Handheld Portable Devices

MARKING DIAGRAMS

VA = W-5200TDI-GT3
Y = Production Year (Last Digit)
M = Production Month (1-9, A, B, C or O, N, D)
R = Production Revision

Typical Application



V_{OUT} = 5 V
$I_{OUT} \leq 50$ mA, for $V_{IN} \geq 2.8$ V
$I_{OUT} \leq 90$ mA, for $V_{IN} \geq 3$ V

Figure 1. Typical Application – 5 V Output

Table 1. PIN DESCRIPTIONS

Designation	Description
OUT	Regulated output voltage.
GND	Ground reference for all voltages.
$\overline{SHDN}$	Shutdown control logic input (Active LOW)
CNEG	Negative connection for the flying capacitor.
IN	Input power supply.
CPOS	Positive connection for the flying capacitor. .

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{IN}, V_{OUT}, $\overline{SHDN}$, C_{NEG}, C_{POS} Voltage	–0.6 to +6.0	V
V_{OUT} Short Circuit Duration	Indefinite	
Output Current	200	mA
ESD Protection (HBM)	2000	V
Junction Temperature	150	°C
Storage Temperature Range	–65 to +160	°C
Lead Soldering Temperature (10 sec)	300	°C
Power Dissipation (SOT23–6)	0.3	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameters	Ratings	Units
V_{IN}	2.7 to 4.5	V
C_{IN}, C_{OUT}, C_{FLY}	1	μF
I_{LOAD}	0 to 100	mA
Ambient Temperature Range	–40 to +85	°C

Table 4. ELECTRICAL SPECIFICATIONS
(Recommended operating conditions unless otherwise specified. C_{IN}, C_{OUT}, C_{FLY} are 1 μF ceramic capacitors and V_{IN} is set to 3.6 V.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Regulated Output	$I_{LOAD} \le 40$ mA, $V_{IN} \ge 2.7$ V $I_{LOAD} \le 100$ mA, $V_{IN} \ge 3.1$ V	4.8	5.0	5.2	V
V_{LINE}	Line Regulation	3.1 V $\le V_{IN} \le$ 4.5 V, I_{LOAD} = 50 mA		6		mV
V_{LOAD}	Load Regulation	I_{LOAD} = 10 mA to 100 mA, V_{IN} = 3.6 V		20		mV
F_{OSC}	Switching Frequency		1.3	2.0	2.6	MHz
V_R	Output Ripple Voltage	I_{LOAD} = 100 mA W-5200–5 Only		30		mVp–p
η	Efficiency	I_{LOAD} = 50 mA, V_{IN} = 3 V, W-5200–5		80		%
I_{GND}	Ground Current	I_{LOAD} = 0 mA, $\overline{SHDN}$ = V_{IN}		1.6	4	mA
I_{SHDN}	Shutdown Input Current	I_{LOAD} = 0 mA, $\overline{SHDN}$ = 0 V to V_{IN}			1	μA
R_{OL}	Open–Loop Resistance	I_{LOAD} = 100 mA, V_{IN} = 3 V (Note 1)		10		Ω
T_{ON}	V_{OUT} Turn–on time (10% to 90%)	I_{LOAD} = 0 mA, V_{IN} = 3 V		0.5		ms
V_{IHSHDN}	High Detect Shutdown Threshold			0.8	1.3	V
V_{ILSHDN}	Low Detect Shutdown Threshold		0.4			V
I_{ROUT}	Reverse Leakage into OUT pin	V_{OUT} = 5 V, Shutdown mode (Note 2)		15	30	μA
I_{SC}	Short–circuit Output	V_{OUT} = 0 V		80		mA
T_{SD}	Thermal Shutdown			160		°C
T_{HYST}	Thermal Hysteresis			20		°C

1. $R_{OL} = (2V_{IN} - V_{OUT})/I_{OUT}$
2. In the event of a controlled shutdown, the output will be isolated from the input, but will remain connected to the internal resistor feedback network. This will cause a small level of reverse current to flow back into the device to ground.

TYPICAL PERFORMANCE CHARACTERISTICS (W-5200–5)

(T_{AMB} = 25°C, C_{IN} = C_{OUT} = C_{FLY} = 1 μF, V_{IN} = 3.3 V unless specified otherwise.)

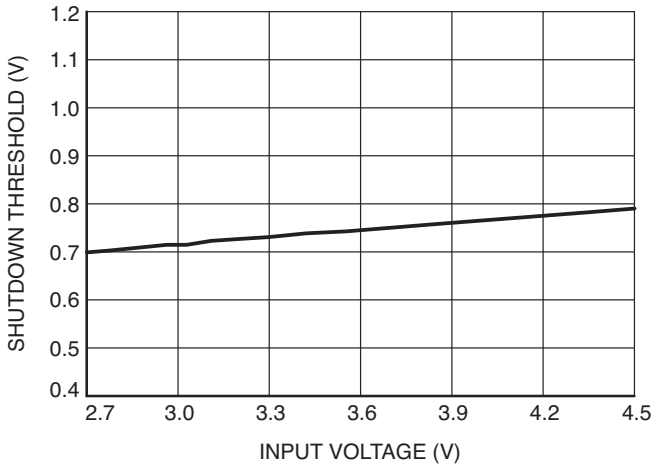


Figure 2. Shutdown Input Threshold vs. Supply Voltage

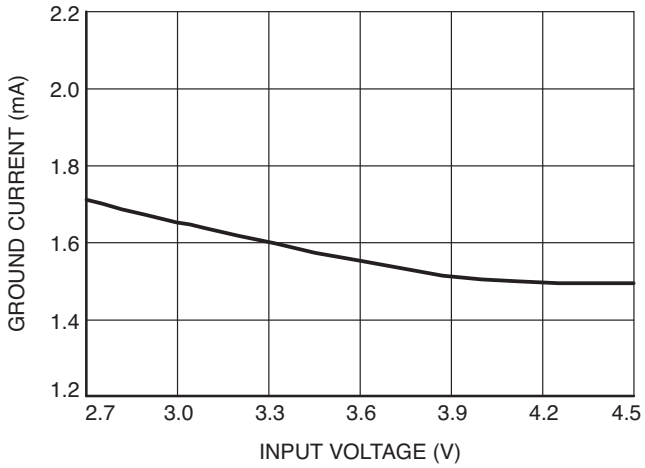


Figure 3. Ground Current vs. Supply Voltage (No Load)

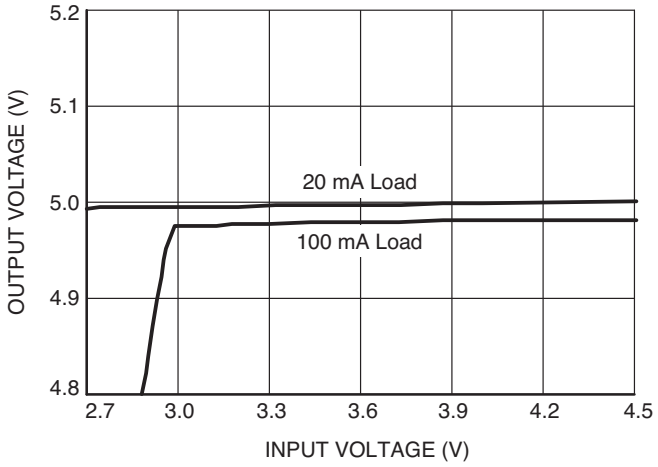


Figure 4. Line Regulation

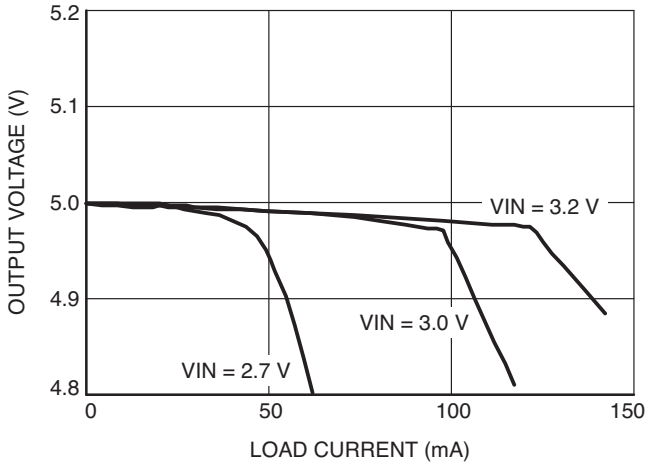


Figure 5. Load Regulation

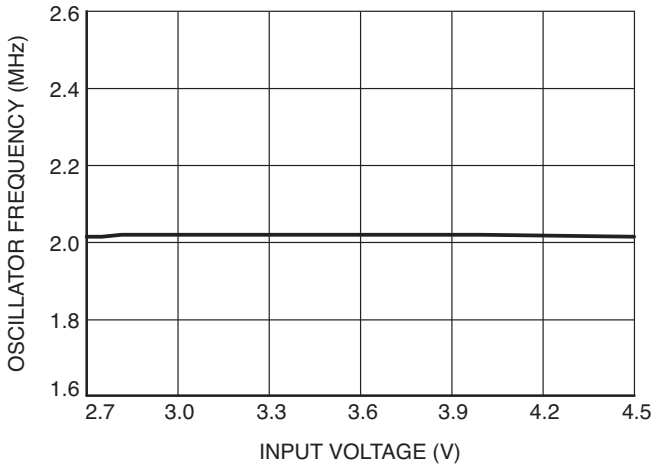


Figure 6. Oscillator Frequency vs. Supply Voltage

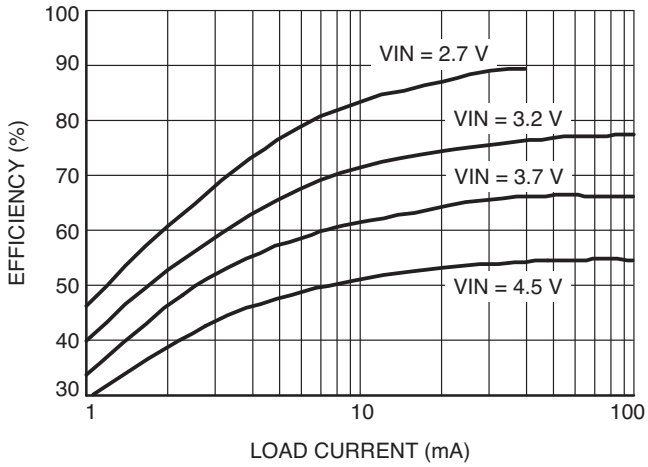


Figure 7. Efficiency vs. Load Current

TYPICAL PERFORMANCE CHARACTERISTICS (W-5200–5)

(T_{AMB} = 25°C, C_{IN} = C_{OUT} = C_{FLY} = 1 μF, V_{IN} = 3.3 V unless specified otherwise.)

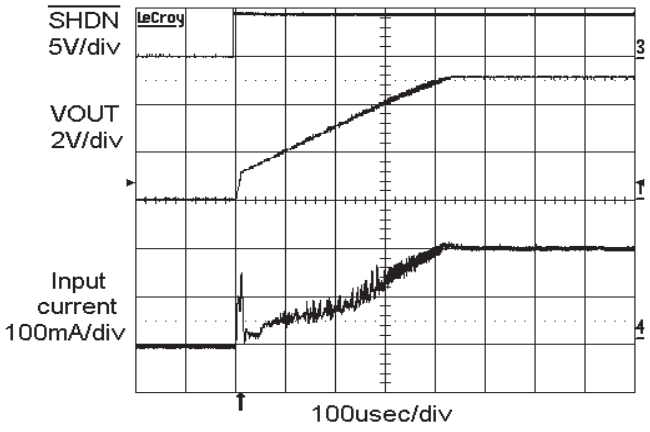


Figure 8. Soft Start Power Up (90 mA Load, 3.3 V Input)

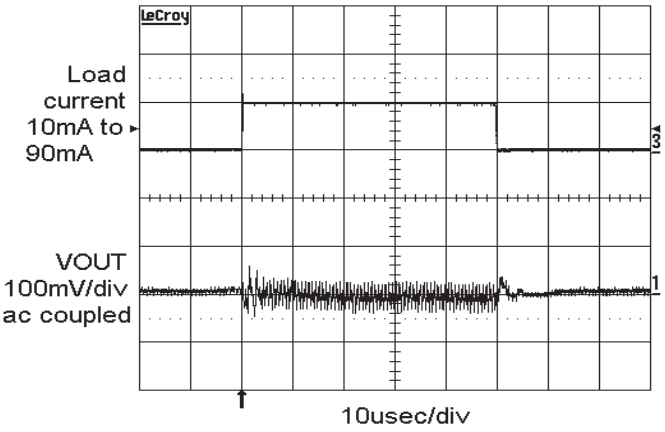


Figure 9. Load Step Response (3.3 V Input)

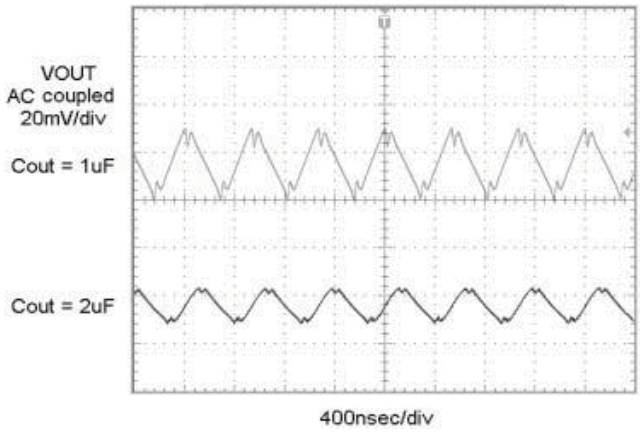


Figure 10. Output Ripple (100 mA Load, 3.3 V Input)

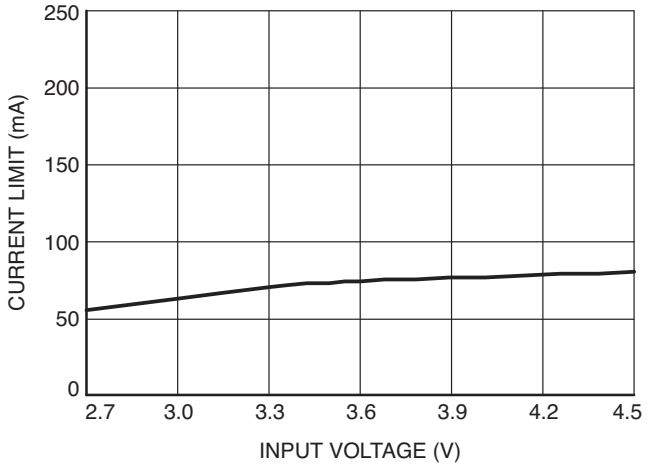


Figure 11. Short Circuit Current vs. Supply Voltage

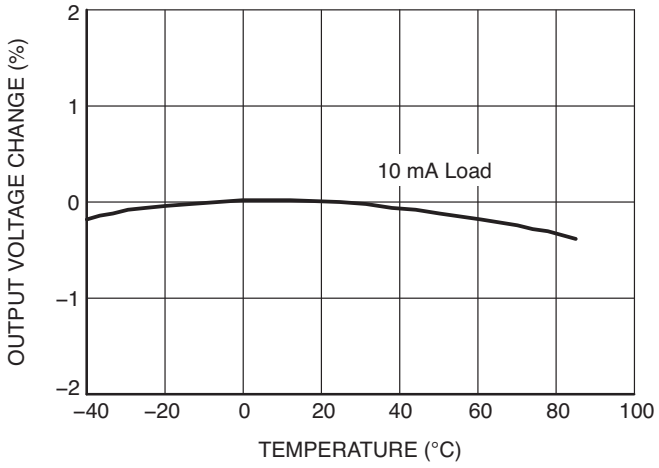


Figure 12. Output Voltage Change vs. Temperature

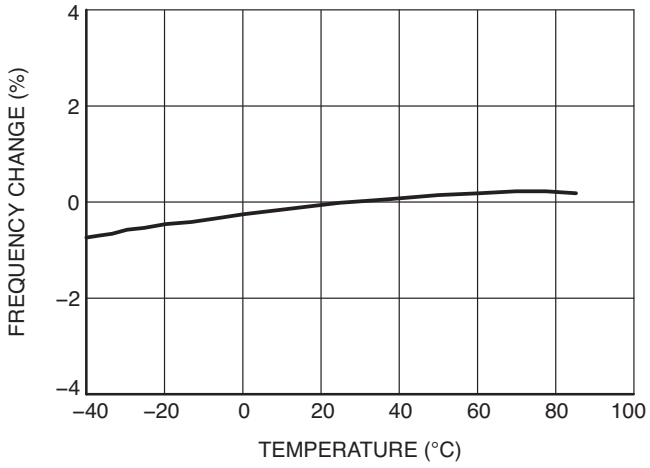


Figure 13. Oscillator Frequency Change vs. Temperature

Block Diagram

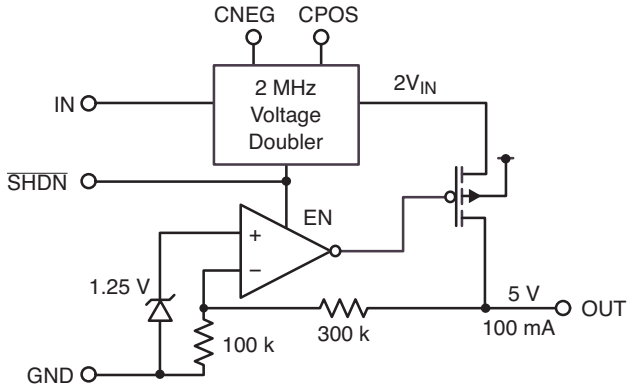


Figure 14 . W-5200–5 5 V Fixed Output

Pin Functions

IN is the power supply. During normal operation the device draws a supply current which is almost constant. A very brief interval of non–conduction will occur at the switching frequency. The duration of the non–conduction interval is set by the internal non–overlapping “break–before–make” timing. IN should be bypassed with a 1 μF to 4.7 μF low ESR (Equivalent Series Resistance) ceramic capacitor

For filtering, a low ESR ceramic bypass capacitor (1 μF) in close proximity to the IN pin prevents noise from being injected back into the power supply.

$\overline{\text{SHDN}}$ is the logic control input (Active LOW) that places the device into shutdown mode. The internal logic is CMOS and the pin does not use an internal pull–down resistor. The $\overline{\text{SHDN}}$ pin should not be allowed to float.

CPOS, CNEG are the positive and negative connections respectively for the charge pump flying capacitor. A low ESR ceramic capacitor (1 μF) should be connected between these pins. During initial power–up it may be possible for the capacitor to experience a voltage reversal and for this reason, avoid using a polarized (tantalum or aluminum) flying capacitor.

OUT is the regulated output voltage to power the load. During normal operation, the device will deliver a train of current pulses to the pin at a frequency of 2 MHz. Adequate filtering on the pin can typically be achieved through the use a low ESR ceramic bypass capacitor (1 μF to 4.7 μF) in close proximity to the OUT pin. The ESR of the output capacitor will directly influence the output ripple voltage.

When the shutdown mode is entered, the output is immediately isolated from the input supply, however, the output will remain connected to the internal feedback resistor network (400 kΩ). The feedback network will result in a reverse current of 10 μA to 20 μA to flow back through the device to ground.

Whenever the device is taken out of shutdown mode, the output voltage will experience a slew rate controlled power–up. Full operating voltage is typically achieved in less than 0.5 msec.

GND is the ground reference for all voltages on W-5200–5 devices.

Device Operation

The W-5200−5 use a switched capacitor charge pump to boost the voltage at IN to a regulated output voltage. Regulation is achieved by sensing the output volatage through an internal resistor divider (W-5200−5) and modulating the charge pump output current based on the error signal. A 2−phase non−overlapping clock activates the charge pump switches. The flying capacitor is charged from the IN voltage on the first phase of the clock. On the second phase of the clock it is stacked in series with the input voltage and connected to OUT. The charging and discharging the flying capacitor continues at a free running frequency of typically 2 MHz.

In shutdown mode all circuitry is turned off and the W-5200−5 draw only leakage current from the V_{IN} supply. OUT is disconnected from IN. The $\overline{SHDN}$ pin is a CMOS input with a threshold voltage of approximately 0.8 V. The W-5200−5 is in shutdown when a logic LOW is applied to the $\overline{SHDN}$ pin. The $\overline{SHDN}$ pin is a high impedance CMOS input. $\overline{SHDN}$ does not have an internal pull−down resistor and should not be allowed to float and. It must always be driven with a valid logic level.

Short−Circuit and Thermal Protection

The W-5200−5 have built−in short−circuit current limiting and over temperature protection. During overload conditions, output current is limited to approximately 225 mA. At higher temperatures, or if the input voltage is high enough to cause excessive chip self heating, the thermal shutdown circuit shuts down the charge pump as the junction temperature exceeds approximately 160°C. Once the junction temperature drops back to approximately 140°C, the charge pump is enabled.

The W-5200−5 will cycle in and out of thermal shutdown indefinitely without latch−up or damage until a short−circuit on OUT is removed.

Application Information

Ceramic Capacitors

Ceramic capacitors of different dielectric materials lose their capacitance with higher temperature and voltage at different rates. For example, a capacitor made of X5R or X7R material will retain most of its capacitance from – 40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range.

Z5U and Y5V capacitors may also have voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. When comparing different capacitors it is often useful consider the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. For example, over rated voltage and temperature conditions, a 1 μF, 10 V, Y5V ceramic capacitor in an 0603 case may not provide any more capacitance than a 0.22 μF, 10 V, X7R available in the same 0603 case. For many W-5200/ W-5200–5 applications these capacitors can be considered roughly equivalent.

The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure the desired capacitance at all temperatures and voltages. Below is a list of ceramic capacitor manufacturers and how to contact them:

Table 5. CERAMIC CAPACITOR MANUFACTURERS

Capacitor Manufacturer	Web	Phone
Murata	www.murata.com	814.237.1431
AVX/Kemet	www.avxcorp.com	843.448.9411
Vishay	www.vishay.com	
Kemet	www.kemet.com	408.986.0424
Taiyo Yuden	www.t–yuden.com	408.573.4150

Thermal Management

For higher input voltages and maximum output current there can be substantial power dissipation in the W-5200–5. If the junction temperature increases to 160°C, the thermal shutdown circuitry will automatically turn off the output.

A good thermal connection to the PC board is recommended to reduce the chip temperature. Connecting the GND pin (Pin 2) to a ground plane, and maintaining a solid ground plane under the device reduces the overall thermal resistance.

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\Theta_{JC}) + P_D (\Theta_{CA})$$
$$= T_{AMB} + P_D (\Theta_{JA})$$

The SOT23 package, when mounted on printed circuit board with two square inches of copper allocated for "heat spreading", will result with an overall θ_{JA} of less than 150°C/W.

For a typical application operating from a 3.8 V input supply, the maximum power dissipation is 260 mW (100 mA x 3 V). This would result if a maximum junction temperature of:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JA})$$
$$= 85°C + 0.26\ W\ (150°C/W)$$
$$= 85°C + 39°C = 124°C$$

The use of multi–layer board construction with power planes will further enhance the overall thermal performance. In the event of no dedicated copper area being used for heat spreading, a multi–l ayer board will typically provide the with an overall θ_{JA} of 200°C/W. This level of thermal conduction would allow up to 200 mW be safely dissipated within the device.

Typical Applications

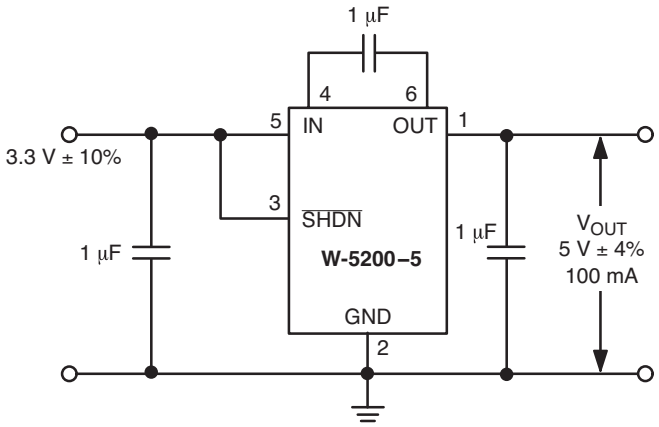


Figure 15. 3.3 V Supply to 5 V

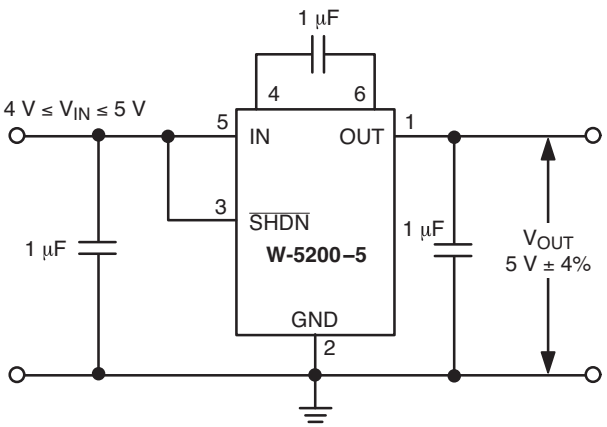


Figure 16. USB Port to Regulated 5 V Power Supply

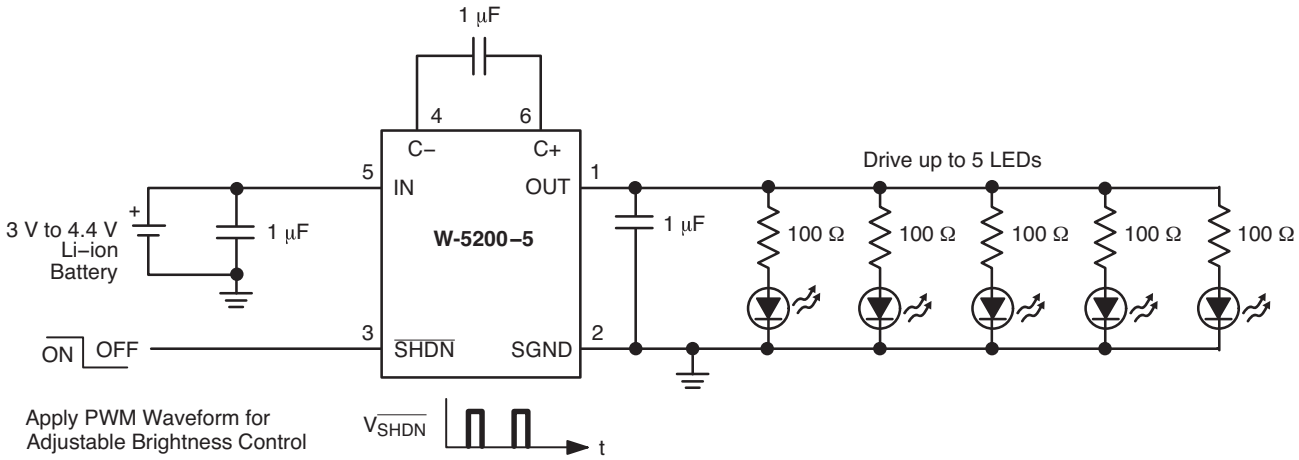
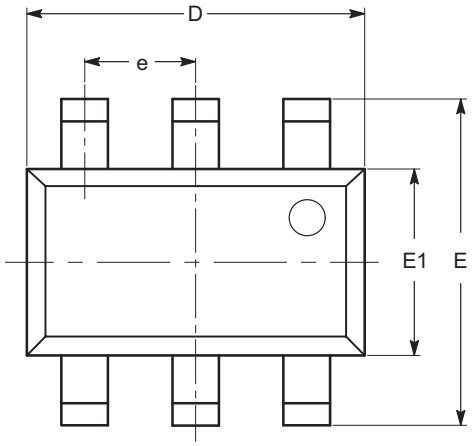


Figure 17. Lithium–I on Battery to 5 V White or Blue LED Driver

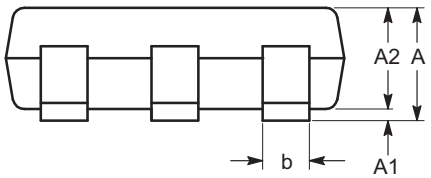
PACKAGE DIMENSIONS

TSOT–23, 6 LEAD
CASE 419AF–01
ISSUE O

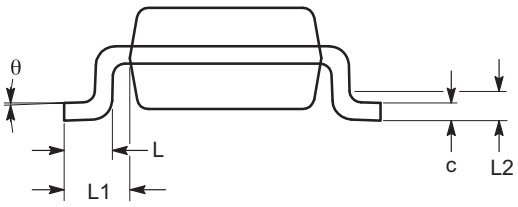


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 TYP		
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
θ	0°		8°



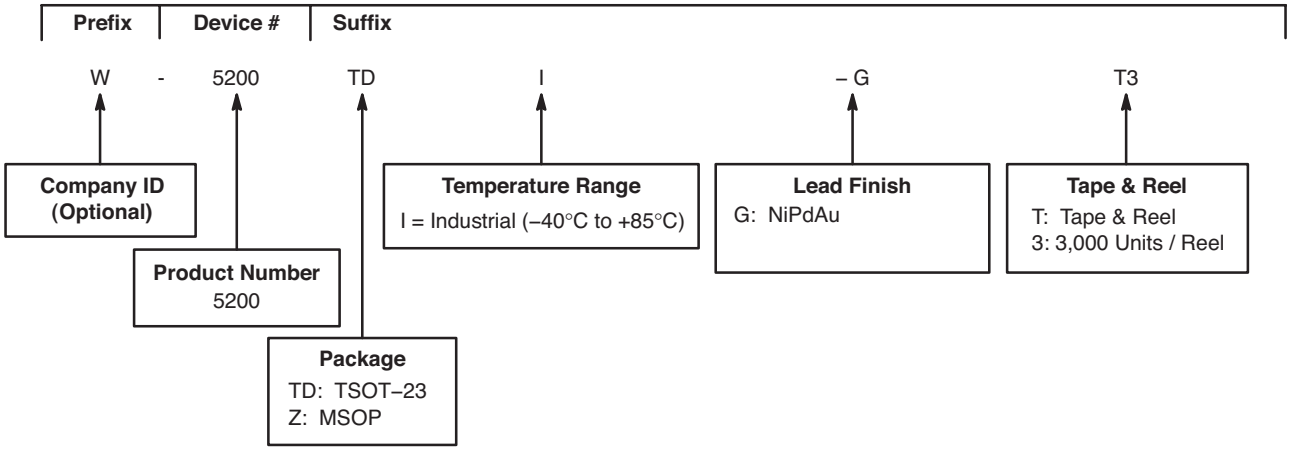
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

Example of Ordering Information (Note 5)



3. All packages are RoHS–compliant (Lead–free, Halogen–free).
4. The standard lead finish is NiPdAu.
5. The device used in the above example is a W-5200TDI–GT3 (TSOT–23, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).